PSET 4

1.1(a) The longest path through the 8 bit combinational multiplier is the latency.

1 AND + 20 FA = $1 \times 2 + 20 \times 3 = 62$ ns

Latency: 62ns

Throughput = 1/Latency = 1/62

1.1b) Explanation:

Each wire connecting b_n going to AND w/ a_m and b_n going to and w/ a_{m+1} should have 0 reg.

Each wire connecting a_m row x and a_m row $x+1$ should have 1 register.

The wires after AND and after FA blocks should have 1 register.

The output S_n should have # registers equal to $15-n$. except S_{15} has 1 register

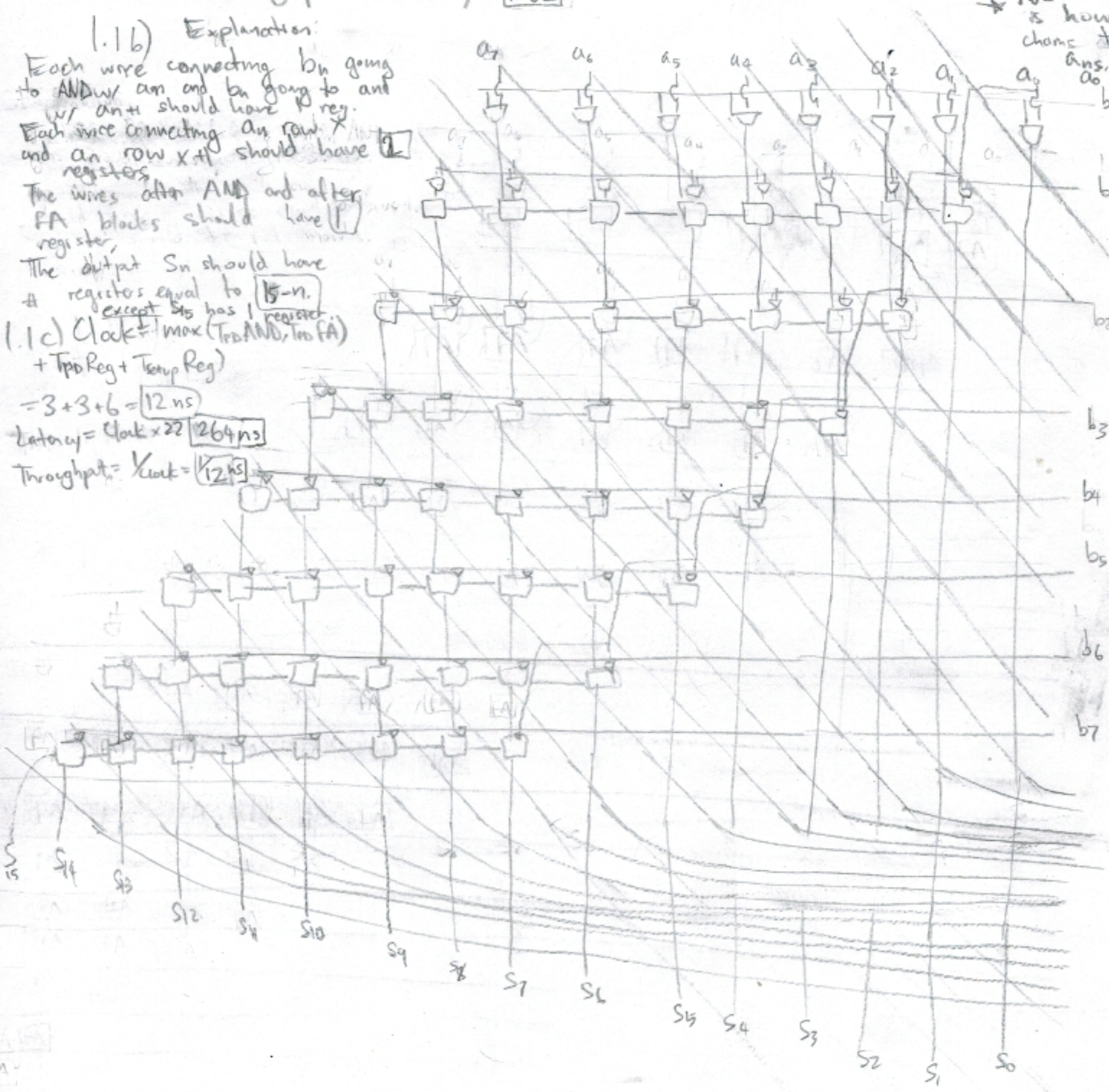
1.1c) Clock = max(TpdAND, TpdFA) + TpdReg + TsetupReg)

$= 3+3+6 =$ 12 ns

Latency = Clock × 22 = 264 ns

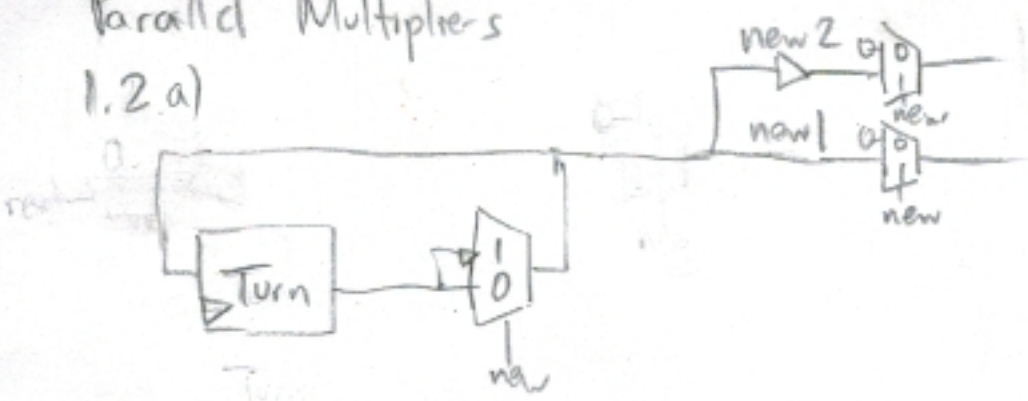
Throughput = 1/Clock = 1/12 ns

* Not shown is how an change to late a_{ns}. Only a_0 is change

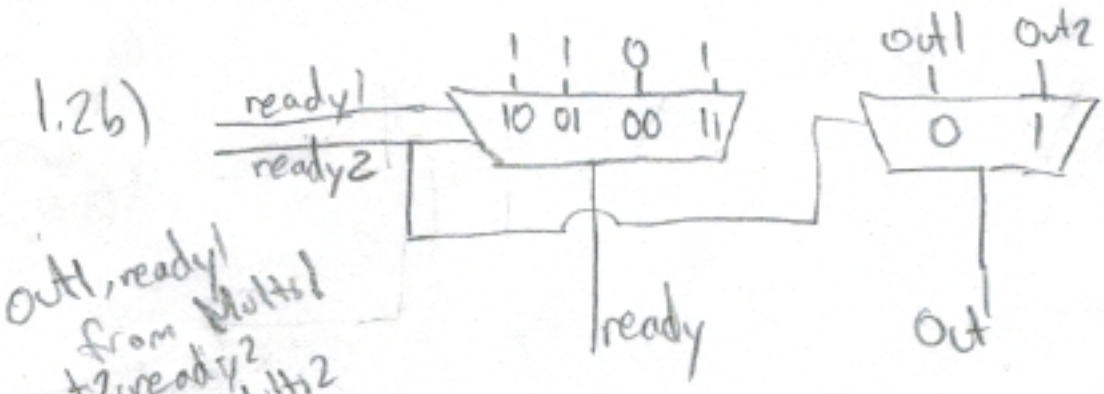


Parallel Multipliers

1.2 a)

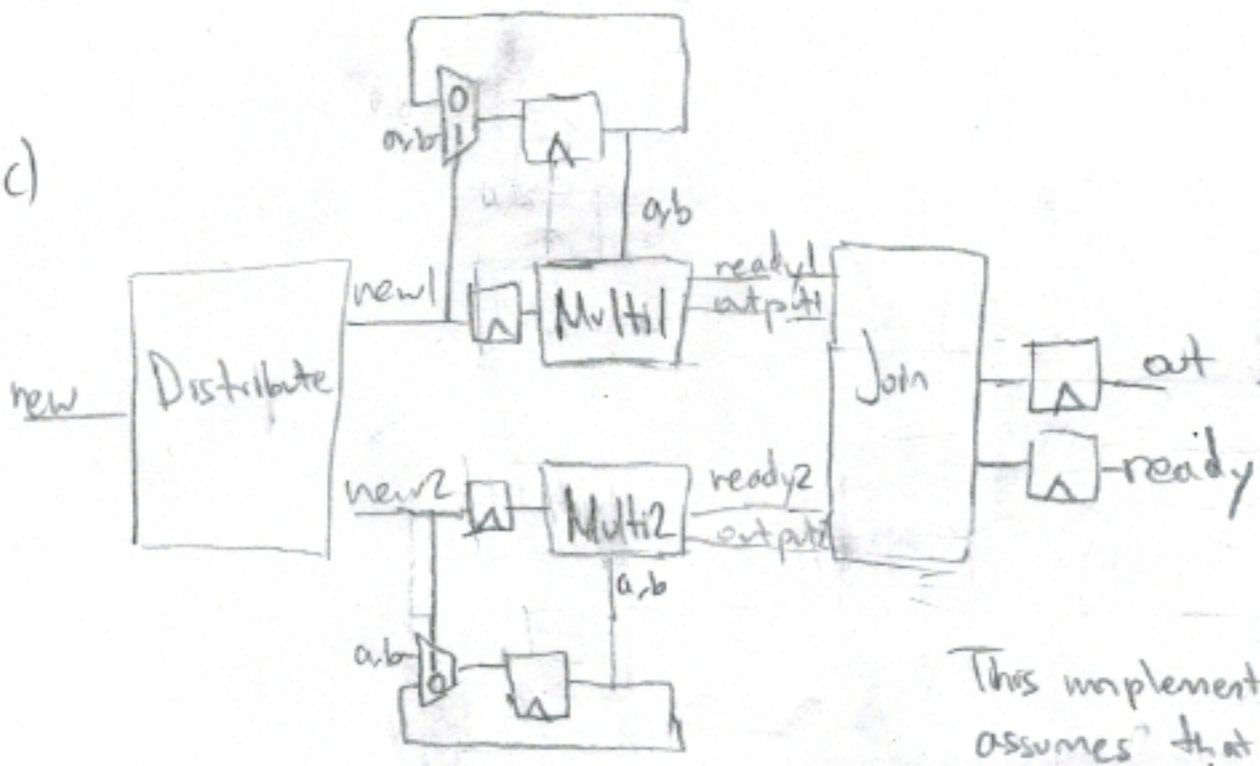


1.2b)



Note: In case where both are ready, (should never happen if multipliers are offset correctly), this join will flash ready and output 2.

1.2c)



Latency = 10 Clk = 10 × 62 = 6

Throughput = $\frac{2}{10 Clk} = \frac{1}{5 Clk}$

$= \frac{1}{5 \times 62} = .003$

This implementation assumes that arb input must be held for multi and multi2.

1.2d) Transistors in FA: 28

Transistors in AND: 4

Transistors in 8bit Multiplier: 64 AND + 56 FA = 64 × 4 + 56 × 28 = 1824

Transistors in Dreg: 2 Dlatch = 2 × 2:1 Mux = 4 × #bits

Transistors in 2:1 Mux: 2 × #bits

Transistors in 4:1 Mux: 3 × 2:1 Mux = 6 × #bits

Transistors in Pipelined 1.1 Multiplier: 8bit Multiplier + [(64 + 56) − 16] × Dreg + 3 × 7 × 7 + $\left(\sum_{n=1}^{15} n\right.$ +

Roughly = 1824 + (281) 4 = 1824 + 1484 = 3308

Transistors in 1.2 Parallel Multiplier: 2 Multipliers + 4 Dreg + 3 × Dreg × 16 + 2:1 Mux × 16 + 2:1 Mux × 3 + 2 Inv + 4:1 Mux + 2:1 Mux × 16

= 2(1824) + 4(4) + 3(4)(16) + (2)(16) + 2(3) + 2(2) + 3 × 2 + 2 × 16 = 3936

Thus, 1.1 wins in terms of area and throughput, 1.2 wins in terms of latency.