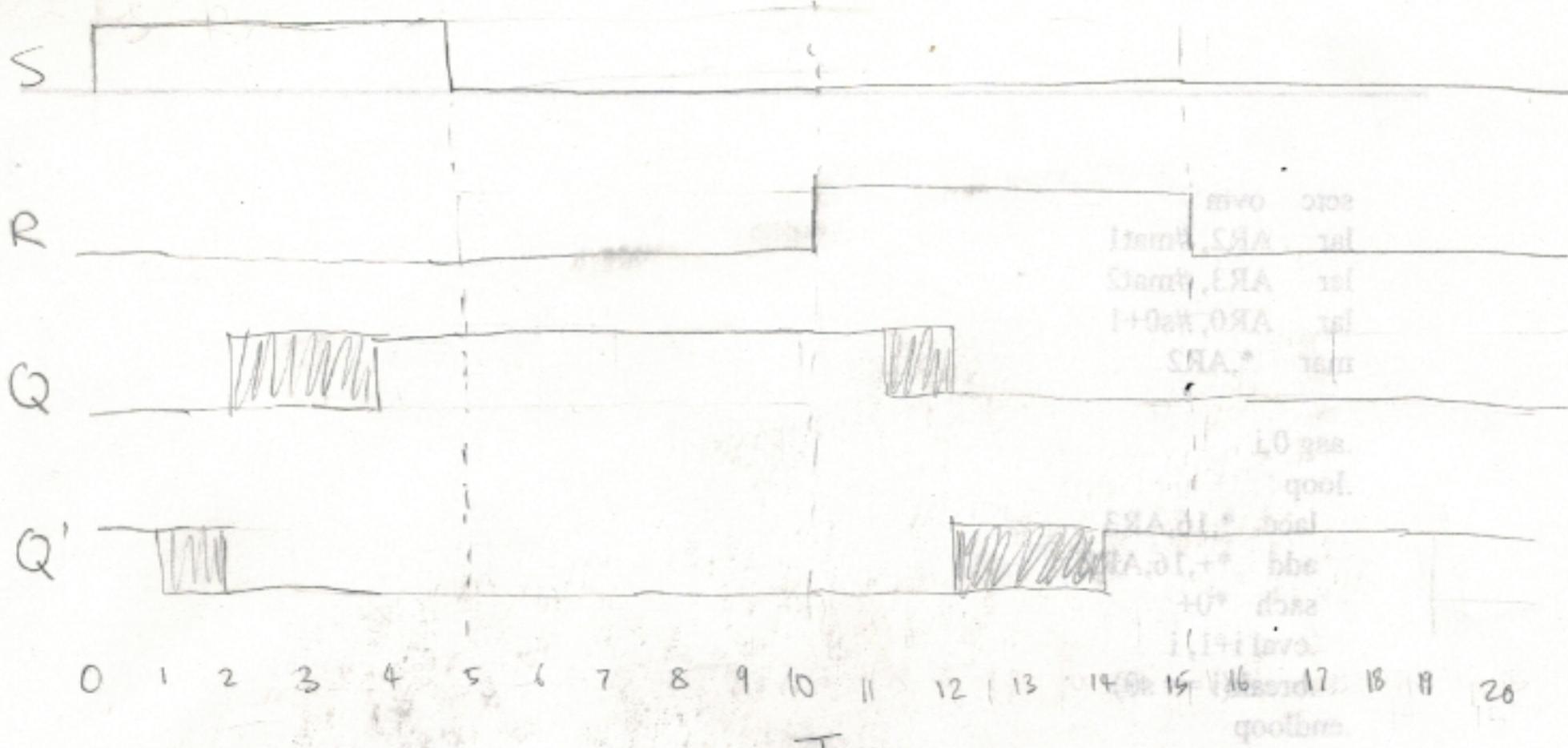


1.0a

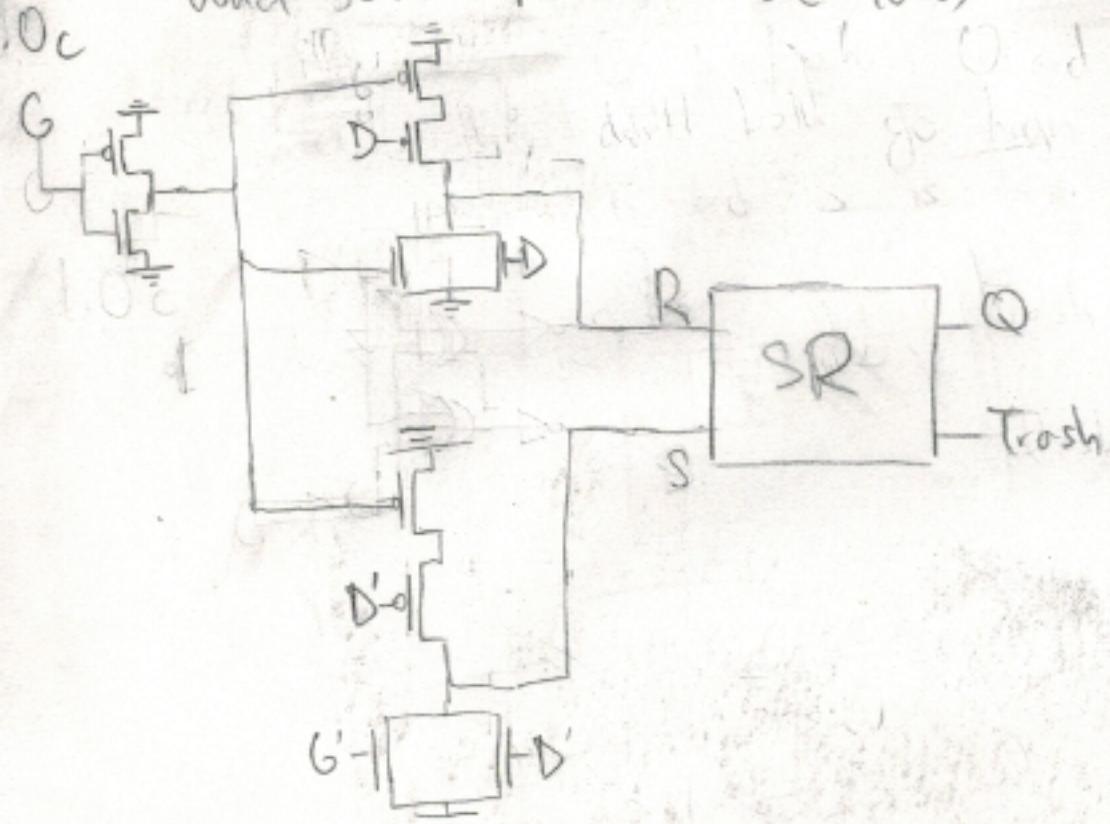


1.0b

	(No Change) $R=0, S=0$	$(Q=1)$ $R=1, S=0$	$(Q=0)$ $R=0, S=1$	(Invalid) $R=1, S=1$ (Clashed)
T_{change}	0	4	4	N/A

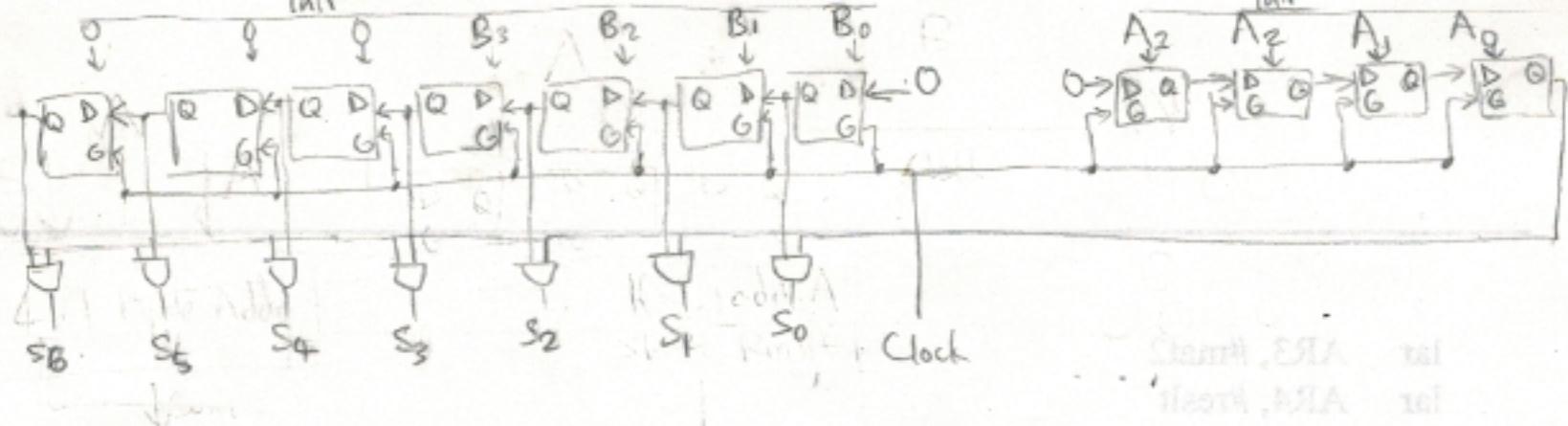
1.0c

When both R and S are low, Q and Q' won't change

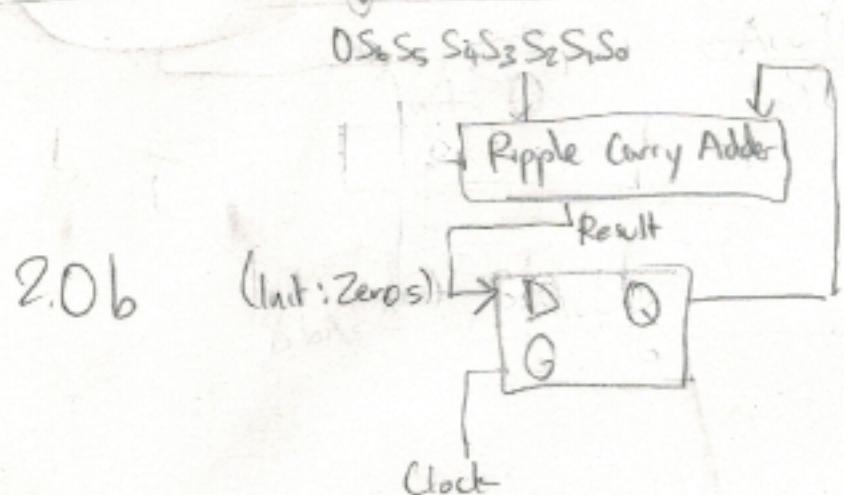


G	D	S	R	Q Hold
0	x	0	0	1
1	1	1	0	0
1	0	0	1	0

$$\begin{aligned} S &= G \& D \\ R &= G \& \bar{D} \end{aligned}$$



Registers of width 7 and 4 for storage of B and A

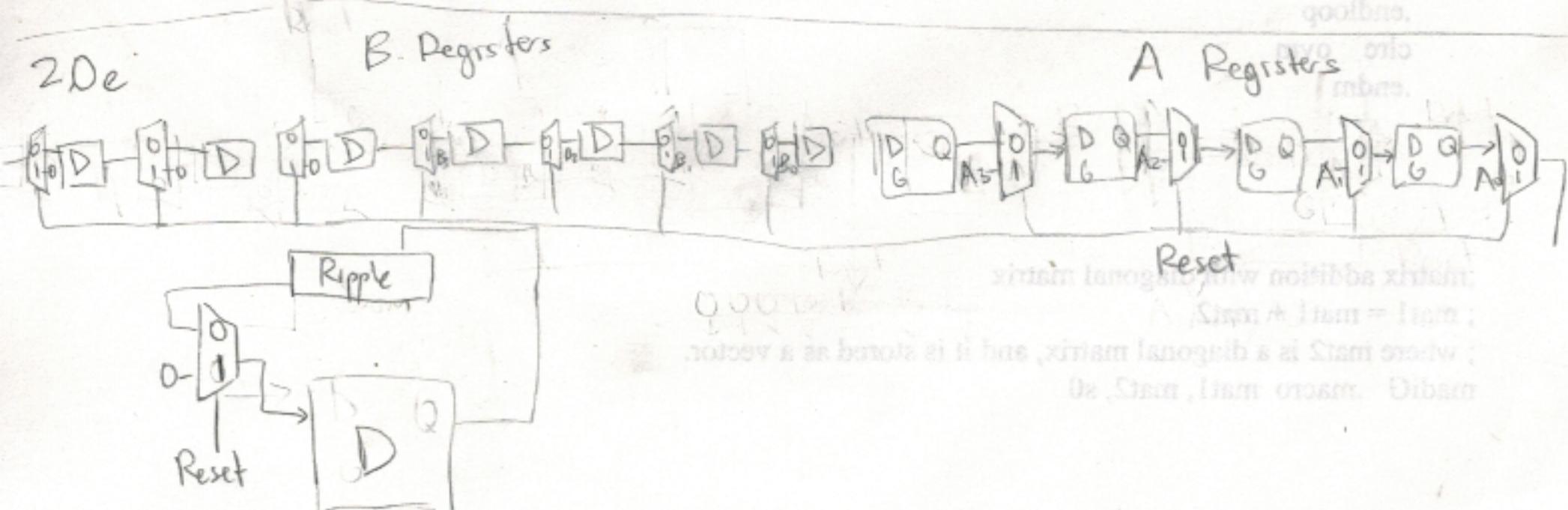


8 bit Ripple Adder

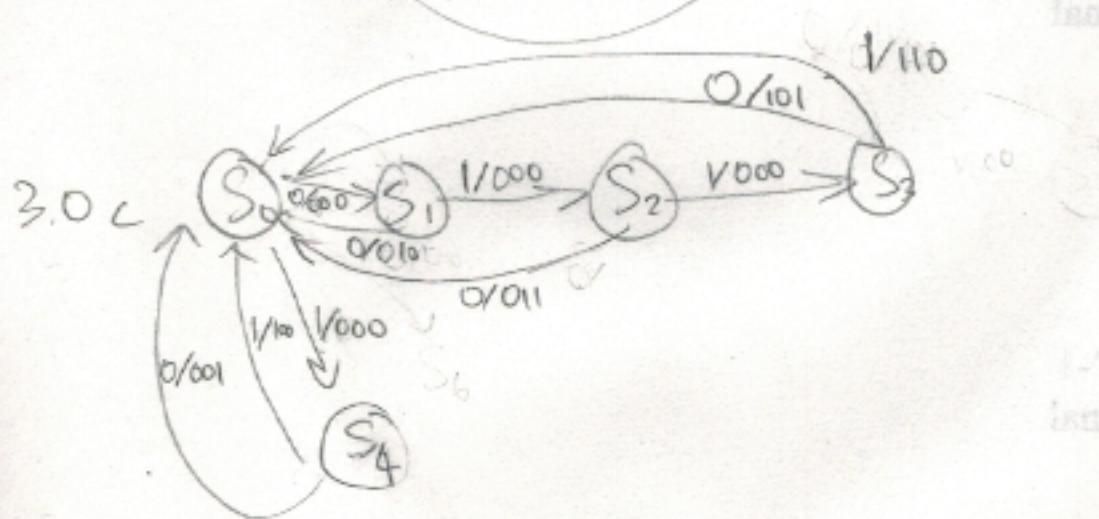
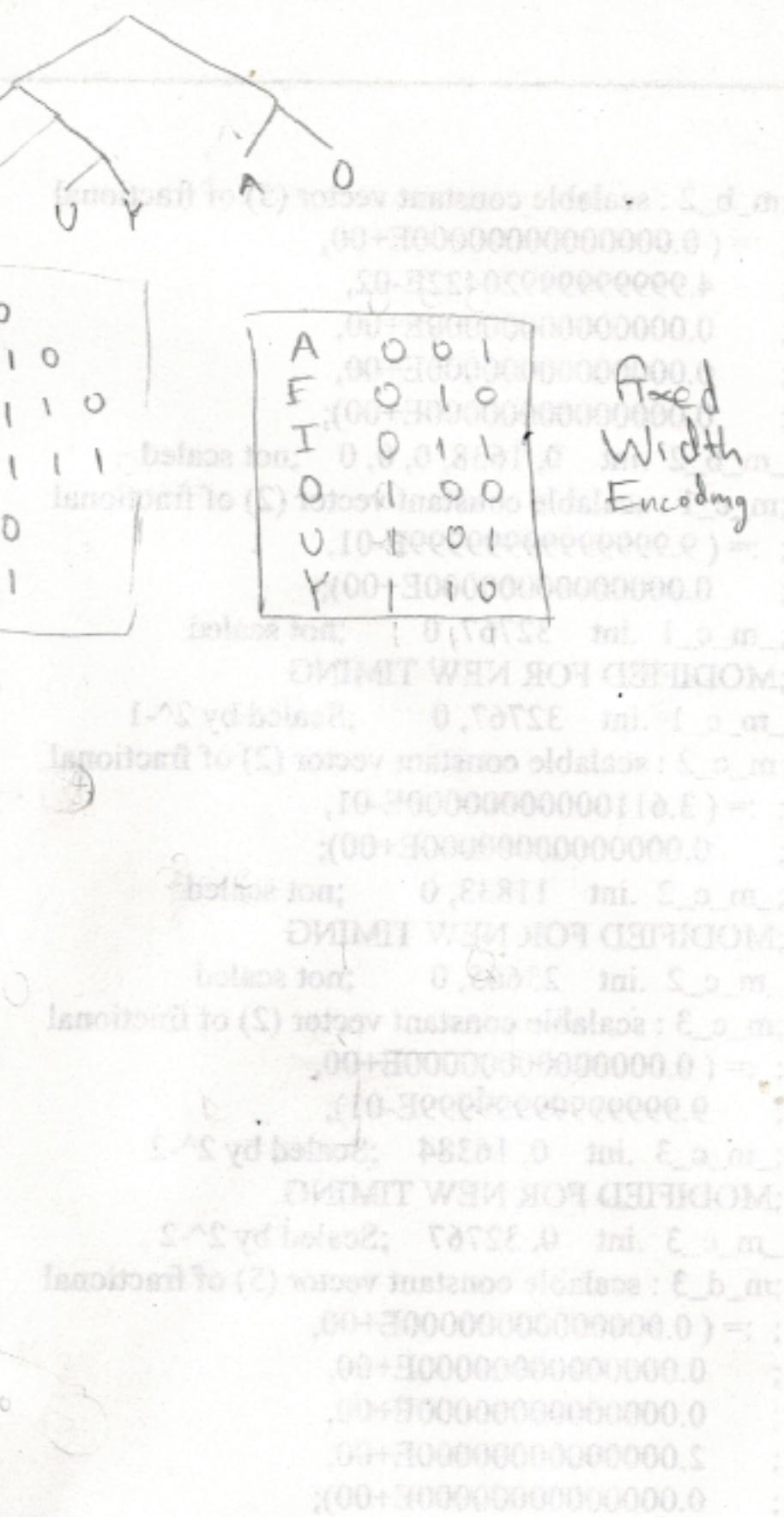
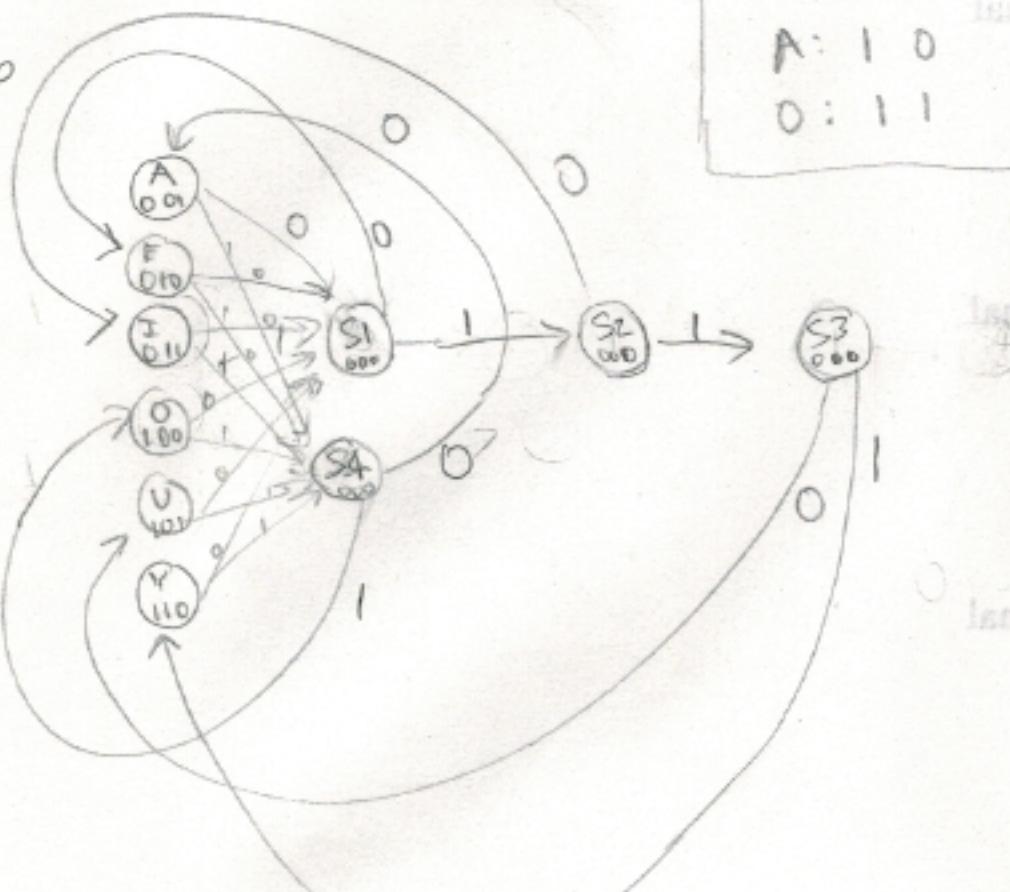
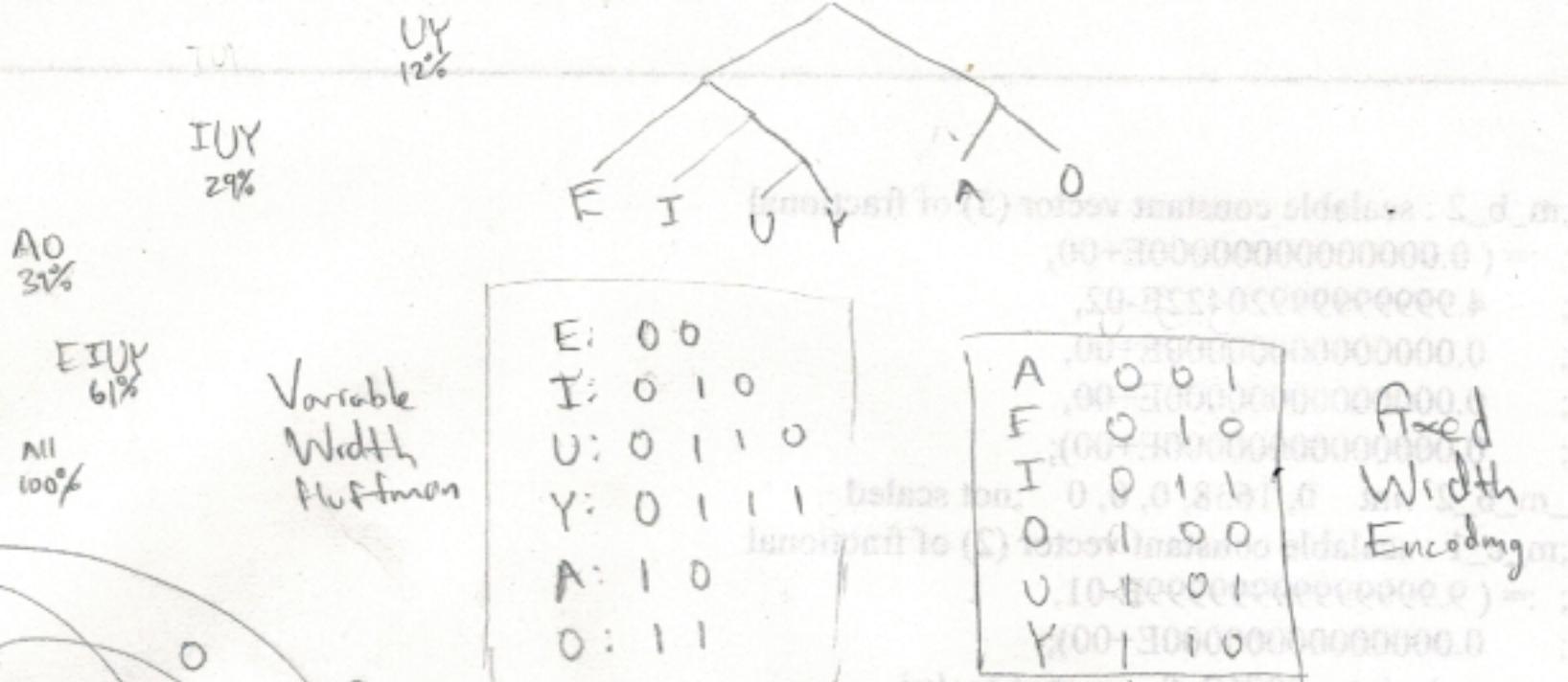
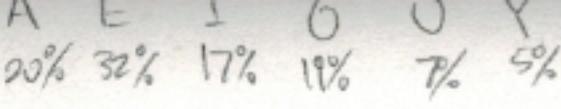
8-bit Register for Accumulator.

20c

2.0 d. Shifters: $T_c \geq t_{\text{setup}} + t_{\text{PD} \text{avg}} + t_{\text{PD} \text{Rip}_b} + t_{\text{PD} \text{A/B}}$
 $t_{\text{hold}} \leq t_{c_d \text{shutter}}$

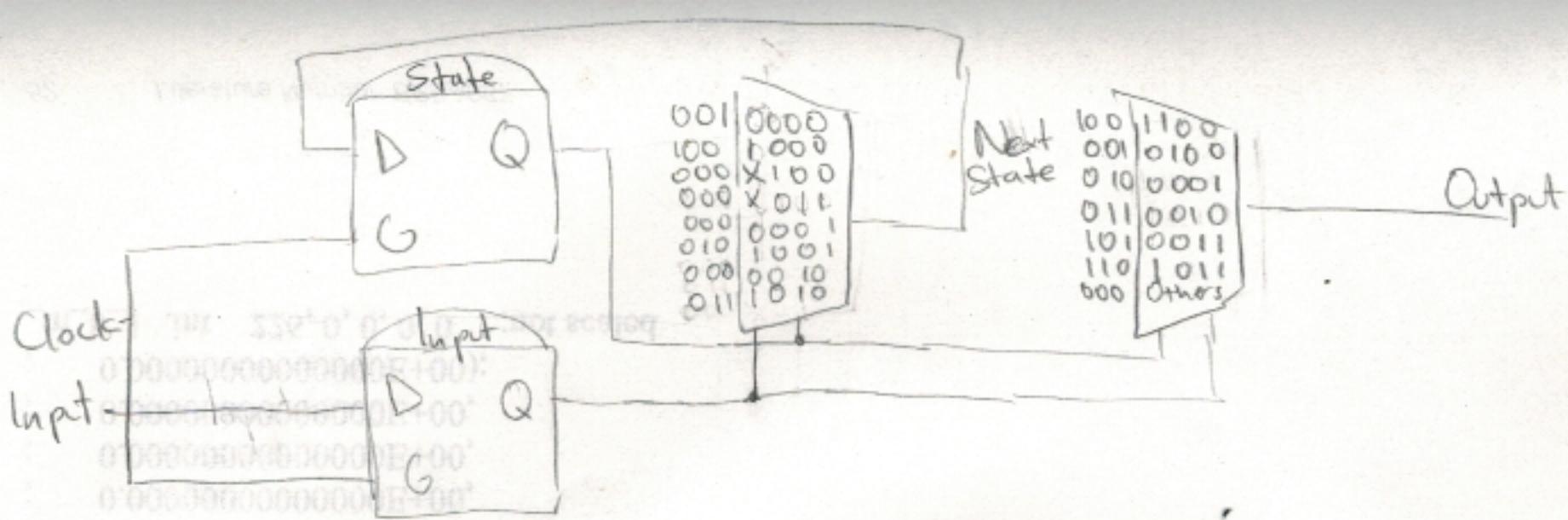


Sum. Register



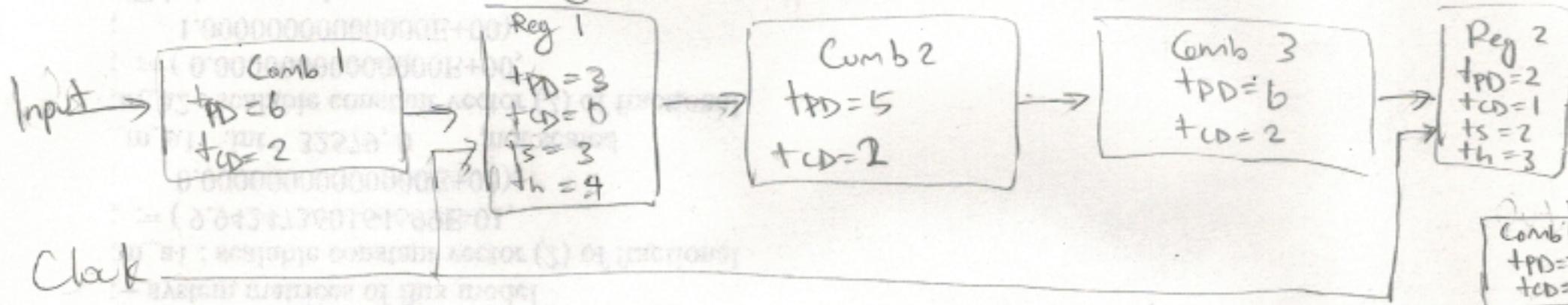
3.0 d	Input	PrevState	NewState	Output
	0	000	001	000
	1	000	100	000
	1	100	000	100
	0	100	000	001
	0	001	000	010
	1	001	010	000
	0	010	000	011
	1	010	011	000
	0	011	000	101
	1	011	000	110

3.0 e



4.0

Consider the following Circuit:

4.0a What's the relationship between t_{HR2} , t_{CDR1} , t_{CDC2} , and t_{CDC3} ?

$$t_{HR2} \leq t_{CDC2} + t_{CDC3} + t_{CDR1}$$

Is this relationship satisfied in this circuit?

$$3 \leq 2+2+0 \quad \checkmark \text{ Yes,}$$

4.0b What's the contamination and propagation delay of this system?

The CD/PD of the system is equal to the CD/PD of the output

$$\begin{aligned} t_{CD} &= t_{CDR2} + t_{CDC4} \\ &= 1+3 = 4 \end{aligned} \quad \begin{aligned} t_{PPD} &= t_{PPDR2} + t_{PPC4} \\ &= 2+7 = 9 \end{aligned}$$

4.0c What's the setup and hold time of the system?

The setup/hold time depends on the input.

$$t_s = t_{sR1} + t_{PPCK}$$

$$= 6+3 = 9$$

$$t_h = t_{hR1} - t_{sCK} \\ = 4-2 = 2$$

4.0d What's the clock period of the system?

$$t_{clock} \geq t_{PD R1} + t_{PD C2} + t_{PD C3} + t_{sR2} = 3+5+6+2 = 16$$

The clock period must be greater than the maximum time for a signal to go from R_1 to R_2 and get set up by R_2 .

```
t_hold <= t_CD,mux + t_CD,dregister + t_CD,ripplecarryadder  
t_clock >= t_PD,reg + t_PD,mux + t_PD,ripplecarryadder + t_Setup,dregister
```