# 數位電路設計

# Lab3 – 同步循序電路之 HDL 模組撰寫與測試

## 1. 目標(Goal)

在這次 Lab 中，我們希望同學們可以熟悉 Latch、正反器、同步循序電路的設計原理。以 **state-diagram-based model 與 structural model** 等不同方式撰寫同步循序電路之 Verilog HDL 電路模組，並撰寫測試模組。分別模擬後，繳交模組檔案與波形圖。

The main purpose of this Lab Unit is to be familiar with the design of latch, flip-flop, and synchronous sequential circuit. Please write the Verilog HDL circuit modules of synchronous sequential circuits by state-diagram-base model and structural model, and write the testbench for these circuit modules. After simulation, upload the files of the modules and the waveforms of the simulation results.

## 2. 撰寫 HDL 電路模組與測試模組(Design of the HDL Circuit Modules and Testbench)

**A.** $\overline{S}\,\overline{R}$ -Latch**:** 下圖為一 $\overline{S}\,\overline{R}$ -Latch 的電路圖，請設計其 Verilog HDL 電路模組。

The circuit diagram of a $\overline{S}\,\overline{R}$ -Latch is shown in the following figure. Please write the Verilog circuit module for it.

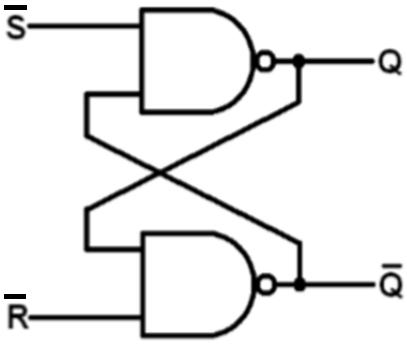


圖 1：$\overline{S}\,\overline{R}$ -Latch 的電路圖

Figure 1: The circuit diagram of an $\overline{S}\,\overline{R}$ -Latch.

i. 請根據上述電路圖(圖 1)，以 gate-level modeling 的方式撰寫其電路模組。假設每個 NAND gate 的 delay 為 5 *ns*。模組名稱與 port list 請訂為 Lab3_SbRb_Latch_gatelevel(input Sb, Rb, output Q, Qb)，檔案則請命名為 Lab3_SbRb_Latch_gatelevel.v。

According to the logic diagram shown in Figure 1, please write the Verilog circuit module in gate-level modeling. Assume that the delay of an NAND gate is 5 *ns*. The circuit module and port list should be named as Lab3_SbRb_Latch_gatelevel(input Sb, Rb, output Q, Qb),

and its file should be named as Lab3_SbRb_Latch_gatelevel.v.

ii. 請撰寫此$\overline{S}\,\overline{R}$-Latch 之測試電路模組，必須至少包含下述指定之測資。請將此測試電路模組命名為 t_Lab3_SbRb_Latch_gatelevel，檔案則命名為 t_Lab3_SbRb_Latch_gatelevel.v。

Please write the testbench of the $\overline{S}\,\overline{R}$-Latch in which the test data shown in the following table must be included. The testbench module should be named as t_Lab3_SbRb_Latch_gatelevel, and its file should be named as t_Lab3_SbRb_Latch_gatelevel.v.

| Time (ns) | Sb | Rb |
|---|---|---|
| 0 | 0 | 1 |
| 30 | 1 | 1 |
| 60 | 1 | 0 |
| 90 | 1 | 1 |
| 120 | 0 | 0 |
| 150 | 1 | 1 |
| 180 | 0 | 1 |

**B. D-type Positive Edge Trigger Flip-Flop:** 下圖為一正緣觸發的 D-Flip-Flop，請設計其 Verilog HDL 電路模組。

The circuit diagram of a D-type positive-edge triggered Flip-Flop is shown in the following figure. Please design the Verilog circuit module for it.

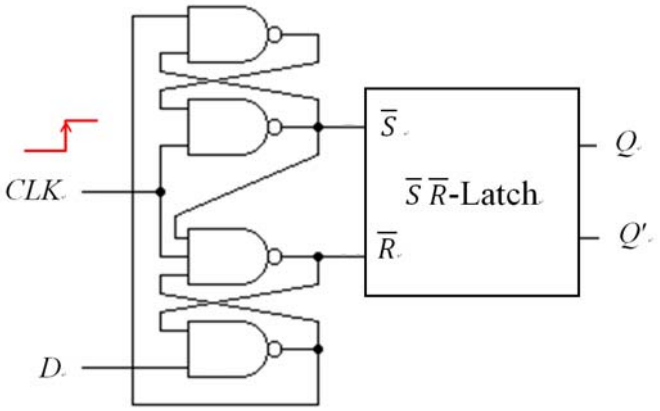


圖 2：正緣觸發的 D-Flip-Flop 電路圖

Figure 2: The circuit diagram of a positive-edge triggered D-Flip-Flop.

i. 請根據上述電路圖(圖 2)，利用 A(i)的 module，以 gate-level modeling 的方式撰寫其電路模組。假設每個 NAND gate 的 delay 為 5 *ns*。模組名稱與 port list 請訂為 Lab3_PE_Dff_gatelevel(input D, clock, output Q, Qb)，檔案則請命名為 Lab3_PE_Dff_gatelevel.v。

According to the logic diagram shown in Figure 2, please write the Verilog circuit module in gate-level modeling by using the module in A(i). Assume that the delay of an NAND gate is 5 *ns*. The circuit module and port list should be named as

Lab3_PE_Dff_gatelevel(input D, clock, output Q, Qb), and its file should be named as Lab3_PE_Dff_gatelevel.v.

ii. 請撰寫此 D-flip-flop 之測試電路模組，clock 之週期為 40 ns (20 ns 為 LOW、20 ns 為 HIGH)，且至少必須包含下述指定之測資。請將此測試電路模組命名為 t_Lab3_PE_Dff_gatelevel，檔案則命名為 t_Lab3_PE_Dff_gatelevel.v。

Please write the testbench of this D flip-flop in which the test data shown in the following table must be included. The period of the clock is 40 ns, LOW for 20 ns and then HIGH for 20 ns. The testbench should be named as t_Lab3_PE_Dff_gatelevel, and its file should be named as t_Lab3_PE_Dff_gatelevel.v.

| Time(ns) | D |
|---|---|
| 0 | 1 |
| 25 | 0 |
| 65 | 1 |
| 88 | 0 |
| 122 | 1 |
| 195 | 0 |

**C. Mealy-Type Synchronous Sequential Circuit:** 設計一個 Mealy-type 的同步順序電路，此電路為序列識別器(sequence recognizer)，有一個輸入變數($x$)、一個輸出變數($z$)。當輸入序列以 010 或 1001 結束時，輸出 z 為 1；其餘情況，輸出為 0。圖 3 為此順序電路之狀態圖(state diagram)，表 1 為其狀態表(state table)。狀態 $S_0$ 是電路的初始狀態。在本電路的設計中無需考慮 delay 的問題。

Design a Mealy-type synchronous sequential circuit which is a sequence recognizer with one input variable $x$ and one output variable $z$. The output $z$ should be 1 if the input sequence ends in either 010 or 1001 and $z$ should be 0 otherwise. The state diagram of the sequential circuit is shown in Figure 3 and its corresponding state table is shown in Table 1. State $S_0$ is the initial state of the circuit. There is no need to consider the issue of delay in the design of this circuit.

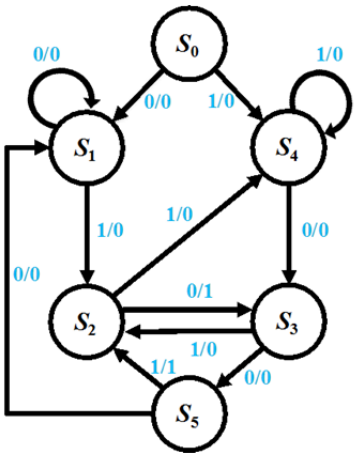


圖 3：序列識別器之狀態圖

Figure 3: The state diagram of the sequence recognizer for “010” and “1001”.

表 1：序列識別器之狀態表

Figure 3: The state table of the sequence recognizer for “010” and “1001”.

| Present State | Next State | | Output | |
|---|---|---|---|---|
| | $x = 0$ | $x = 1$ | $x = 0$ | $x = 1$ |
| $S_0$ | $S_1$ | $S_4$ | 0 | 0 |
| $S_1$ | $S_1$ | $S_2$ | 0 | 0 |
| $S_2$ | $S_3$ | $S_4$ | 1 | 0 |
| $S_3$ | $S_5$ | $S_2$ | 0 | 0 |
| $S_4$ | $S_3$ | $S_4$ | 0 | 0 |
| $S_5$ | $S_1$ | $S_2$ | 0 | 1 |

i. 請根據此電路之狀態圖(圖 3)或狀態表(表 1)，以 **state-diagram-based** model 方式撰寫其 Verilog HDL 電路模組。各狀態之二元編碼為 $S_0$ = 000, $S_1$ = 001, $S_2$ = 010, $S_3$ = 011, $S_4$ = 100, $S_5$ = 101。假設此同步順序電路在 clock 之正緣觸發其狀態改變，且有 reset 輸入訊號；reset 訊號為 Active LOW，可設定電路至初始狀態 $S_0$ (000)。模組名稱與 port list 請訂為 Lab3_Sequence_Recognizer_state_diagram (input x, clock, reset, output z)，檔案則請命名為 Lab3_Sequence_Recognizer_state_diagram.v。

According to the state diagram shown in Figure 3 or the state table shown in Table 1, write the Verilog circuit module for this synchronous sequential circuit by **state-diagram-based** model. The binary assignment of the states are $S_0$ = 000, $S_1$ = 001, $S_2$ = 010, $S_3$ = 011, $S_4$ = 100, $S_5$ = 101. Assume that this circuit is positive-edge triggered and has an active-LOW *reset* signal which may reset the circuit to its initial state $S_0$ (000). The circuit module and port list should be named as Lab3_Sequence_Recognizer_state_diagram (input x, clock, reset, output z), and its file should be named as Lab3_Sequence_Recognizer_state_diagram.v.

ii. 完成此同步順序電路之設計，以 D 正反器做為其儲存元件。根據推導出之電路圖，以 **structural model** 方式撰寫其 Verilog HDL 電路模組。各狀態之二元編碼同 i.所訂。假設此電路有 reset 輸入訊號，可設定電路至初始狀態 $S_0$ (000)。模組名稱與 port list 請訂為 Lab3_Sequence_Recognizer_structure (input x, clock, reset, output z,)，檔案則請命名為 Lab3_Sequence_Recognizer_structure.v。請注意，此電路模組中需要用到有 asynchronous reset (又稱 direct reset) 之 D flip-flop 的電路模組，可自行撰寫或使用課本上之模組，檔案請命名為 D_ff_AR.v。此正反器應為正緣觸發，其 *reset* 訊號為 Active-LOW。

Complete the design of this synchronous sequential circuit by using D flip-flops. According to the circuit diagram derived, write the Verilog circuit module for this circuit by **structural model**. The binary assignments of the states are the same as that defined in (i.). Assume that the circuit can be reset to its initial state $S_0$ (000) by input signal *reset*. The circuit module and port list should be named as Lab3_Sequence_Recognizer_structure (input x, clock, reset, output z), and its file should

be named as Lab3_Sequence_Recognizer_structure.v . Note that this circuit module requires to instantiate the circuit module of a D flip-flop with *asynchronous reset*, also called as *direct reset*. You may design the D flip-flop module by yourself or apply the module provided in the textbook. The file of the D flip-flop should be named as D_ff_AR.v. Assume that the flip-flop is positive-edge triggered and the *reset* signal is active-LOW.

iii. 請撰寫一測試模組來完整測試上述兩個電路模組。請將此測試模組命名為 t_Lab3_Sequence_Recognizer，檔案則請命名為 t_Lab3_Sequence_Recognizer.v。
Please write a testbench to test the two circuit modules designed above thoroughly. The testbench module should be named as t_Lab3_Sequence_Recognizer, and its file should be named as t_Lab3_Sequence_Recognizer.v .

*** 注意事項：**

- 請用 Icarus Verilog 作為編譯器，以 vvp 執行，並以 GTKWave 觀察波形圖。
  Please compile your Verilog code by Icarus Verilog, execute the compiled code by vvp, and then observe the waveform by GTKWave.
- 請務必依照上述各項目之規定命名模組及檔案，違者至少扣 10 分。
  Be sure to name the modules and files as described above; otherwise, there will be 10 points penalty on your score at least.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point.
- 助教會以其他測資去測試上述作業。
  TA will use similar testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

## 3. 作業及 HDL 模組繳交(Hand in)

**A.** **作業報告繳交：pdf 檔，命名為 Lab3_學號**
包含下列項目：
**Hand in a pdf file, named Lab3_StudentID, including the following items:**

(1) 2A 之模擬結果波形圖，並說明其模擬結果波形圖是否正確。(20%)
Give the waveform of the simulation results in 2A, and explain whether it is correct or not.

(2) 2B 之模擬結果波形圖，並說明其模擬結果波形圖是否正確。(20%)
Give the waveform of the simulation results in 2B, and explain whether it is correct or not.

(3) 敘述 2C 之 Mealy-type 同步順序電路之設計過程，以 D 正反器為儲存元件，推導出其電路圖。而後，列出 2C 之模擬結果波形圖，並說明其 testbench 如何設計、針對 input stimulus 預期之狀態轉換與輸出值為何、及 i.和 ii.兩種電路模組之模擬結果波形圖是否正確。(50%)
Describe the design of the Mealy-type synchronous sequential circuit in 2C by using D

flip-flops based on the design procedure of synchronous sequential circuits. Then, give the waveform of the simulation results in 2C, explain how you design your testbench, show the state transitions and outputs for the input stimuli, and determine whether each of the two circuit modules designed by you is correct or not.

(4) 心得與感想、及遭遇到的問題或困難 (10%)

Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

**B. Verilog modules 檔案繳交：eight .v files**

**Hand in the following Verilog modules: 8 .v files**

Lab3_SbRb_Latch_gatelevel.v、t_Lab3_SbRb_Latch_gatelevel.v、
Lab3_PE_Dff_gatelevel.v、t_Lab3_PE_Dff_gatelevel.v、
Lab3_Sequence_Recognizer_state_diagram.v、Lab3_Sequence_Recognizer_structure.v、
D_ff_AR.v、t_Lab3_Sequence_Recognizer.v

# 4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (pdf file) and the corresponding HDL code (.v files) onto e-Campus platform.
- **作業繳交截止日期為 2021/5/31 (一) 23:55。不接受逾期繳交。**
  The deadline for handing in lab report and Verilog files is **2021/5/31 (Monday) 23:55. No late hand-in is allowed.**
- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** (禁止上傳 rar 檔或是其他檔案格式)，並以「Lab3_學號」的方式命名，如：「Lab3_0816000」。壓縮檔案時，請選取好要求繳交的檔案執行壓縮，不要對整個資料夾壓縮。
  Please compress the pdf file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file (rar file or other format is not accepted), and name the zip file as "Lab3_StudentID" , for example, "Lab3_0816000". When compressing files, please select the requested files for compression, and do not compress the entire directory.
- 上機演示 Demo 時間暫定為 **2021/6/2 (三) 10:00AM~9:00PM**，之後會再發公告通知大家上網填寫 Demo 時間表。未繳交作業者，將不予 Demo;有繳交作業但未 Demo 者，亦不予計分。
  The time for on-line demo is arranged at **2021/6/2 (Wed.) 10:00AM~9:00PM** tentatively, and we will send an announcement to inform you to fill the Demo schedule online. Those who have not hand-in their lab reports and Verilog files will not be able to demo their work.
- 程式碼請勿抄襲別人或讓別人抄襲，經查證後此次 lab 總分一律以 0 分計算。
  **Any assignment work by fraud will get a zero point.**