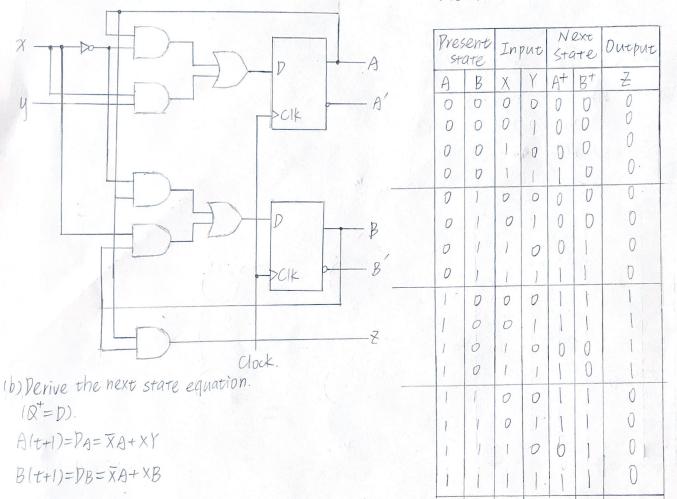
34.

$$DA = \overline{A}A + XY$$

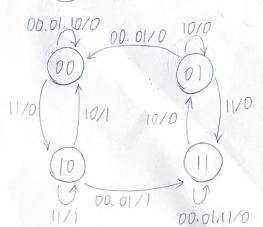
(a) Draw the logic diagram of the circuit.

(C) Complete the transition/state table of the circuit.



(d) Draw the state diagram.

State AB Input/Output XY/Z.



(e) was figgered and one of the the same dragorin

Cycle	0	45	2	3	4	5	6	2	
xy	01	1.1	1)	00	bo	01	11	10	No. of
AB	00	00	10	10	11.	01	00	10	00
Z	0	0	P.	1	0	0	0		0

35.
(a) Derive the memory Input equation and the output equation.

(b) Perive the next state equation

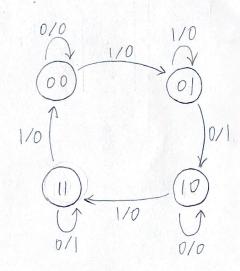
$$= \pi A'B + (X + B)A' = \pi A'B + AB'$$

$$= \pi A'B + \pi A' + AB' = \pi B' + AB'$$

$$B^{+}=JBB'+KB'B=7B'+(7A'+7'A)B'$$

(0).

	sent ate	Input	Ne Sta	xt te	Output
A	B	7	A+	B+	Z
0	0	. 0	0	0	0
0	0	1	D		0
0	- 1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	0
1	0	J	1	1	0
1		0	1	1	1
1	11	1	0	0	0



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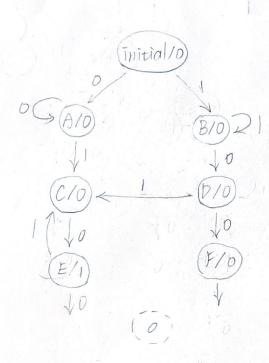
- $(0) \times OR + XOR = 2(ns) + 2(ns) = 4(ns)$
- (b) XOR+Inverter + Secup time = 2(ns)+0.5 (ns)+1(ns)=3,5(ns))
- (c) thp-flop\*2(sync Seq Ckt)+XOR+XOR=2(ns)+2(ns)+2(ns)=6(ns)
- (d) Flip-flop\*2(sync Seq Ckt)+XOR+ Setup time+Inverter=2(ns)+2(ns)+1(ns)+0.5(ns)=5.5(ns)
- (2) max (4. 3.3. 6. 5.5)=6(n5)=tp.

37.

(b)

cycle	1	2	3	4	5	6	2	8	9	10	11	12	. 13	14	15
Input	0	0	1	1	1	0		0	·I	0	01	> X	0.	1	
State	A	A	0	D	D								1	44	
Output	0	0	D	0	0	.0	0.	0	1	0	1	0	0	0	0
	4														

(a)

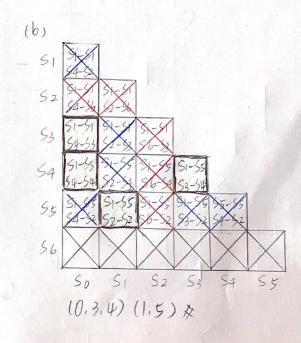


initial	
A = 0	
B=1	
C=01	1. 9 States
D=10	
E=010	
t=109	

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Present	Next	State X=1	DUT!	カルセ
So	51	54	0	0
51	51	52	0	0
52	51	56	0	0
53	51	53	0	0
54	55	54	0	0
55	S <sub>5</sub>	SZ	0	0
56	S5	53	0	

by row matching method can't find any equivalent states \*



$$QA(t+1) = DA(QA,QB,X) = \Sigma m(2,2)$$

$$QB(t+1) = DB(QA,QB,X) = \Sigma m(1,4,5)$$

$$Z(A,B,X) = \Sigma m(3,4)$$

$$QA(t+1) = QB$$

$$QA(t+1) = QB(t+1)$$

X

×

X

X

X