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HANDLERS.INC
                            Include File
; Timer Definitions
; Addresses
Tmr0Ctrl
             EQU
                   OFF56H
                                 ;address of Timer O Control Register
                   OFF52H
                                ; address of Timer O Max Count A Register
Tmr0MaxCntA
            EOU
Tmr0Count
                   OFF50H
            EQU
                                ;address of Timer O Count Register
; Control Register Values
Tmr0CtrlVal EQU
                   0E001H
                                 ; value to write to Timer O Control Register
                    ;0E009H
                                 :1----- enable timer
                                 ;-1---- write to control
                                 ;--1----- enable interrupts
                                 ;---000000---- reserved
;---0---- read only
;----- TMRINO is an enable
                                 ;-----2 count timer 2 outs
                                 ;----0- single counter mode
                                 ;----1 continuous mode
; Interrupt Vectors
Tmr0Vec EQU
                                ;interrupt vector for Timer 0
; Interrupt Controller Definitions
; Addresses
INTCtrlrCtrl
             EQU
                  0FF32H
                                 ;address of interrupt controller for timer
INTCtrlrEOI
            EQU
                   OFF22H
                                 ;address of interrupt controller EOI register
; Register Values
INTCtrlrCVal EQU
                    00001H
                                 ;set priority for timers to 1 and enable
                                 ;0000000000000---- reserved
                                 ;----- enable timer interrupt
                                 ;-----001 timer priority
TimerEOI
             EQU
                    H80000
                                 ; Timer EOI command (same for all timers)
             EQU
                    08000Н
NonSpecEOI
                                 ; Non-specific EOI command
; Chip Select Unit Definitions
; Addresses
PACSreq
            EQU
                    OFFA4H
                                 ;address of PACS register
                                 ;address of MPCS register
MPCSreg
            EQU
                    OFFA8H
; Control Register Values
PACSval
            EQU 00003H
                                 ; PCS base at 0, 3 wait states
                                 ;0000000000----- starts at address 0
                                 ;----- reserved
                                 ;----0-- wait for RDY inputs
                                 ;-----11 3 wait states
MPCSval
             EQU
                    00183H
                                 ; PCS in I/O space, use PCS5/6, 3 wait states
                                 ;0----- reserved
                                 ;-0000001---- MCS is 8KB
                                 ;----- output PCS5/PCS6
                                 ;----- PCS in I/O space
```

;-----0-- wait for RDY inputs ;-----11 3 wait states

; Timing Definitions

COUNTS_PER_MS EQU 2304 ;number of timer counts per 1 ms (assumes 18.432 MHz clock)

MS PER SEG EQU 200 ;number of ms for each segment

; General Definitions

FIRST_RESERVED_VEC LAST_RESERVED_VEC NUM IRQ VECTORS		EQU EQU EOU	1 3 256	<pre>;reserve vectors 1-3 ;number of interrupt vectors</pre>
_ ~_ LEDDisplay	EQU	0080н		;display address
NUM_DIGITS	EQU	8		;number of digits in the display