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CS 250 Homework #4
Building a CPU
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Test / File	Working
Arithmetic	Computed correct values with given tests for addi, add, sub.
Boolean	Computed addi, nand, xor functions correctly with given tests.
Control	Performed addi, bgt, jal, beqz, and j functions correctly and passed given tests. The tests don't fully account for the **jr** instruction, but I believe my implementation should work; in my mux when I compute the address of the next PC, I set the jr instruction to compute the next PC address as the result of $rs, specified by 's' from my regFile in the main circuit.
io	Outputted correct results with given tests.
Memory	Performed lw, sw functions correctly. Passed given tests.
Shift	Both shl, shra performed as expected and passed given tests.
Register File (RegFile)	Single 16-bit registers strung together correctly. Each register is constructed from 16 D-FlipFlops. Outputs are as expected into the RegFile from main. Register Decoder correctly selects Mux output.
ALU	16-bit Adder correctly displays output. Built from a 4-bit Adder which is built from 1-bit Adders. Subtractor works. Functions like adder but flips bits and adds 1. Left Shift displays shifted result correctly. Right Shift correctly shifts bits to the right by given amount. Mux functions in accordance to the opcode.
Controller	Decodes opcodes correctly. Each output works as expected with the given instructions (i.e. jal output is 1 when the instruction opcode is 1101).
Sign Extender	Sign extends 6 bit input to 16 bits correctly.