High Speed 400MS/s 8b Digital to Analog Converter

Design of a high-speed 400MS/s 8b DAC in a 0.18µm CMOS technology

Sinan Yilmaz
PhD Candidate in Electrical Engineering
Columbia University
sy2943@columbia.edu

Jens Daci
M.S. Student in Electrical Engineering
Columbia University
jd3693@columbia.edu

***Abstract*—In this paper, the design, implementation, and testing of a high speed 400MS/s 8 bit digital to analog converter will be thoroughly discussed. The design will be implemented in a 0.18µm CMOS technology and laid out in Cadence Virtuoso. Testing of the DAC will be performed on the same software platform to verify if the design matches all of the transient, frequency, and power consumption requirements.**

***Key Terms*—**Current Steering DAC, SFDR, SNDR, DNL, INL.

I. Introduction

A digital-to-analog converter, as its name implies, converts digital inputs to analog outputs. There are many ways to implement a DAC in an electronic circuit, but the most used in the industry is implementing them in an integrated circuit. These typically take the form of metal–oxide–semiconductor (MOS) mixed-signal integrated circuit chips that integrate both analog and digital circuits.

As part of this project, it is required to design a high speed 400MS/s 8-bits digital-to-analog converter. Since most of the DACs are usually implemented in integrated circuits, the same applies to the design of this project. The circuit needs to be designed in a 0.18µm CMOS technology operating from a 1.8V supply voltage.

The DAC will take an 8-bit digital input and should provide differential outputs with up to 1.5V peak-to-peak differential output swing. In other words, the DAC should provide a 750mV per side output voltage. The differential DAC is intended to drive an off-chip differential transmission line channel with 100Ω characteristic impedance. As a result, the output of the DAC should have a 100Ω differential output resistance and a 25Ω common-mode output resistance. In addition, parasitic capacitances associated with the output bond pad and electrostatic discharge (ESD) protection devices should be taken into account. These introduce a 480fF of capacitive loading to ground at each output. Moreover, a single 100µA reference current is available for use.

Another crucial requirement of the project is the Spurious-Free Dynamic Range (SFDR) which measures the nonlinearity in the design. The SFDR is a metric that represents the ratio between the strength of the fundamental signal to the strongest spurious signal in the output. As part of this project, it is required that the SFDR should be better than 42dB across the Nyquist band. After the design has been implemented, simulations will be performed over process corners. Final metrics and graphs such as the DNL, INL, SFDR, and SNDR will be reported.

II. Architecture

There are many ways that a differential DAC can be implemented using analog components. Different types of digital-to-analog architectures can range from simple structures that are binary weighted to more complex ones that require thermometer encoding. Out of all the different types of DAC architectures available, the one used for this specific project is the Current-Steering digital-to-analog converter. The current-steering DAC replaces the resistor element in the resistor DAC architectures with a MOSFET current element and uses summation of the current elements to produce the result. A binary-weighted version of this architecture has been chosen for the project rather than the thermometer encoded one.

One of the design requirements is the use of a single reference current to derive any bias needed in the design. This type of architecture allows the use of the 100µA reference in order to scale the currents coming out of the current mirrors. Resistive or capacitive architectures might not be the best option for this design since they require the use of an amplifier at the output. Because the DAC is driving a small resistive load, it is quite difficult to have the amplifier and the load connected together at the output.

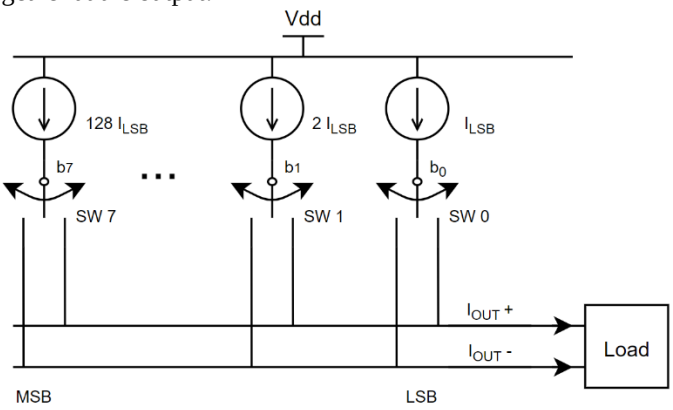

Figure 1. High-Level View of the Differential Current Steering DAC

As seen in the high-level view of the differential Current-Steering DAC depicted in Figure 1 above, the architecture would require 8 current sources, each producing a current based on their binary weight. Depending on the switch position, either the positive or negative side will have a designated current flowing through. These currents will directly feed the load impedance and produce a desired differential output swing. This topology is suited for delivering a high-performance time-continuous signals into small resistive loads.

III. Building Blocks

In the following few sections, the building blocks of the differential Current-Steering DAC will be examined. These include the analog components which are the current mirrors and the differential switches, and the digital components such as the ratioed logic latch.

A. Current Mirrors

The implementation of the current sources in the Current-Steering DAC architecture will be done using current mirrors. There are many types of current mirrors that could have been chosen for this design project, such as a simple two transistor current mirror, a cascode current mirror with 4 transistors, a Wilson current mirror, or a wide-swing current mirror. Because of the stringent requirements of this project, the latter current mirror was chosen to be the most optimal of the topology group. Such a current mirror can be seen depicted in Figure 2 below. Each unit current element will be a wide-swing current mirror that requires a bias voltage at the gate of one of the transistors. The output current will be based on the ratio between the reference transistor sizes on the left and the mirrored transistors on the right.

A wide-swing current mirror is beneficial for the design of this project since it provides a high output impedance. Because of its differential design, it is expected that the DAC will exhibit third order nonlinearities. A nonlinearity specification of the DAC can be easily converted into a current source output resistance specification. In this conversion, the amount of harmonic distortion is proportional to the ratio of the load resistance to the current source resistance, with the latter being in the denominator. Hence, a higher output impedance will reduce the nonlinearities in the design resulting in a lower INL of the overall DAC.

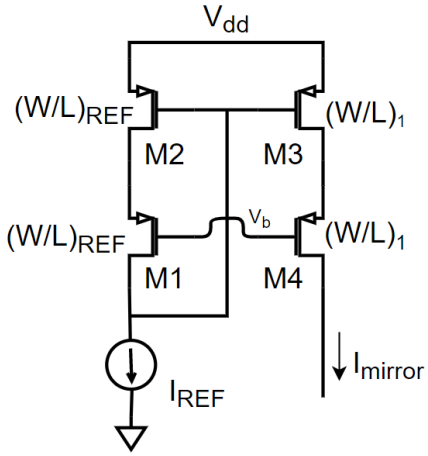

Figure 2. Wide-Swing Current Mirror

B. Differential Switches

Most digital-to-analog converters are constructed as differential circuits. The design of this digital-to-analog converter also requires for the outputs to be differential. In order to satisfy this requirement, two switches are needed at the output of the current mirror. If only one switch is used, when the current source is selected, the DAC settling time will be degraded due to the time it takes for the current source to come out of triode. An advantage of the differential switches is that it avoids this problem by steering the DAC element current into the negative side when that element is not selected. The switches that will be used in this project will be constructed using PMOS transistors as depicted in Figure 3. In the overall DAC architecture, the wide-swing current mirror together with the differential switches will be a single unit element that will be instantiated several times based on the binary weights.

These switches will either steer the current coming out of the current mirror to the positive side or the negative side depending on the digital input bit that is applied to the DAC. One of the switches will be connected to the bit itself whereas the other will be connected to its inverted value. As a result, when the bit is asserted, the right PMOS will turn on and steer the current through the positive side of the differential output. On the other hand, when the input bit is low, the left PMOS will turn on and provide a path for the current to the negative side of the output.

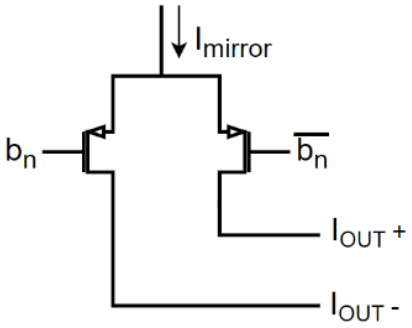

Figure 3. Differential Switches using PMOS Transistors

C. Ratioed Logic Latch

A digital block such as a ratioed logic latch is needed in the design in order to drive the differential switches. To get rid of the spikes arising during the transitions between DAC states, it is critical to have the bits switch simultaneously. The delay between bits and their inverses is inherent to the ratioed logic latch that we will use.

Figure 4. Ratioed Logic Latch Symbol showing Inputs and Outputs

D. Inverter Driver Stage

As we increase the significance of the bits, the current sources associated with the bits size up. The switches that are used to steer those currents also need to be sized accordingly so that they can support the higher current levels. The transistors in the ratioed logic latch that are driving those sized switches are also increasing in size as we move towards the MSB. In order to have equal delay on each bit path, an inverter driver stage is designed as the entry block of the DAC. This stage includes eight inverter chains to drive the ratioed logic latches dedicated for each bit and another chain to drive the clock line.

IV. DAC Design

In this section, a more in-depth view of each of the building blocks of the Current-Steering DAC will be analyzed. Transistor sizes, current calculations and design considerations for each block will be explained.

A. Current Mirrors

Before starting the transistor design of the current mirror, the first step was to pick the length of the transistors and use that length to size the widths based on the ratios and areas needed. It was decided that the length of all the transistors would match the technology that the DAC will be designed in, meaning a length of 180nm. Then, one of the first calculations that is performed is the Least-Significant-Bit (LSB) current. Considering single sided output voltage of 750mV, the load and the resolution of the DAC, the current can be calculated as follows:

$$I_{LSB} = \frac{750mV}{(2^8-1)*25\Omega} = 117.65\ \mu A \qquad (1)$$

Based on the LSB current calculation and the known reference current that can be used in the design, the current mirror ratio for the LSB can be calculated in the following way:

$$\frac{(W/L)}{(W/L)_{REF}} = \frac{I_{LSB}}{I_{REF}} = \frac{117.65\ \mu A}{100\ \mu A} = 1.1765 \qquad (2)$$

Next, the sizing of the reference branch was based on simulations of the output current from a single current mirror by choosing scenarios that mimicked the DAC. The first iteration of the current mirror did not include the bias voltage as it was just a simple cascode version. The mismatch calculations provided a limit to the gate area of the transistors used in the design. In order to achieve a small mismatch of 7% in the drain current, a minimum gate area can be calculated as follows:

$$\frac{\sigma^2(\Delta I_d)}{I_d^2} = \frac{1}{WL}\left[\frac{4*A_{VT}^2}{(V_{GS}-V_T)^2} + A_\beta^2\right]$$

$$\left(\frac{7}{100}\right)^2 = \frac{1}{WL}\left[\frac{4*(5mV*\mu m)^2}{(500mV)^2} + (0.01\mu m)^2\right]$$

$$WL = 1.647(\mu m)^2 \quad L = 0.18\mu m \quad W = 9.15\mu m \qquad (3)$$

The ultimate goal of the design is to keep all transistors in the saturation region even though the output of the DAC changes. Increasing the size of these active devices allowed us to reduce the Vgs drop across those transistors, hence there is no node voltage that is below 0. However, it was challenging to keep all of the active devices in saturation while maintaining a relatively small width with just a simple cascode design.

As a result, a wide-swing current mirror would solve the issue. Usage of the wide-swing current mirror, such as the one in Figure 2, allowed us to reduce the size of the reference branch transistors while keeping all the DAC mirror transistors in saturation. The reference branch transistors were sized with widths of 10µm. The optimal bias voltage was determined to be 700mV and was produced by a simple resistive divider from the supply voltage to ground. The resistors chosen for this implementation are:

$$R_1 = 2\ k\Omega \text{ and } R_2 = \frac{2k\Omega - (1.4k/1.8V)}{0.7/1.8V} = 3.142\ k\Omega \qquad (4)$$

On the other hand, the transistors on the mirrored branch were sized based on the current ratios determined in equation (2). After sizing the transistors in the mirrored branch in this form, it was observed that the current mirror was not producing the desired current based purely on the ratio. Therefore, after simulations, some adjustments were needed to be made to the theoretical ratio in order to achieve the desired LSB current, from the LSB branch, as depicted in equation (1). The new ratio was determined to be higher than the theoretical one and the mirrored LSB branch was sized as follows:

$$W_{REF} = 10\ \mu m \qquad (5)$$

$$W_{LSB\ branch} = W_{REF} * ratio = 10\mu m * 1.244 = 12.44\ \mu m$$

As seen in the figure below, after the sizing of the LSB branch, all the other branches were binary weighted multiples of the first. On Cadence, this was realized based on a multi-finger layout by providing a binary weighted number of instances for each unit element. Since we have an 8-bit DAC, the largest size pertains to the MSB with 128 instances of a unit element.

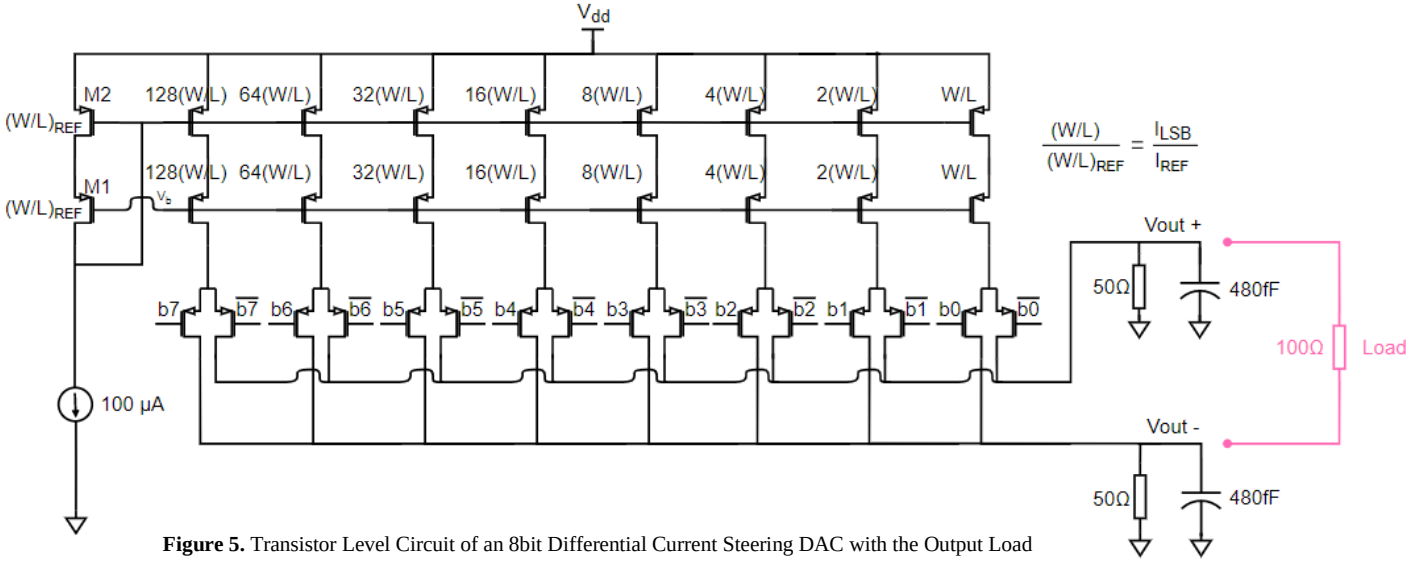

Figure 5. Transistor Level Circuit of an 8bit Differential Current Steering DAC with the Output Load

B. Differential Switches

The differential switches underneath the current mirrors were sized based on the output currents resulting from the corresponding current mirrors that they enabled. One of the hidden requirements of every CMOS design is to keep the area as small as possible without trading off a considerable amount of performance or higher power consumption. The only requirement that we have for the switch transistors is that they need to support the current levels supplied by the DAC mirror transistors.

A challenging problem with the differential switches was the headroom issue when the output voltage of the DAC comes near its high values. This is especially a big issue when the current level increases more than 10 mA when we get close to the most significant bits. As with the design of the current mirror, the final goal was to keep the switch transistors in the saturation region even though the output of the DAC changes. As a result, the sizing of the differential switch transistors for the LSB branch was optimized after a series of simulations and parametric sweeps to be the following:

$$W_{SW+} = W_{SW-} = 5\ \mu m \tag{6}$$

Based on the simulations performed, a switch width of 5µm ensured that none of the transistors would leave the saturation region even though the DAC reached a high output voltage. The sizing of the transistors for the other branches was also based on a multi-finger layout. On Cadence, to facilitate the layout of the circuit, the wide-swing current mirror together with the differential switches was thought of as a single unit element that was instantiated several times based on the binary weights of each branch.

C. Ratioed Logic Latch

The sizing of the ratioed logic latch is critical for the performance of the DAC. Its driving transistors need to be sized big enough to drive the switches, but not bigger than needed so that the inverter driver stage coming before can drive its input gates. Also, the ratio between the PMOS and NMOS transistors inside the stage need to be sized to achieve an intended but not too long delay between two transitions. In order to minimize the delay, pull-down (NMOS) network of the ratioed logic latch is stronger than the pull-up (PMOS) network.

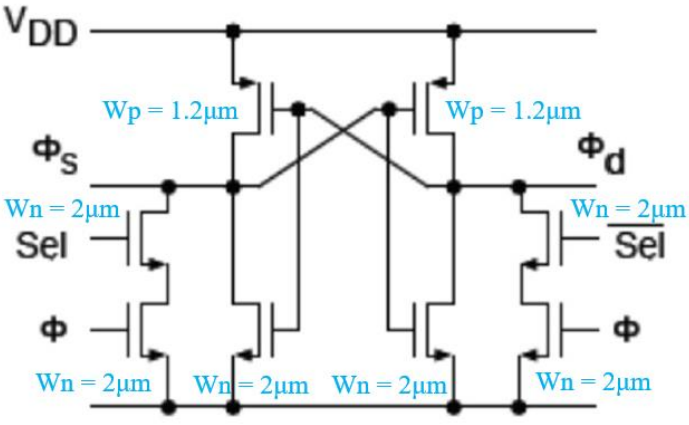

Figure 6. Circuit Implementation of the Ratioed Logic Latch

D. Inverter Driver Stage

As described in Section III, the inverter driver stage has nine bus lines in total, one of which belongs to the clock and other eight is used for bit transmission. The clock line's output capacitance is determined by the sizes of the NMOSes in the ratioed logic latches. In total, this line will drive 255*2 unit NMOS transistors. The input capacitance of the equivalent inverter of the first stage is given in our specifications, 1080 nm. Based on these values, we optimized the number of stages to be 5 and stage gain to be 3.94 which is very close to FO4 delay.

All eight-bit lines need to drive transistors with different widths and wide range of output capacitances. Each line requires optimization for the number of stages and their stage gains while trying to attain close to equal delay on each one of them. This optimization allows us to determine the trade-off between delay and the area of the DAC based on the output and input capacitances. Additionally, number of stages need to be even number so that our output is not an inverted version of the input sinusoidal. Below is a summary of each bit line's theoretically optimized number of stages and their respective stage gains:

Bits	Output Cap.	# of Stages	Stage Gain
B0	5.2 µm	2	2.19
B1	10.4 µm	2	3.1
B2	20.8 µm	2	4.38
B3	41.6 µm	4	2.49
B4	83.2 µm	4	2.96
B5	166.4 µm	4	3.52
B6	332.8 µm	6	2.6
B7	665.6 µm	6	2.92

Table 1. Theoretical Stage Gain Calculations for Eight Bit Lines

In our design, we took these values as our basis and arranged these values to strive for equal delays in each line while achieving our main specification, that is SFDR of 42 dB.

E. Output Differential Load

The differential DAC is intended to drive an off-chip differential transmission line channel with 100 Ω characteristic impedance. In the case when we used a single 100 Ω load, our single sided outputs were swinging between 330 mV and 1.08 V instead of 0 and 750 mV due to the loading effect. The loading effect happens in the case where one side of the output voltage increases too high as to drive the differential switch transistors out of the saturation region. As a result, we used two different 50 Ω resistors, instead of a single 100 Ω resistor as load, to get a better case for the headroom scenario. This allowed us to keep all of our switch transistors in saturation even when the output peaked.

F. Operation in One Clock Cycle

During the high period of the true phase of the clock ("$clock\_t$"), the input bits traverse through the inverter driver stage and reaches to the ratioed logic latch. Ratioed logic latches' clock is 180° shifted, referred to as "$clock\_s$". Within

the high period of the *clock_s*, ratioed logic gate takes in the bits driven by the inverter driver stage and gives out the bits with two opposite polarities. The differential inputs are given to the eight branches of the DAC that steer the current into the desired path. The resulting current is then converted into voltage thanks to the differential load. This operation is completed within one clock cycle of the true phase.

V. DAC Simulation

The performance of the DAC will be characterized based on its static and dynamic performance. Simulations were performed over process corners on Cadence and the results are presented in the next few sections. All graphs are based on tt process corners.

A. Static Performance

The static performance of the differential DAC can be examined by the differential nonlinearity (DNL) and the integral nonlinearity (INL). In order to simulate the DNL and the INL of the DAC, a ramp function should be produced at the output of the DAC. To have such a function at the output, square wave signals with different periods and delays are going to be used as inputs to the designed DAC, as shown in the testbench figure below. The periods and delays of these signals are chosen such that the output voltage of the DAC has time to settle. As a result, samples are taken in the middle of these settled voltages.

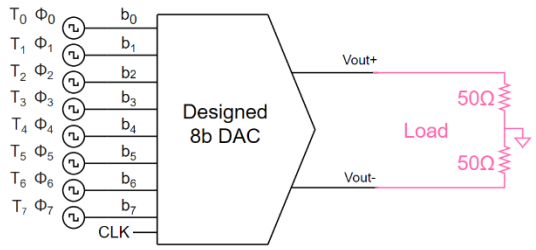

Figure 7. DNL and INL Testbench Setup

The DAC produced a stair-step function with voltages that ranged from the minimum of -750mV to the maximum of 750mV. The graph depicted in Figure 8 shows this type of function plotted on Cadence. On the other hand, the MATLAB plot presented in Figure 9 shows the ramp function based on the samples taken. We need to correct for the offset and full-scale errors, before we measure the DNL and INL, by calculating the effective V_{LSB} as follows.

$$V_{LSB,actual} = \frac{V_{1\ldots1} - V_{0\ldots0}}{2^N - 1} = 5.894\ mV$$

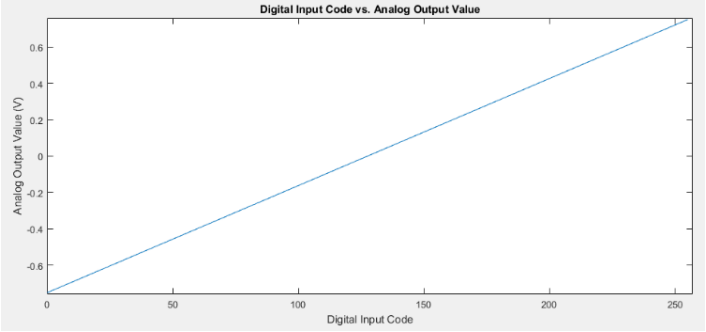

Figure 8. Ramp Function Based on Samples Taken (MATLAB)

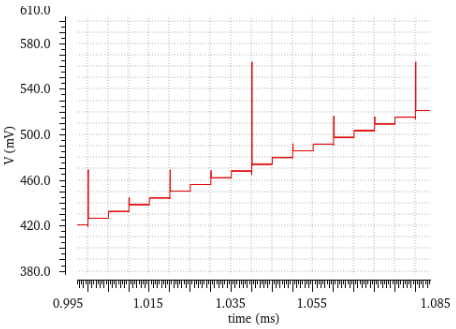

Figure 9. Stair-Step Function Produced at the DAC Output (Cadence)

1) DNL

The first metric that will be calculated is the differential nonlinearity (DNL) of the DAC. The following figure shows the DNL of the designed DAC plotted in terms of the input code. Based on the minimum and maximum DNLs listed in the title, we can conclude that the DAC is monotonic.

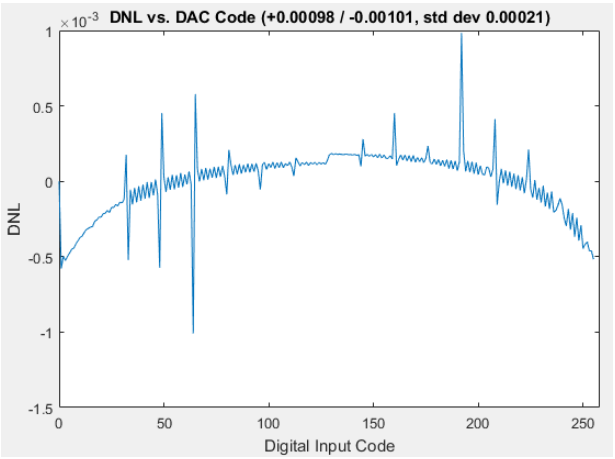

Figure 10. DNL vs. DAC Code

2) INL

As seen in the plot of Figure 11, the INL has a shape of a 3rd order function which is expected since the design is differential. Moreover, the value of the output resistance of the current mirror impacts the INL of the current DAC. Since a wide-swing-current-mirror is used, with a large output resistance, we are getting low INL values.

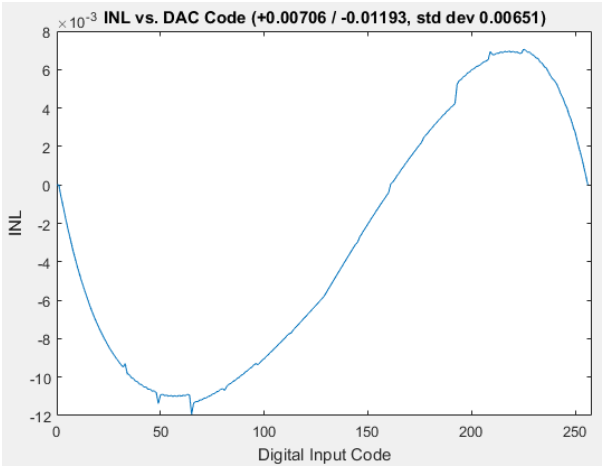

Figure 11. INL vs. DAC Code

B. *Dynamic Performance*

The performance of the DAC will also be characterized based on its dynamic performance. The spurious-free dynamic range (SFDR) and the signal-to-noise and distortion ratio (SNDR) metrics will be plotted based on the input frequency. In addition, the effective number of bits (ENOB) for the differential DAC design will also be reported. The following figure shows the dynamic performance testbench setup for the DAC.

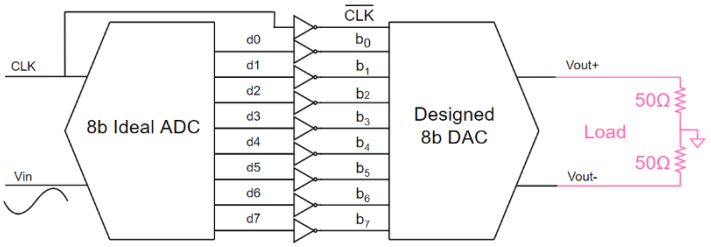

Figure 12. Dynamic Performance Testbench Setup

A transient simulation of the above testbench was run to characterize the dynamic performance of the DAC. In order to get the spectrum plot of the results, the data was converted using a Discrete Fourier Transform. When looking at the spectrum of a DAC, it is important that the sampling rate of the DFT should be much higher than the DAC sampling rate. This is especially mandatory when the DAC is usually used in applications where its output is continuous time which is the case for this design. The DFT sampling rate that was decided for this project depends on several parameters and can be found as follows:

$$f_{s,DFT} = pts/symbol * f_{s,DAC} = 1024 * f_{s,DAC}$$

There are a few obstacles when running a DFT simulation. One of the challenges is that not any value for the input frequency would result in proper transforming of the data. An integer ratio of the sampling clock frequency to the input frequency would result in undesired and highly deterministic time-domain samples. As a result, the ratio of the sampling clock to the input frequency must be irrational to avoid deterministic quantization noise. Moreover, another challenge of a DFT simulation is to not get spectral leakage at the output spectrum. To avoid this issue, it is crucial that the input waveform is repetitive. A solution to both of these difficulties would arise from a simple input signal function where the parameters must be chosen carefully. The sinusoidal function can be written as:

$$y(t) = A * cos(2\pi * f_s * \frac{J}{M} t)$$

In this function, A represents the signal amplitude, and f_s represents the DAC sampling rate. The variable M represents the number of samples to be processed by the data converter which should be a power of 2. The variable J represents the number of sinusoidal cycles. If M is chosen as a power of 2, then any odd value for J will satisfy the relatively prime condition. The value of J is swept depending on the desired input frequency, whereas the value of M is set to 2048.

The following figure shows a successful DFT simulation where the highest power is present at the frequency of the input and some distortion power at different frequencies can also be seen. The spectrum was simulated for a value of $J = 113$.

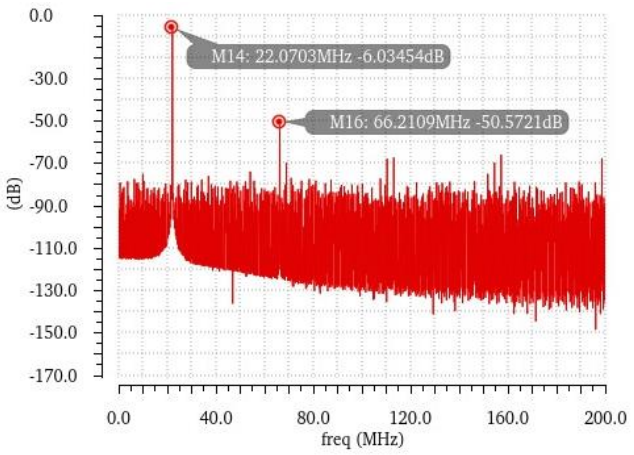

Figure 13. DFT Spectrum Results (Input Frequency = 22.1 MHz)

One of the requirements of the project is to achieve an SFDR of better than 42dB across the Nyquist band. As a result, ten different values for the variable J was chosen to plot the DFT spectrum of the differential DAC. Since the high frequency quantization noise will be attenuated by the Zero-Order Hold, the values computed by the Cadence functions will not be correct. As a result, the DFT spectrum for every single input frequency was extracted as a table of values and analyzed in MATLAB to produce the correct SFDR, SNDR, and ENOB values. The following plots show these converter metrics as a function of the variable J (function of the input frequency).

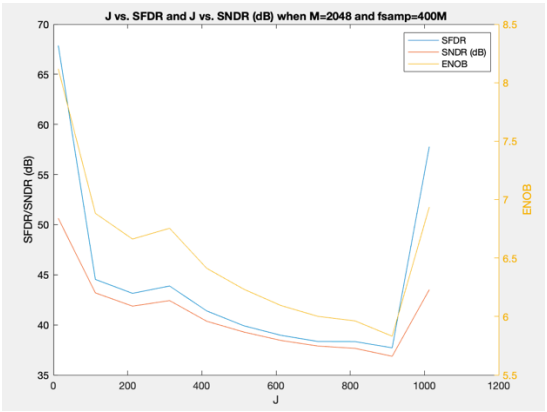

Figure 14. SFDR, SNDR and ENOB plot with our Inverter Driver Stage

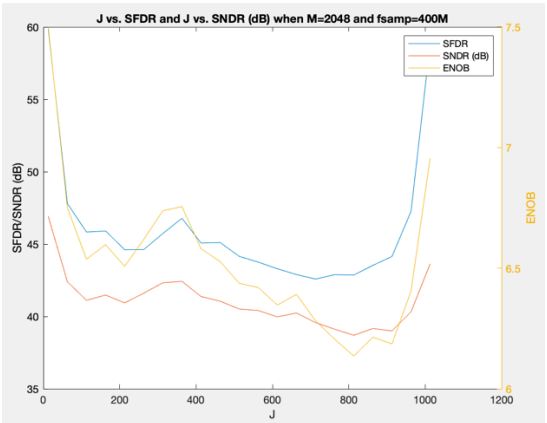

Figure 15. SFDR, SNDR and ENOB plot with ideal D Flip-Flop Driver

C. DAC Performance Summary

The summary of the performance of the DAC is divided into two tables. The first table deals with the static performance, whereas the second table deals with the dynamic performance. The values show the results simulated for all process corners.

Metrics (in LSBs)	Process Corners		
	typical/typical	slow/slow	fast/fast
$(DNL)_{min}$	-0.00101	-0.00085	-0.00117
$(DNL)_{max}$	+0.00098	+0.00125	+0.00060
$\sigma(DNL)$	0.00021	0.00028	0.00040
$(INL)_{min}$	-0.01193	-0.01181	-0.01408
$(INL)_{max}$	+0.00706	+0.00881	+0.01401
$\sigma(INL)$	0.00651	0.00729	0.00977

Table 2. Static Performance Summary

Metrics	Process Corners		
	typical/typical	slow/slow	fast/fast
$SFDR\ @\ LF$	67.87 dB	67.45 dB	61.24 dB
$SFDR\ @\ HF$	57.78 dB	54.61 dB	60.12 dB
$Peak\ SFDR$	67.87 dB	67.45 dB	61.24 dB
$SNDR\ @\ LF$	50.63 dB	50.64 dB	50.46 dB
$SNDR\ @\ HF$	43.51 dB	42.14 dB	44.80 dB
$ENOB\ @\ LF$	8.11 bits	8.12 bits	8.09 bits
$ENOB\ @\ HF$	6.94 bits	6.71 bits	7.15 bits

Table 3. Dynamic Performance (LF=2.54 MHz and HF=197.85 MHz)

Based on the results shown above, the differential DAC is working correctly and satisfying all the requirements in the low frequency inputs. However, as seen in Figure 14, the converter metrics start to degrade at higher frequencies. At the middle frequencies, the spectrum results show a lower than 42 dB of SFDR, but still very close to matching the requirements.

The results obtained with our Inverter Driver Stage, plotted in Figure 14, can be compared with the results obtained with the ideal D-Flip-Flop drivers, plotted in Figure 15. One can see that, with the ideal drivers, the SFDR is better than 42 dB across the Nyquist band. Moreover, the SNDR and the ENOB show much better results in this comparison.

Based on this analysis, it can be concluded that the circuit block that is mostly limiting our design is the inverter driver stage. This circuit block adds a considerable amount of delay between the inputs to the DAC and the inputs to the PMOS switches. As a result, these delays can cause distortion in the output voltage which results in worse converter metrics such as SFDR, SNDR, and ENOB.

VI. Power Dissipation and Area

The break down of the power dissipation and the area for each circuit block can be seen in the next few sections. A table summarizing these values is presented at the end.

A. Current Mirror

$$Power = [255 * 117\mu A] * 1.8V = 53.7\ mW$$

$$Area = [2 * 10 + 255 * (2 * 12.44)] * 0.18\mu m = 1145\mu m^2$$

B. Differential Switches

$$Area = [255 * (2 * 5\mu m)] * 0.18\mu m = 459\mu m^2$$

C. Ratioed Logic Latch

$$Power = \frac{1}{T}\int (I * V)\, dt = 3.1\ mW$$

$$Area = [255 * (6 * 2 + 2 * 1.2)] * 0.18\mu m = 660\mu m^2$$

D. Inverter Driver Stage

$$Power = \frac{1}{T}\int (I * V)\, dt = 0.5\ mW$$

$$Area = [(0.72\mu m + 0.36\mu m) * 1515] * 0.18\mu m = 295\mu m^2$$

The following calculation represents the Figure of Merit for the differential DAC design. The one used in this report will be the inverse Walden FoM.

$$FoM = \frac{Power}{f_s * 2^{ENOB}} = \frac{57.3\ mW}{400\ MHz * 2^{6.94}} = 1.167pJ/conv\ step$$

DAC Architecture	Current Steering DAC
Technology Node	0.18µm CMOS
Resolution	8 bits
Power	$57.3\ mW$
Area	$2559\ \mu m^2$
Walden FoM @ Nyquist	$1.167pJ/conv\ step$

Table 4. Power and Area Summary

VII. Conclusion

In conclusion, the report presented the design of a High Speed 400MS/s 8b Digital to Analog Converter in a 0.18µm CMOS technology. The differential Current Steering DAC included analog and digital blocks in its design. The simulations were performed over process corners and they showed the successful operation of the overall DAC. Most of the requirements explained at the beginning of the report were satisfied with relatively small power consumption and area.