FIR Core
Design Project Metrics

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Project Metrics

- **Input:** Randomly generated 10k 16-bit real-valued numbers
- **Throughput:** Prime-Time report with design compiler generated sdf annotation
- **Maximum Clock Frequency:** Prime-Time report with design compiler generated. sdf annotation
- **Power Analysis:** Prime-Time report
- **Energy Efficiency:** Prime-Time report with the design compiler generated .sdf and QuestaSim generated .vcd annotations
- **Area:** Design Compiler generated report
- **Accuracy:** RMSE against MATLAB results in 32-bit floating point numbers. Inputs are 16-bit and generated by the random function of MATLAB.

Area

An area analysis was conducted to show that the area metrics are matched. The total cell area is the physical space occupied by the core and would estimate how big the chip would need to be in order to be manufactured. The report from Figure 9 is listed below:

$$Combinational\ Area = 18{,}730.08\ mm^2$$
$$Buffer\ and\ Inverter\ Area = 3{,}631.68\ mm^2$$
$$Noncombinational\ Area = 2{,}190.24\ mm^2$$

By combining all these values, the total cell area would be:

$$Total\ Cell\ Area = 20{,}920.32\ mm^2$$

Area

Open | fir.dc.rpt ~/Desktop/Project/dc/fir | Save

```
****************************************
Report : area
Design : fir
Version: O-2018.06-SP5-1
Date   : Mon Dec 14 23:18:19 2020
****************************************

Library(s) Used:

    scx3_cmos8rf_lpvt_tt_1p2v_25c (File: /courses/ee6321/share/
ibm13rflpvt/synopsys/scx3_cmos8rf_lpvt_tt_1p2v_25c.db)

Number of ports:                         1247
Number of nets:                          4736
Number of cells:                         2491
Number of combinational cells:           2326
Number of sequential cells:               154
Number of macros/black boxes:               0
Number of buf/inv:                        673
Number of references:                      35

Combinational area:              18730.080454
Buf/Inv area:                     3631.680137
Noncombinational area:            2190.239960
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 20920.320414
Total area:                 undefined

Information: This design contains black box (unknown) components.
(RPT-8)
```

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Fig 9. Area Report from the Design Compiler

Timing

A timing analysis was conducted to show that the timing metrics were matched. In it, we display the critical path delay and the minimum path delay. Based on Figure 12 and Figure 13 the delays are as follows:

$$Minimum\ Path\ Delay = 0.2090\ ns$$

$$Critical\ Path\ Delay = 9.4361\ ns$$

Timing

(Minimum Path Delay)

Open ▾ fir_pt.rpt ~/Desktop/Project/pt/fir Save

```
Startpoint: s (input port clocked by clk)
Endpoint: presentState_reg_0_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.0000     0.0000
clock network delay (ideal)                             0.0000     0.0000
input external delay                                    0.0500     0.0500 r
s (in)                                                  0.0379     0.0879 r
U1126/Y (OAI21XLTS)                                     0.1211     0.2090 f
presentState_reg_0_/D (DFFTRX1TS)                       0.0000     0.2090 f
data arrival time                                                  0.2090

clock clk (rise edge)                                   0.0000     0.0000
clock network delay (ideal)                             0.0000     0.0000
clock reconvergence pessimism                           0.0000     0.0000
presentState_reg_0_/CK (DFFTRX1TS)                                 0.0000 r
library hold time                                      -0.0414    -0.0414
data required time                                                -0.0414
-----------------------------------------------------------------------------
data required time                                                -0.0414
data arrival time                                                 -0.2090
-----------------------------------------------------------------------------
slack (MET)                                                        0.2504
```

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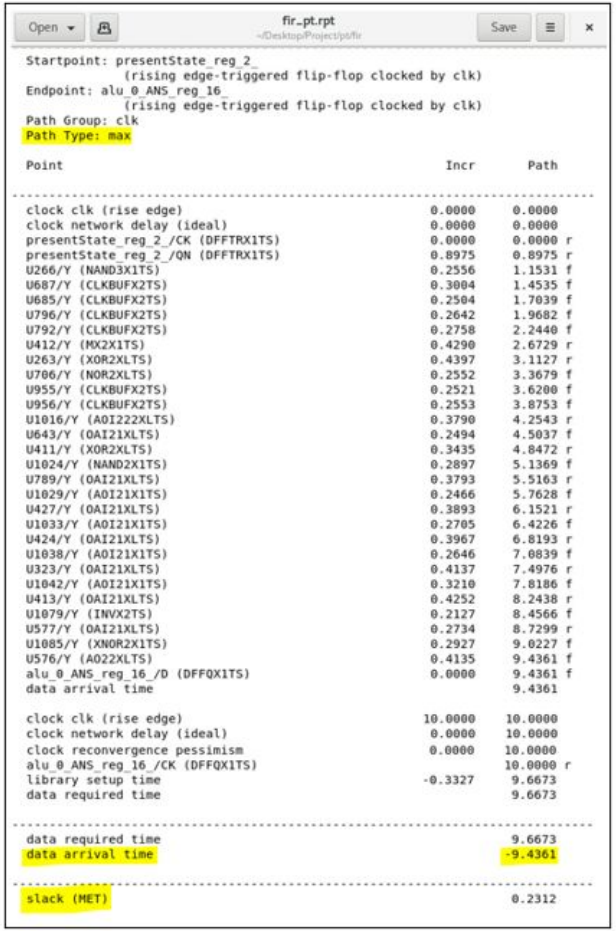
Fig 12. Shortest Path Delay

Timing

(Critical Path Delay)



fir_pt.rpt
~/Desktop/Project/pt/fir

```
Startpoint: presentState_reg_2_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: alu_0_ANS_reg_16_
            (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.0000     0.0000
clock network delay (ideal)                             0.0000     0.0000
presentState_reg_2_/CK (DFFTRX1TS)                      0.0000     0.0000 r
presentState_reg_2_/QN (DFFTRX1TS)                      0.8975     0.8975 r
U266/Y (NAND3X1TS)                                      0.2556     1.1531 f
U687/Y (CLKBUFX2TS)                                     0.3004     1.4535 f
U685/Y (CLKBUFX2TS)                                     0.2504     1.7039 f
U796/Y (CLKBUFX2TS)                                     0.2642     1.9682 f
U792/Y (CLKBUFX2TS)                                     0.2758     2.2440 f
U412/Y (MX2X1TS)                                        0.4290     2.6729 r
U263/Y (XOR2XLTS)                                       0.4397     3.1127 r
U706/Y (NOR2XLTS)                                       0.2552     3.3679 f
U955/Y (CLKBUFX2TS)                                     0.2521     3.6200 f
U956/Y (CLKBUFX2TS)                                     0.2553     3.8753 f
U1016/Y (AOI222XLTS)                                    0.3790     4.2543 r
U643/Y (OAI21XLTS)                                      0.2494     4.5037 f
U411/Y (XOR2XLTS)                                       0.3435     4.8472 r
U1024/Y (NAND2X1TS)                                     0.2897     5.1369 f
U789/Y (OAI21XLTS)                                      0.3793     5.5163 r
U1029/Y (AOI21X1TS)                                     0.2466     5.7628 f
U427/Y (OAI21XLTS)                                      0.3893     6.1521 r
U1033/Y (AOI21X1TS)                                     0.2705     6.4226 f
U424/Y (OAI21XLTS)                                      0.3967     6.8193 r
U1038/Y (AOI21X1TS)                                     0.2646     7.0839 f
U323/Y (OAI21XLTS)                                      0.4137     7.4976 r
U1042/Y (AOI21X1TS)                                     0.3210     7.8186 f
U413/Y (OAI21XLTS)                                      0.4252     8.2438 r
U1079/Y (INVX2TS)                                       0.2127     8.4566 f
U577/Y (OAI21XLTS)                                      0.2734     8.7299 r
U1085/Y (XNOR2X1TS)                                     0.2927     9.0227 f
U576/Y (AO22XLTS)                                       0.4135     9.4361 f
alu_0_ANS_reg_16_/D (DFFQX1TS)                          0.0000     9.4361 f
data arrival time                                                  9.4361

clock clk (rise edge)                                  10.0000    10.0000
clock network delay (ideal)                             0.0000    10.0000
clock reconvergence pessimism                           0.0000    10.0000
alu_0_ANS_reg_16_/CK (DFFQX1TS)                                   10.0000 r
library setup time                                     -0.3327     9.6673
data required time                                                 9.6673

-----------------------------------------------------------------------------
data required time                                                 9.6673
data arrival time                                                 -9.4361
-----------------------------------------------------------------------------
slack (MET)                                                        0.2312
```

Fig 13. Critical Path Delay

Clock Frequencies

The clock frequency is what determines how fast our circuit operates and is an important parameter when considering the FIR core. We use this frequency to calculate the throughput of our design. The throughput calculation is handled in the next section. Based on the testbench, the half clock period is the following:

$$T_{half} = 5\ ns$$

As a result, the clock period can be calculated as:

$$T = 2 \times T_{half} = 10\ ns$$

We can calculate the frequency of our clock by using the following equation and by plugging in our period:

$$frequency = \frac{1}{T} = \frac{1}{10\ ns} = \frac{1}{10 \times 10^{-9}} = 100\ MHz$$

The maximum frequency is calculated as follows:

$$F_{max} = \frac{1}{T_{min}} = \frac{1}{critical\ path\ delay + t_{su} + t_{cq}}$$

$$= \frac{1}{9.4361\ ns} = 105.98\ MHz$$

Throughput

A throughput analysis was conducted to show that the throughput metrics were matched. Based on the maximum clock frequency from Part C, the throughput can be calculated using the formula below:

$$Throughput = F_{max} \times 16\ bits = 1.696\ Gbits/s$$

Accuracy

An accuracy analysis was conducted to show that the accuracy metrics were matched. An equation is given in the project parameters for how we can calculate the accuracy. The Normalized Root Mean Squared Error (NRMSE) equation is as follows:

$$NRMSE = \frac{RMSE}{y_{max} - y_{min}}$$

Where the equation for RMSE is as follows:

$$\sqrt{\frac{\sum_{i=0}^{n}(y_i - y_i^*)}{n}}$$

Where y_i is your full precision MATLAB result and y_i^* is the quantized result from your RTL simulation. Since our outputs were unable to show in our waveform, we are not able to calculate the accuracy. However, we expect a very high accuracy compared to the golden outputs produced by the MATLAB.

Power

The Total Power is the combination of the Net Switching Power, Cell Internal Power and Cell Leakage Power. The black-box power is also included in the calculations. The values for these metrics are as follows:

$$Net\ Switching\ Power = 3.938 \times 10^{-5}\ W$$

$$Cell\ Internal\ Power = 1.936 \times 10^{-4}\ W$$

$$Cell\ Leakage\ Power = 2.179 \times 10^{-8}\ W$$

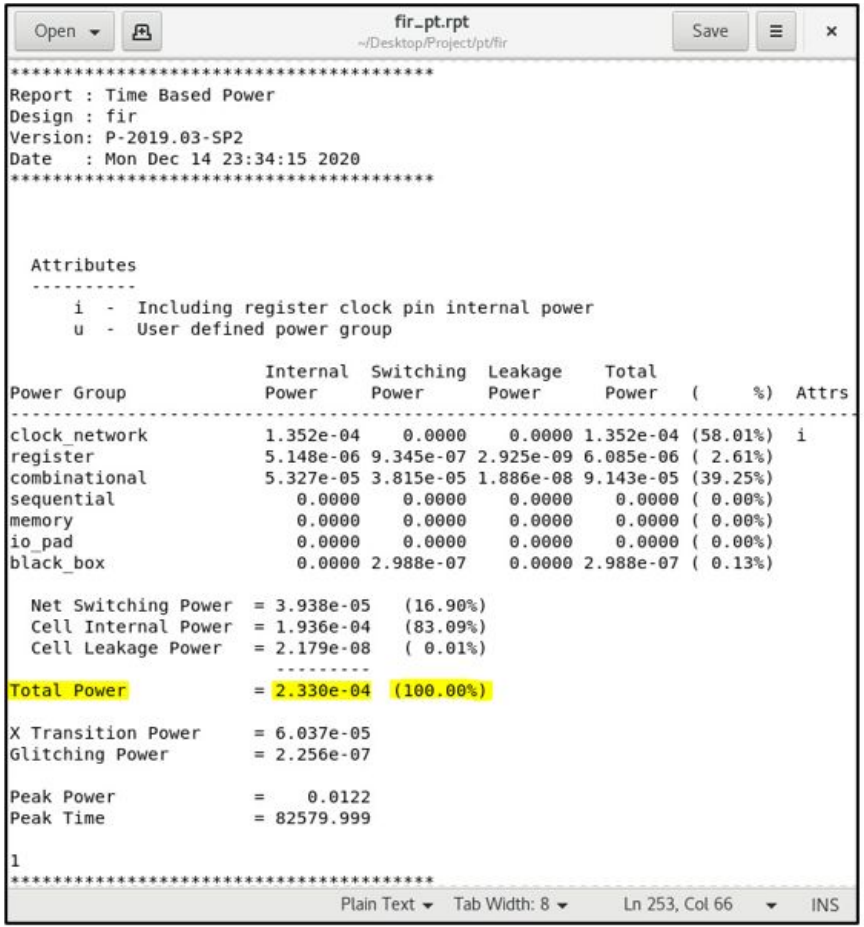
By combining all of these values, shown also in Figure 14, the Total Power is the following:

$$Total\ Power = 2.330 \times 10^{-4} = 0.233 \times 10^{-3}$$

$$Total\ Power = 0.233\ mW$$

Power

(Time Based Power)




```
****************************************
Report : Time Based Power
Design : fir
Version: P-2019.03-SP2
Date   : Mon Dec 14 23:34:15 2020
****************************************



  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
------------------------------------------------------------------------------
clock_network             1.352e-04    0.0000    0.0000 1.352e-04 (58.01%)  i
register                  5.148e-06 9.345e-07 2.925e-09 6.085e-06 ( 2.61%)
combinational             5.327e-05 3.815e-05 1.886e-08 9.143e-05 (39.25%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                    0.0000 2.988e-07    0.0000 2.988e-07 ( 0.13%)

  Net Switching Power  = 3.938e-05   (16.90%)
  Cell Internal Power  = 1.936e-04   (83.09%)
  Cell Leakage Power   = 2.179e-08   ( 0.01%)
                         ---------
Total Power            = 2.330e-04  (100.00%)

X Transition Power     = 6.037e-05
Glitching Power        = 2.256e-07

Peak Power             =    0.0122
Peak Time              = 82579.999

1
****************************************
```


Fig 14. Time Based Power Report

Power

(Hierarchical Time Based Power)

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```
****************************************
Report : Time Based Power
        -hierarchy
Design : fir
Version: P-2019.03-SP2
Date   : Mon Dec 14 23:34:15 2020
****************************************


                                    Int      Switch   Leak     Total
Hierarchy                           Power    Power    Power    Power    %
-------------------------------------------------------------------------------
fir                                 1.94e-04 3.94e-05 2.18e-08 2.33e-04 100.0
  imem_0 (imem)                     3.27e-06 1.53e-06 7.90e-09 4.81e-06   2.1
    mux_1__mux (mux_16_1_2)         5.27e-07 1.98e-07 1.62e-09 7.26e-07   0.3
    mux_0__mux (mux_16_1_3)         5.19e-07 1.95e-07 1.63e-09 7.15e-07   0.3
    mux_3__mux (mux_16_1_0)         5.31e-07 1.92e-07 1.60e-09 7.26e-07   0.3
    mux_2__mux (mux_16_1_1)         5.27e-07 1.91e-07 1.60e-09 7.19e-07   0.3
  cmem_0 (cmem)                        0.000 5.95e-10    0.000 5.95e-10   0.0


                                    Peak     Peak            Glitch   X-tran
Hierarchy                           Power    Time            Power    Power
-------------------------------------------------------------------------------
fir                                 1.22e-02 82579.999-82580.000
                                                             2.26e-07 6.04e-05
  imem_0 (imem)                     3.04e-03 55085.999-55086.000
                                                             3.47e-11 8.02e-08
    mux_1__mux (mux_16_1_2)         7.44e-04 23701.302-23701.303
                                                                0.000 1.27e-08
    mux_0__mux (mux_16_1_3)         5.82e-04 33941.458-33941.459
                                                                0.000 7.68e-09
    mux_3__mux (mux_16_1_0)         7.44e-04 23701.302-23701.303
                                                                0.000 2.27e-08
    mux_2__mux (mux_16_1_1)         7.44e-04 23701.302-23701.303
                                                                0.000 1.77e-08
  cmem_0 (cmem)                     9.12e-04 146.000-146.001    0.000 1.66e-11
1
```

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Fig 15. Hierarchical Time-Based Power Report

Energy Efficiency

An energy efficiency analysis was conducted to show that the energy efficiency metrics were matched. The calculation for the energy can be seen in the formula below:

$$Energy = Power\ Consumed \times Critical\ Path\ Delay$$

$$= 0.233 \times 10^{-3} \times 9.4361 \times 10^{-9}$$

$$Energy = 2.199\ pJ/S$$