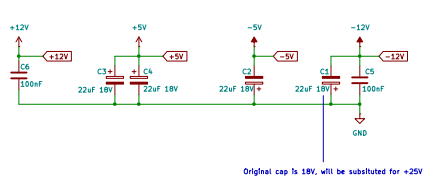
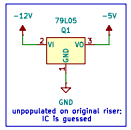


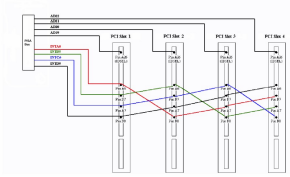


4.4 Interrupt-Routing

Following Interrupt routing on the backplane is recommended for proper bios support:

Backplane Slot	PISA INT A	PISA INT B	PISA INT C	PISA INT D
Slot 1 (AD19)	INT A	INT B	INT C	INT D
Slot 2 (AD20)	INT B	INT A	INT B	INT C
Slot 3 (AD21)	INT C	INT D	INT A	INT B
Slot 4 (AD22)	INT B	INT C	INT D	INT A

e.g. INT B signal of PCI-Slot 3 (IDSEL AD21) has to be routed to signal INT D of the PISA board



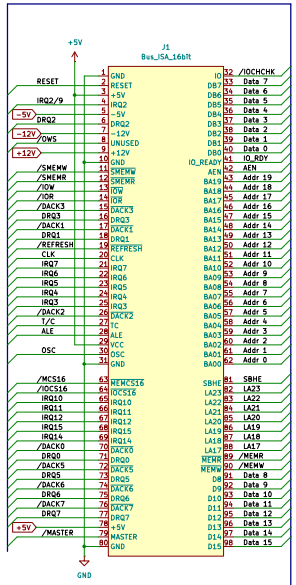
Original riser is mapped to an undocumented slot:
AD17:
PISA INT A–> PCI C
PISA INT B–> PCI A
PISA INT C–> PCI D
PISA INT D–> PCI B

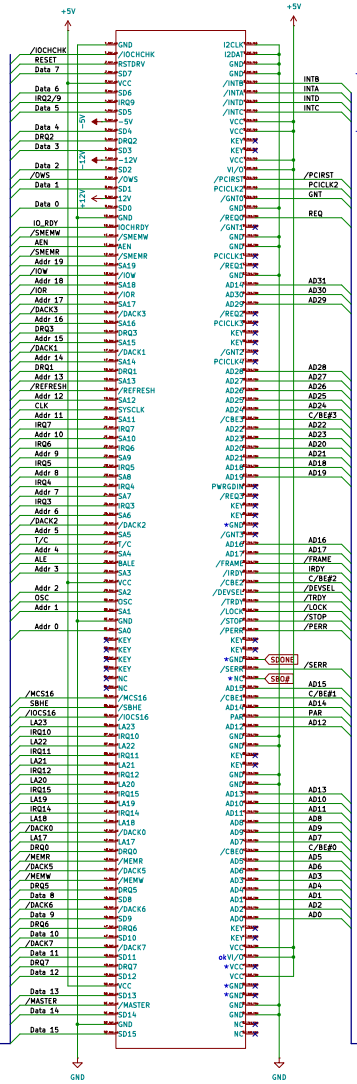
4.2 IDSEL mapping

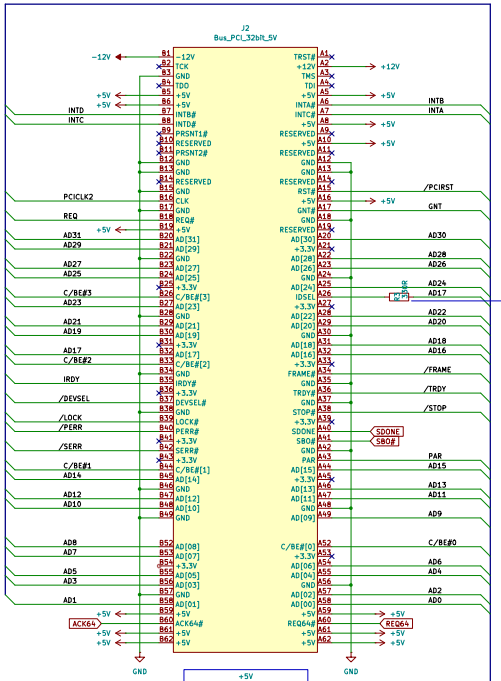
The table below shows the implementation of the necessary IDSEL routings on the CPU board and the backplane.

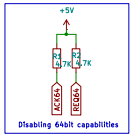
target-device	AD line	Description
0	AD11	PISA CPU chipset internal device
1	AD12	PISA CPU chipset internal device
2	AD13	PISA CPU onboard device # 1
3	AD14	PISA CPU onboard device # 2
4	AD15	PISA CPU onboard device # 3
5	AD16	PISA CPU onboard device # 4
6	AD17	
7	AD18	
8	AD19	PISA Backplane slot # 1
9	AD20	PISA Backplane slot # 2
10	AD21	PISA Backplane slot # 3
11	AD22	PISA Backplane slot # 4
12	AD23	
13	AD24	
14	AD25	
15	AD26	

PCI slot is mapped to target device #6









*: original riser differs from PISA specification
#: Error in PISA specification; should be AD31

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