James Ensminger

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EXPERIENCE

Applications Engineer Nov 2023 - Present

PowerFlex | Mountain View, CA and Los Angeles, CA

- Enhancing EVSE communication reliability through bench testing, innovative tooling, and data-driven R&D.
- Advancing distributed control system design iterations with the HW team for optimized power distribution, networking, and telemetry between onsite network devices and DERs.
- Leading the development, launch, and maintenance of customer-facing and internal-facing technical documentation platforms on PowerFlex HW and SW products along with documentation creation.

Asset Health and Performance Center Engineering Intern Jun 2021 - Sep 2021

Pacific Gas and Electric | San Francisco, CA

- Leveraged GIS to provide informative data on future EFD (Early Fault Detection) and DFA (Distribution Fault Anticipation) line sensor technology installments across Northern California's electric grid.
- Managed and cross-functionally coordinated multiple teams to compile a quarterly voltage curtailment report on solar powered line sensor units, while taking initiative to reduce data compilation processing time by 20% on Palantir Foundry (saving 1 hour) through root cause analysis and process improvement methodologies.

PROJECTS AND ACHIEVEMENTS

Multi-Device Wireless Charger Dec 2022 - Jun 2023

- Created a Qi standard wireless charger with increased freedom of placement for multi-device charging, an intuitive visual charge indicator determined by stakeholders, and an efficient heat management system enabling it to operate 5°C cooler than chargers on the market.

Ground Bounce PCB Test Circuit Mar 2022 - Jun 2022

- Designed a PCB test circuit to experimentally observe the electrical phenomena of ground bounce.
- Developed the PCB design with OrCAD Capture and Allegro PCB Editor, then milled it using an M60 LPKF.

"Bouncy Ball" Verilog Game Nov 2021 - Dec 2021

- Designed a fully synchronous Verilog game programmed on a Basys3 FPGA featuring an FSM and VGA timing logic (Hsync/Vsync, pixel counters) for real-time graphical display of gameplay logic, motion dynamics, and collision handling.
- Performed hardware verification of RTL system through simulations and on-board testing, achieving timing closure at 25MHz with a 33MHz maximum operating frequency.

EDUCATION

University of Southern California | Master of Science in Electrical Engineering Aug 2025 - May 2027

- **Coursework:** Modern Solid-State Devices, Power Systems, MOS VLSI Design, Nanotechnology

University of California, Santa Cruz | Bachelor of Science in Electrical Engineering Sep 2019 - Jun 2023

- **Clubs:** MEP, NeuroTechSC, SlugSat, UCSC IEEE
- **Grader:** ECE178 and ECE224 Semiconductor Device Electronics [Winter Quarter 2023]
- **Coursework:** Logic Design, High-Speed Digital Design, Analog Electronics & Circuit Design, Signals & Systems, Feedback Control, Embedded Systems, Physics, Probability Statistics, Properties of Materials, Communication Systems, Energy Conversion & Control, Adv. Renewable Energy Sources, Electromagnetic Fields & Waves, Senior Design Capstone

SKILLS, TOOLS, AND TECHNOLOGIES

- **Electrical:** OrCAD Capture, PSpice, Allegro PCB Editor, Cadence Virtuoso, Ansys Maxwell, Hardware Development/Debugging, Microcontrollers, RTL Design, FPGA, PLC programming (IEC 61131-3), Modbus TCP, Computer Networking, Soldering, Lab Equipment (Oscilloscopes, Signal Generators, Power Supplies, DMMs, Spectrum Analyzers)
- **Software:** Verilog, Python, C, Java, SQL, PowerShell, Linux, Git, MATLAB
- **Mechanical:** SolidWorks, 3D Printing, Ansys Mechanical