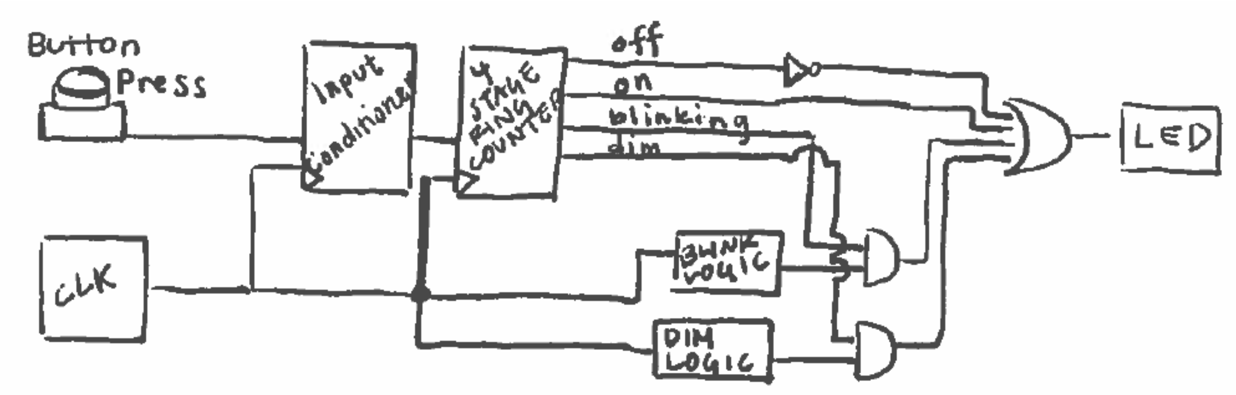
Block Diagram



The system is made up of a button, an internal clock (**clk**), an input conditioner, a 4-stage ring counter that toggles between the four modes, logic for '**blinking**', logic for '**dim**', some basic components to manage various stages, and an LED driver.

Total Cost Estimate

Component	Total
System Clock*	2
Input Conditioner	533
4-Stage Ring Counter	83
Blink Logic	182
Dim Logic	112
Stage -> LED Driver Components* **(Inverter, one 4 Input OR, two 2 Input ANDs)**	1+5+3+3
LED Driver*	211
ALL COMPONENTS	1135

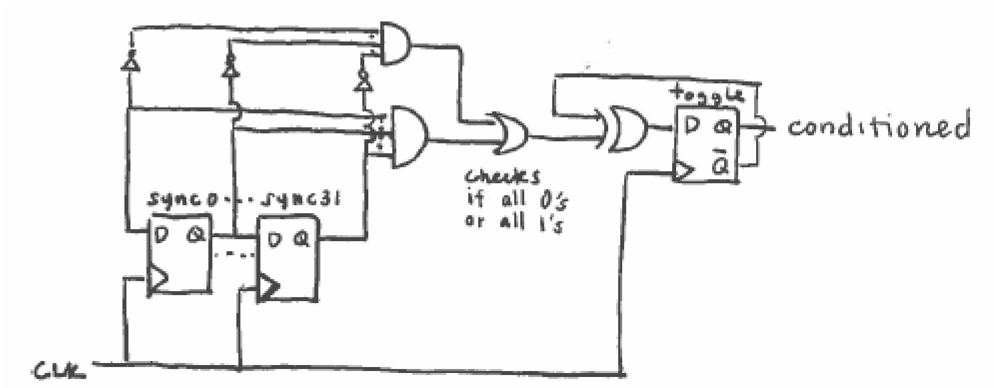
* = pre-baked

Non-"Pre-Baked" Components

- Input Conditioner
    - Specifications
        - The input conditioner takes in the noisy signal from the button press. Since the button noise/bouncing decays within 1 ms and the system clock runs at 32,768 Hz, the signal should settle after 32.768 clock cycles, so an assumption is made that the signal should settle after 32

clock cycles (2^5 clock cycles). Thus, the input passes through 32 flip-flops, and once the inputs and outputs of the flip-flops are all equal, meaning that the noise has settled, then the toggle will occur.

- Inputs
  - **clk** is the clock input from the system clock.
  - **noisy signal** is a one-bit signal from the button.
- Outputs
  - **conditioned** is a one-bit conditioned output.
- Schematic



(NOTE: this is a costly method that can be simplified)

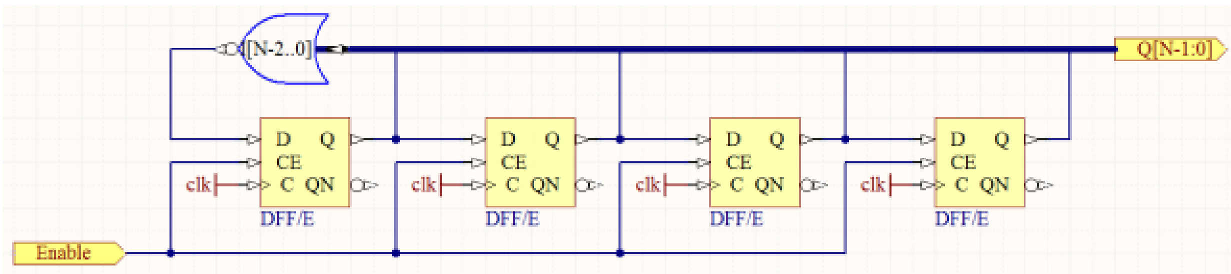
- Size of component in terms of the number of Gate Inputs it uses

Subcomponent	**Cost per**	**# Used**	**Total**
Edge-Triggered D-Flip-Flop	13	33	429
32 Input AND Gate	32+1	2	66
Inverter	1	33	33
2 Input OR Gate	2+1	1	3
2 Input XOR Gate	2	1	2
			533

- 4-Stage Ring Counter
  - Specifications
    - This parameterized component is a one-hot counter. When **E** is asserted, the hot bit moves one element down the ring each positive **clk** edge.
  - Inputs

- **clk** is the clock input.
- **E** is the enable input.

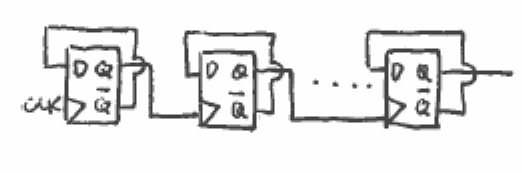
- Outputs
  - **Q[3:0]** has exactly one bit high and all others are low. The high rotates through the group each positive **clk** edge when **E** is asserted high.
  - The **NOR** gate restarts the cycle when the hot bit is at the end of the ring.
- Schematic



- Size of component in terms of the number of Gate Inputs it uses

Subcomponent	Cost per	# Used	Total
D-Flip-Flop with Enable	20	4	80
3 Input NOR	3	1	3
			83

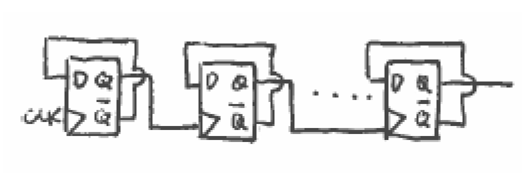
- Blink Logic
  - Specifications
    - The blink logic is to adjust the frequency specifically for the blink mode, which, on the specifications sheet is noted as having a frequency of 4.0 Hz. Thus, the blink logic consists of a chain of **13** flip-flops as each flip-flop halves the input frequency.
  - Inputs
    - **clk** is the clock input from the system clock.
  - Outputs
    - The output is a modified clock running at a frequency of 4.0 Hz.
  - Schematic



- Size of component in terms of the number of Gate Inputs it uses

Subcomponent	Cost per	# Used	Total
Edge Triggered D-Flip-Flop	13	13	169
Inverter	1	13	13
			182

- Dim Logic
  - Specifications
    - The dim logic is to adjust the frequency specifically for the dim mode, which is set to 128 Hz since that is the human vision flicker limitation. Thus, the dim logic consists of a chain of **8** flip-flops as each flip-flop halves the input frequency.
  - Inputs
    - **clk** is the clock input from the system clock.
  - Outputs
    - The output is a modified clock running at a frequency of 128 Hz.
  - Schematic



(Same logic as blink but with a different number of flip-flops (8 instead of 13)

  - Size of component in terms of the number of Gate Inputs it uses

Subcomponent	Cost per	# Used	Total
Edge Triggered D-Flip-Flop	13	8	104
Inverter	1	8	8
			112