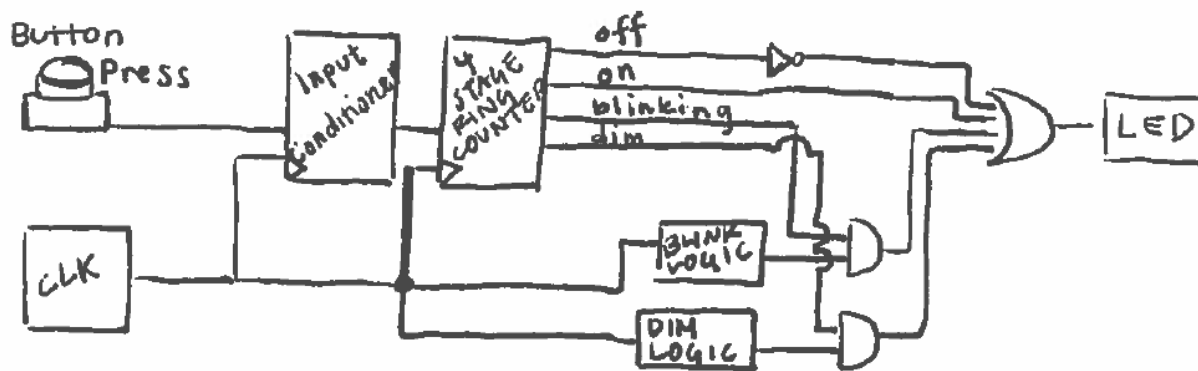


Block Diagram



The system is made up of a button, an internal clock (clk), an input conditioner, a 4-stage ring counter, logic for 'blinking', logic for 'dim', some basic components to manage various stages, and an LED driver to drive the LED with the output of all the logic.

Total Cost Estimate

Component	Total
System Clock*	2
Input Conditioner	533
4-Stage Ring Counter	83
Blink Logic	182
Dim Logic	112
Stage -> LED Driver Components (Inverter, OR, two ANDs)	1+5+3+3
LED Driver*	211
ALL COMPONENTS	1135

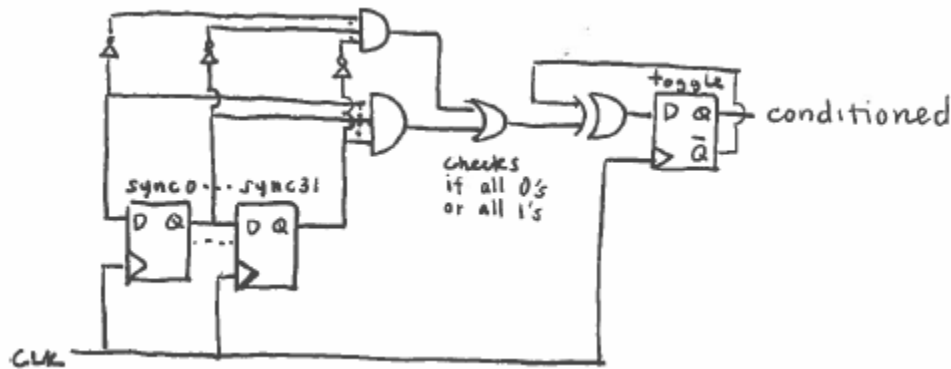
* = pre-baked

Non-“Pre-Baked” Components

- Input Conditioner
 - Specifications
 - The input conditioner takes in the noisy signal from the button press. Since the button noise/bouncing decays within 1 ms and the system clock runs at 32,768 Hz, the signal should settle after 32.768 clock

cycles, so an assumption is made that the signal should settle after 32 clock cycles (2^5 clock cycles).

- Inputs
 - **clk** is the clock input from the system clock
 - **noisy signal** is a one-bit signal from the button
- Outputs
 - **conditioned** is a one-bit conditioned output
- Schematic



- Size of component in terms of the number of Gate Inputs it uses

Subcomponent	Cost per	# Used	Total
Edge-Triggered D-Flip-Flop	13	33	429
32 Input AND Gate	33	2	66
Inverter	1	33	33
2 Input OR Gate	2+1	1	3
2 Input XOR Gate	2	1	2
			533

- 4-Stage Ring Counter

- Specifications
 - This parameterized component is a one-hot counter. When E is asserted, the hot bit moves one element down the ring each positive **clk** edge
- Inputs
 - **clk** is the clock input
 - **E** is the enable input
- Outputs

-

- | Subcomponent | Cost per | # Used | Total |
|--------------|----------|--------|-------|
| DFF w/ E | 20 | 4 | 80 |
| 3 NOR | 3 | 1 | 3 |

- Specifications

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Subcomponent	Cost per	# Used	Total
Edge Triggered D-Flip-Flop	13	13	169
Inverter	1	13	13
			182

- Dim Logic
 - Specifications
 - The dim logic is to adjust the frequency specifically for the dim mode, which is set to 128 Hz since that is the human vision flicker limitation. Thus, the blink logic consists of a chain of 8 flip-flops as each flip-flop halves the input frequency.
 - Inputs
 - **clk** is the clock input from the system clock
 - Outputs
 - a modified clock running at a frequency of 128 Hz.
 - Schematic



(Same logic as blink but with a different number of flip-flops)

- Size of component in terms of the number of Gate Inputs it uses

Subcomponent	Cost per	# Used	Total
Edge Triggered D-Flip-Flop	13	8	104
Inverter	1	8	8
			112