COEN 313 Lab 3

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ID number:	40009896
Course number:	COEN313 UJ-X Lab
Date performed:	Wednesday, 8 March 2023
Due Date:	Wednesday, 22 March 2023

"I certify that this submission is my original work and meets the Faculty's Expectations of Originality"

Table of Contents

1. Objective

The objective of this lab is to build a combinational VHDL code to convert a 4 bits input into its equivalent 4 bits two's complement representation. The following table will be the representation of the circuit.

Input	Value is sign-magnitude	Value in 2's complement	Output
0000	+0	+0	0000
0001	+1	+1	0001
0010	+2	+2	0010
0011	+3	+3	0011
0100	+4	+4	0100
0101	+5	+5	0101
0110	+6	+6	0110
0111	+7	+7	0111
1000	-0	-8	1000

Figure 1 look up table for the converter when positive

Input	Value is sign-magnitude	Value in 2's complement	Output
1001	-1	-7	1111
1010	-2	-6	1110
1011	-3	-5	1101
1100	-4	-4	1100
1101	-5	-3	1011
1110	-6	-2	1010
1111	-7	-1	1001

Figure 2 look up table for the converter when negative

Here is the conceptual diagram to implement the VHDL simulation code.

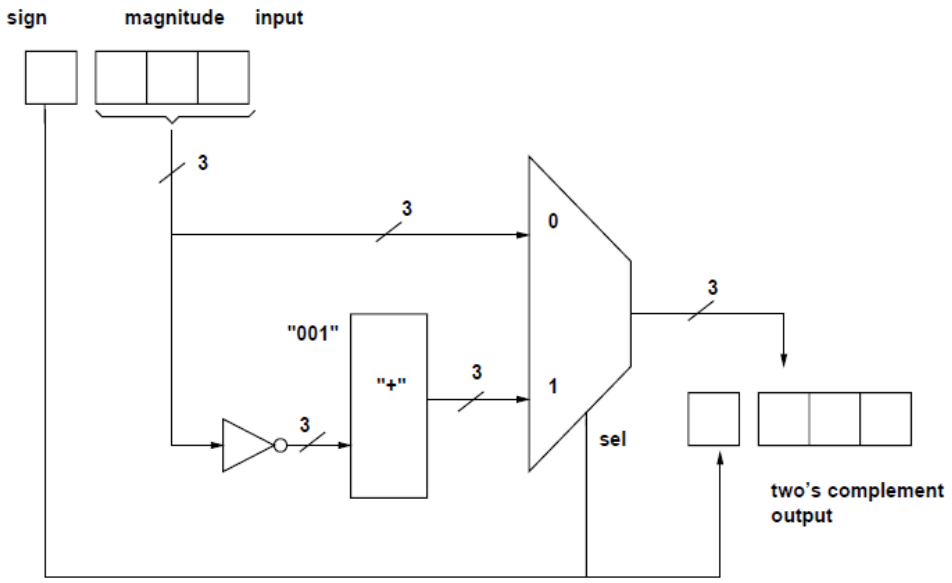

Figure 3 Conceptual diagram

In this report, a concurrent structure, consisting of a 2x1 mux, will be used to implement the circuit in the design.

2. Procedure

2.1 VHDL simulation :

In this simulation are going to exam the first bit by an if statement.

If the MSB is ==0 we keep the rest 3 bits, else we toggle the 3 bits and plus “001”.

I wrote 1 vhd file(converter.vhd) and 1 do file(lab3.do) to test all the possible cases.

2.1.1 Writing vhdl code

```
--SID:40009896
--Name:JUNPENG GAI
library ieee;
use IEEE.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity converter is
port( sign_mag : in std_logic_vector(3 downto 0) ;
twos_comp : out std_logic_vector(3 downto 0) );
end converter;


architecture complement of converter is
--11
signal tempinput1 :std_logic_vector (2 downto 0);
signal tempinput2 :std_logic_vector (2 downto 0);
signal tempinput3 :std_logic_vector (2 downto 0);
signal sel:std_logic;

begin
tempinput1 <= not sign_mag(2 downto 0);
sel<=sign_mag(3);
tempinput2 <= tempinput1+"001";

process(sign_mag,sel)
begin
if(sel='0')then
tempinput3 <= sign_mag(2 downto 0);
else
tempinput3 <=tempinput2;
end if;
end process;
twos_comp<=sel & tempinput3;
end complement;
```

Figure 4 converter.vhdl

We created 3 intermedia signals:

tempinput1: taking the invert result of

tempinput2: tempinput1+”001”;

tempinput3: taking original sign_mag(2 downto 0) when sel is 0 else taking tempinput2 which is the two’s complement for the negative number.

2.1.2 Modelsim simulation

Here is our do file

```
add wave sign_mag
add wave twos_comp

force sign_mag 0000
run 2
force sign_mag 0001

run 2
force sign_mag 0010

run 2
force sign_mag 0011

run 2
force sign_mag 0100

run 2
force sign_mag 0101

run 2
force sign_mag 0110

run 2
force sign_mag 0111

run 2

force sign_mag 1000

run 2
force sign_mag 1001

run 2
force sign_mag 1010

run 2
force sign_mag 1011

run 2
force sign_mag 1100

run 2
force sign_mag 1101

run 2
force sign_mag 1110

run 2
force sign_mag 1111

run 2
```

Table 2 lab2.do file

Therefore, we can use the modelsim to generate the wave:

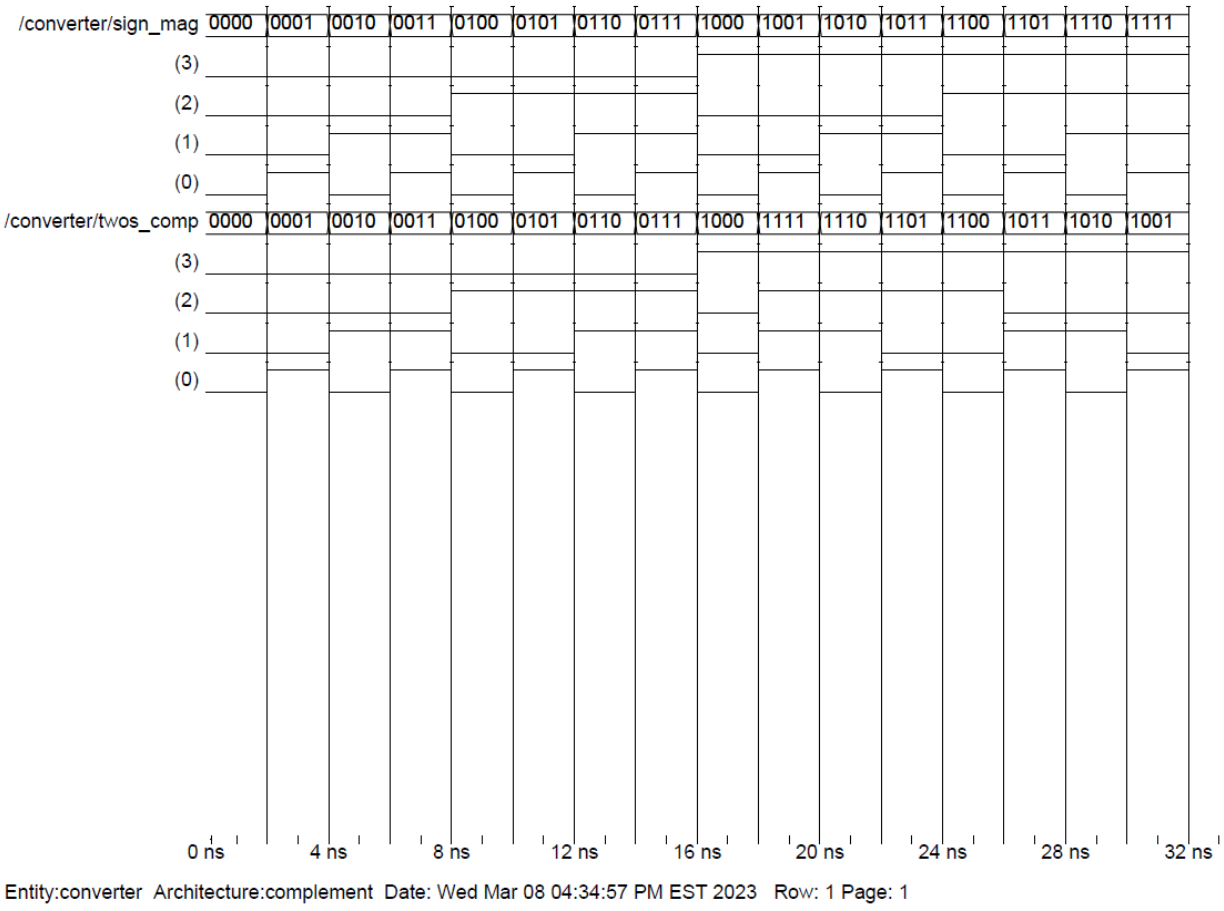

Figure 5 Modelsim result for port map version

Since we have 4 bits meaning that we will have 2^4 =16combinations, from the figure above we can see that the first 8 inputs are the positive number and its 2's complement is the same. For the rest 8 combinations, they are negative numbers and the tow's complement is 1+invert(xxx)+"001".

The simulation results prove that the vhdl code is on the right track, then we can move to the FPGA implementation.

2.1.3 Xilin implementation

After we import the vhd file and constrain file to the Xilinx Vivado, above figure shows us the elaboration design for the device in the FPGA board.

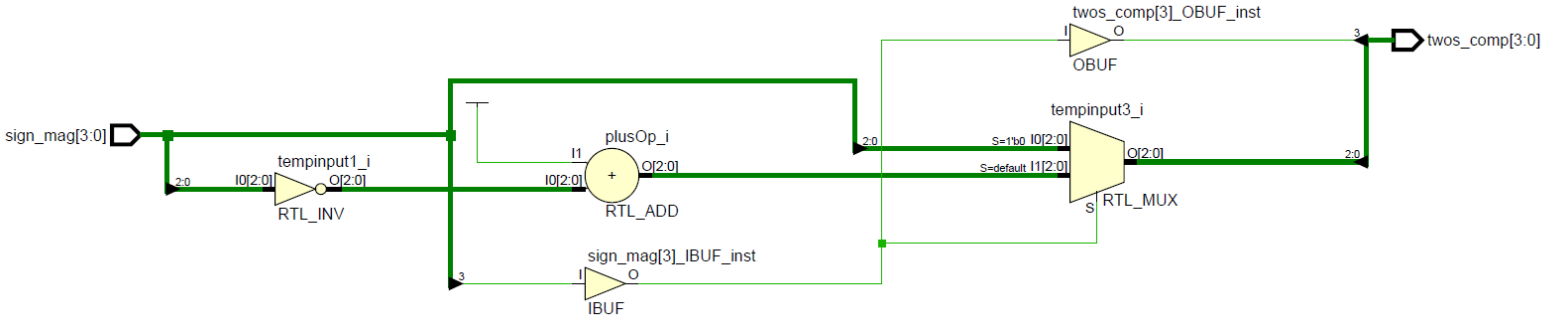

Figure 7 RTL elaborated schematic

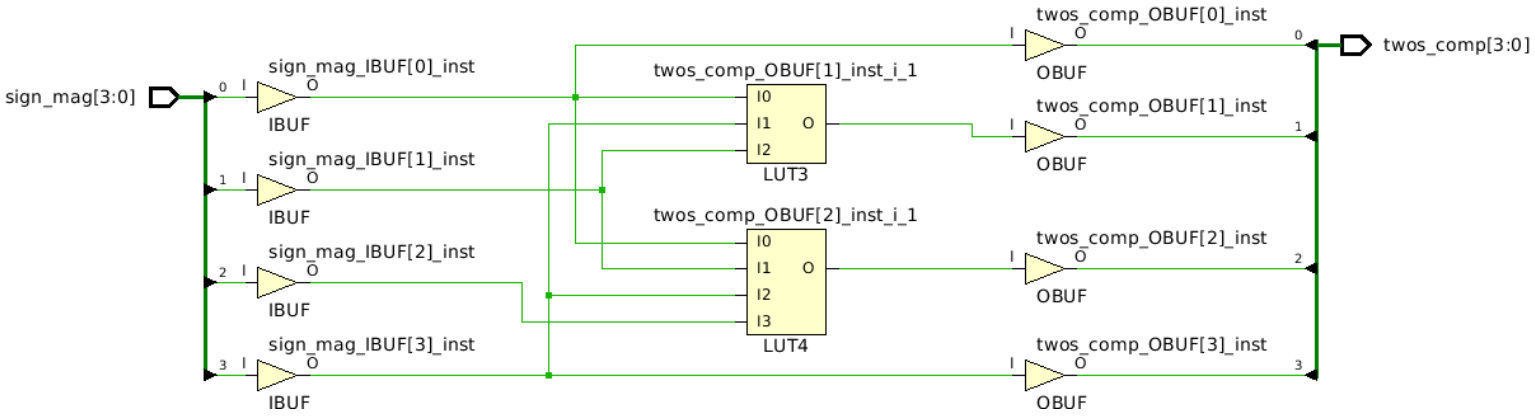

Figure 4 Implementation design schematic

Here is the RTL schematic, from the figure we can see that this is very similar to the conceptual diagram in the lab manual.

```
# Vivado does not support old UCF syntax
# must use XDC syntax


set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCMOS33 }   [ get_ports { sign_mag(3) }       ] ;
set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCMOS33 }   [ get_ports { sign_mag(2) }  ] ;
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 }   [ get_ports { sign_mag(1) }    ] ;
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 }   [ get_ports { sign_mag(0) }       ] ;
set_property -dict { PACKAGE_PIN N14 IOSTANDARD LVCMOS33 }   [ get_ports { twos_comp(3) }    ] ;
set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 }   [ get_ports { twos_comp(2) }    ] ;
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 }   [ get_ports { twos_comp(1) }    ] ;
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 }   [ get_ports { twos_comp(0) }    ] ;
```

Figure 5 lab3.xdc constrain file

Above is the xdc file we used to implement the .bit file to the FPGA board. Here I set the switch J15, L16, M13, R15 to the input and N14, J13, K15, H17 are setting to the output led.In the lab section I have demonstrated the FPGA to the Teaching Assistant.

2.1.4 Log files

As required in the lab manual, we need to upload 2 log files which are synthesis and implementation log files. **I have attached all the files in the appendix.**

Implementation warning:

WARNING: [Power 33-232] No user defined clocks were found in the design!

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

Here because our design doesn't include a user defined clock, so the Xilinx will automatically constrain clocks for us.

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties:

Because we didn't specify any configuration voltage and also, it's not given in the manual. By looking it up in the online material, those value are supposed to be defined in the constrain file , but our constrain file only contains GPIO instead of some parameters like CONFIG_VOLTAGE.

Synthesis warning:

WARNING: [Constraints 18-5210] No constraint will be written out.

This is the same issue as showing above and our constrain file is too simple. Seems like we need to learn more about the constrain in the Xilinx Vivado to specify timing, placement and other requirements.

Conclusion

In this lab section, we have practiced how to design and implement the project from an idea of a conceptual diagram. There are always lots of ways to implement the design, in this lab we can use either concurrent statement or sequential statement to write the VHDL code. I chose the concurrent one and test the results with all possible cases. Also, I learnt how to write xdc constrain file for std_logic_vector in this lab, I should use vector[n] instead of vector(n).

3. Question

1. ***What will result (during synthesis) if a signal appears on both sides of the signal assignment operator (<=) within a combinational VHDL process such as:***

   If on both sides of the signal assignment operator, which means this is a feedback circuit which is wrong in the design. I think maybe the synthesis will optimize the design to fix the problem like using an intermedia signal.

2. ***What will happen during simulation if a signal is read from within a combinational process but does not appear in the process sensitivity list?***

   If a signal doesn't appear in the sensitivity list, even if the signal changed process won't response to it and update the value. Only when the other parameters changed, it's value will be updated. For example, in our lab, if we forget to include the signal ***sel*** the result will be a mess. No matter the original 4bits is positive or negative, we won't update the ***sel*** signal, so the circuit will treat all the input as positive/negative numbers.

3. ***If you made use of variable in your combinational process, rewrite the VHDL code such that the process makes use of only signals. If you originally made use of only signals, rewrite your VHDL code such that it makes use of variable(s). Simulate your new VHDL code to show that it gives the same simulation results. You do not have to re-synthesize.***

Comment on the salient differences between the code which uses only signals and the code which makes use of a variable.

```
library ieee;
use IEEE.std_logic_1164.all;
use IEEE.NUMERIC_STD.all;
entity converter2 is
port( sign_mag : in std_logic_vector(3 downto 0) ;
twos_comp : out std_logic_vector(3 downto 0) );
end converter2;


architecture complement of converter2 is
--ll
begin
process(sign_mag)

variable temp:unsigned(3 downto 0);
begin
temp:=unsigned(sign_mag);
if(sign_mag(3)='0')then
temp:=temp;
else
temp(2 downto 0):= 1+unsigned(not sign_mag(2 downto 0));
end if;
twos_comp<=std_logic_vector(temp);
end process;
end complement;
```

Figure 6 Modified code with variable

Here is the modified code with variable, because I used the signal in the lab section. Following is the simulation result of this modified code.

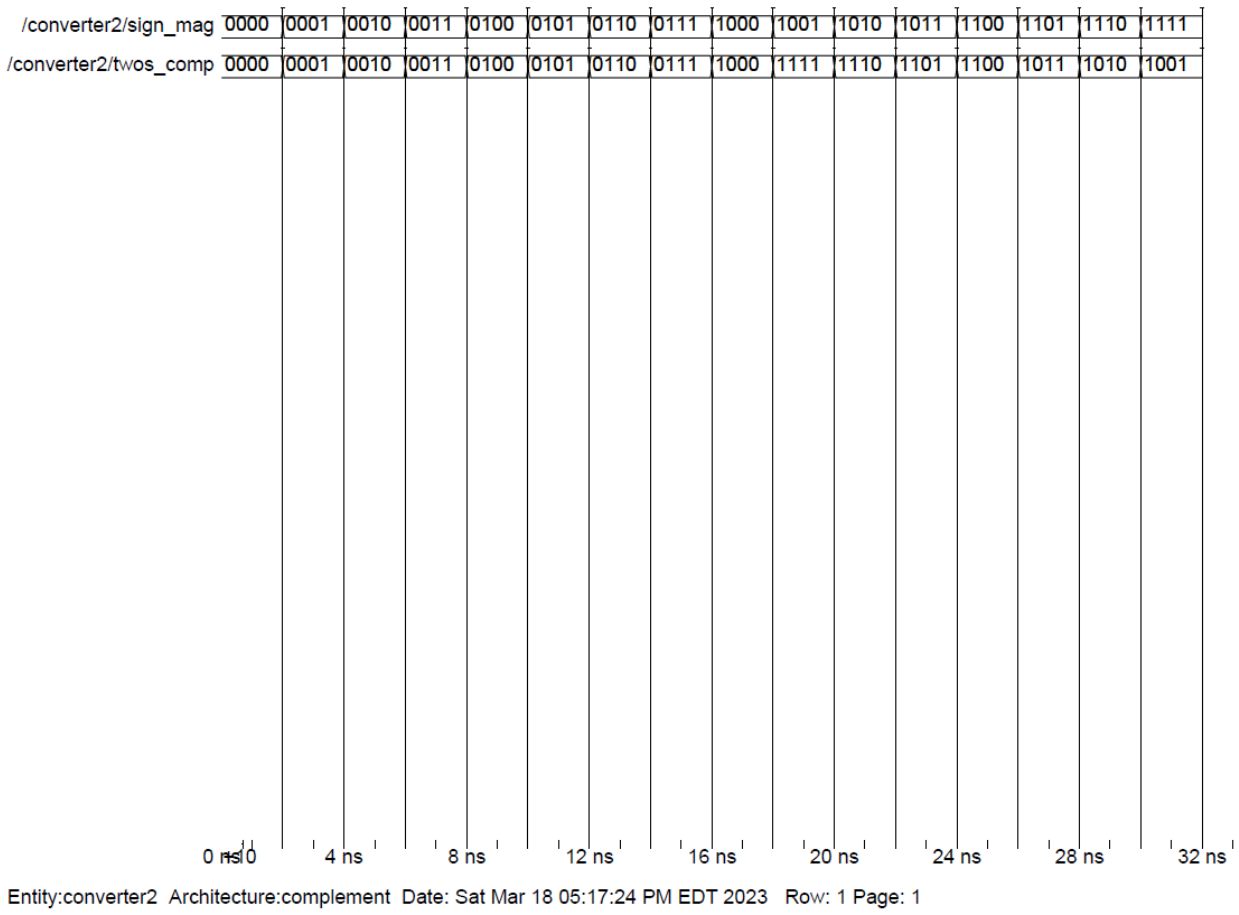

Figure 7 Simulation result of using variable

In general, signal and variable are interchangeable, we can use either variable or signal to design the same circuit but one of them is better for certain requirements.

By comparing the results, I find out that variable is more flexible compared with signal. Sometime when we have value<= not value situation, signal it's easier to use. Variable is like a small storage of memory, we can perform calculation, comparison and assignment.

4. Appendix

5.1 converter.vhdl

```
--sid:40009896:
--name:Junpeng GAI
library ieee;
use IEEE.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity converter is
port( sign_mag : in std_logic_vector(3 downto 0) ;
twos_comp : out std_logic_vector(3 downto 0) );
end converter;


architecture complement of converter is
--11
signal tempinput1 :std_logic_vector (2 downto 0);
signal tempinput2 :std_logic_vector (2 downto 0);
signal tempinput3 :std_logic_vector (2 downto 0);
signal sel:std_logic;

begin

tempinput1 <= not sign_mag(2 downto 0);
sel<=sign_mag(3);
--20
```

```
tempinput2 <= tempinput1+"001";

tempinput3      <= sign_mag(2 downto 0)when sel='0' else
                   tempinput2;
twos_comp<=sel & tempinput3;

end complement;
```

5.2 lab3.do

```
add wave sign_mag
add wave twos_comp

force sign_mag 0000
run 2
force sign_mag 0001

run 2
force sign_mag 0010

run 2
force sign_mag 0011
```

run 2

force sign_mag 0100

run 2

force sign_mag 0101

run 2

force sign_mag 0110

run 2

force sign_mag 0111

run 2

force sign_mag 1000

run 2

force sign_mag 1001

run 2

force sign_mag 1010

run 2

force sign_mag 1011

run 2

force sign_mag 1100

run 2

force sign_mag 1101

run 2

force sign_mag 1110

run 2

force sign_mag 1111

run 2

5.3 lab3.xdc

 # Vivado does not support old UCF syntax

 # must use XDC syntax

set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCMOS33 } [get_ports { sign_mag(3) }] ;

set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCMOS33 } [get_ports { sign_mag(2) }] ;

set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 } [get_ports { sign_mag(1) }] ;

set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [get_ports { sign_mag(0) }] ;

set_property -dict { PACKAGE_PIN N14 IOSTANDARD LVCMOS33 } [get_ports { twos_comp(3) }] ;

set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 } [get_ports { twos_comp(2) }] ;

set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 } [get_ports { twos_comp(1) }] ;

set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [get_ports { twos_comp(0) }] ;

5.4 implementation.log

**** Running vivado*

with args -log converter.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source converter.tcl -notrace

******* Vivado v2018.2 (64-bit)*

***** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018*

***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018*

*** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.*

source converter.tcl -notrace

Command: link_design -top converter -part xc7a100tcsg324-1

Design is defaulting to srcset: sources_1

Design is defaulting to constrset: constrs_1

INFO: [Netlist 29-17] Analyzing 4 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/constrs_1/imports/Lab3/ct.xdc]

Finished Parsing XDC File [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/constrs_1/imports/Lab3/ct.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link_design completed successfully

link_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:31 . Memory (MB): peak = 1652.371 ; gain = 344.242 ; free physical = 8831 ; free virtual = 20958

Command: opt_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:00.11 ; elapsed = 00:00:00.32 . Memory (MB): peak = 1720.395 ; gain = 68.023 ; free physical = 8830 ; free virtual = 20956

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:09 ; elapsed = 00:00:37 . Memory (MB): peak = 2166.895 ; gain = 446.500 ; free physical = 8409 ; free virtual = 20536

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

Ending Logic Optimization Task | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.895 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2166.898 ; gain = 0.004 ; free physical = 8445 ; free virtual = 20571

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 1bfe8fc0e

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.898 ; gain = 0.000 ; free physical = 8445 ; free virtual = 20571

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt_design completed successfully

opt_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 2166.898 ; gain = 514.527 ; free physical = 8445 ; free virtual = 20571

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2198.914 ; gain = 0.004 ; free physical = 8441 ; free virtual = 20569

INFO: [Common 17-1381] The checkpoint '/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/impl_1/converter_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report_drc -file converter_drc_opted.rpt -pb converter_drc_opted.pb -rpx converter_drc_opted.rpx

Command: report_drc -file converter_drc_opted.rpt -pb converter_drc_opted.pb -rpx converter_drc_opted.rpx

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/impl_1/converter_drc_opted.rpt.

report_drc completed successfully

Command: place_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Running DRC as a precondition to command place_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8403 ; free virtual = 20530

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 19cdfb6e3

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8403 ; free virtual = 20530

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8403 ; free virtual = 20530

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 19cdfb6e3

Time (s): cpu = 00:00:00.52 ; elapsed = 00:00:00.34 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8403 ; free virtual = 20530

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 286dc5eca

Time (s): cpu = 00:00:00.57 ; elapsed = 00:00:00.36 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8402 ; free virtual = 20529

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 286dc5eca

Time (s): cpu = 00:00:00.57 ; elapsed = 00:00:00.36 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8402 ; free virtual = 20529

Phase 1 Placer Initialization | Checksum: 286dc5eca

Time (s): cpu = 00:00:00.57 ; elapsed = 00:00:00.36 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8402 ; free virtual = 20529

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 286dc5eca

Time (s): cpu = 00:00:00.60 ; elapsed = 00:00:00.38 . Memory (MB): peak = 2270.949 ; gain = 0.000 ; free physical = 8401 ; free virtual = 20528

WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 1d3407b14

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.47 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8382 ; free virtual = 20509

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 1d3407b14

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.47 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8382 ; free virtual = 20509

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 252d17ac3

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.49 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8382 ; free virtual = 20509

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 29a164c8b

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.49 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8382 ; free virtual = 20509

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 29a164c8b

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.49 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8382 ; free virtual = 20509

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.77 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8377 ; free virtual = 20504

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.77 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8377 ; free virtual = 20504

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8377 ; free virtual = 20504

Phase 3 Detail Placement | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8377 ; free virtual = 20504

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8377 ; free virtual = 20504

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8379 ; free virtual = 20506

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8379 ; free virtual = 20506

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8379 ; free virtual = 20506

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1cf8e3121

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8379 ; free virtual = 20506

Ending Placer Task | Checksum: 10eed454d

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2332.965 ; gain = 62.016 ; free physical = 8396 ; free virtual = 20523

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place_design completed successfully

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2332.965 ; gain = 0.000 ; free physical = 8394 ; free virtual = 20522

INFO: [Common 17-1381] The checkpoint '/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/impl_1/converter_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report_io -file converter_io_placed.rpt

report_io: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2332.965 ; gain = 0.000 ; free physical = 8388 ; free virtual = 20515

INFO: [runtcl-4] Executing : report_utilization -file converter_utilization_placed.rpt -pb converter_utilization_placed.pb

report_utilization: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2332.965 ; gain = 0.000 ; free physical = 8395 ; free virtual = 20522

INFO: [runtcl-4] Executing : report_control_sets -verbose -file converter_control_sets_placed.rpt

report_control_sets: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2332.965 ; gain = 0.000 ; free physical = 8396 ; free virtual = 20523

Command: route_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs

Checksum: PlaceDB: 5e51c835 ConstDB: 0 ShapeSum: b09b7d18 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 128b152d0

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2390.973 ; gain = 58.008 ; free physical = 8240 ; free virtual = 20368

Post Restoration Checksum: NetGraph: 2f37f4c3 NumContArr: f9795e0d Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 128b152d0

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2397.961 ; gain = 64.996 ; free physical = 8210 ; free virtual = 20337

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 128b152d0

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2397.961 ; gain = 64.996 ; free physical = 8210 ; free virtual = 20337

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: a26ae473

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8206 ; free virtual = 20334

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 65d1dbb5

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8205 ; free virtual = 20332

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8205 ; free virtual = 20332

Phase 4 Rip-up And Reroute | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8205 ; free virtual = 20332

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8205 ; free virtual = 20332

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8205 ; free virtual = 20332

Phase 6 Post Hold Fix | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8205 ; free virtual = 20332

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.00356879 %

Global Horizontal Routing Utilization = 0.00113669 %

*Routable Net Status**

***Does not include unroutable nets such as driverless and loadless.*

Run report_route_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 5.40541%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 10.8108%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 4.41176%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

Reporting congestion hotspots

Direction: North

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.227 ; gain = 71.262 ; free physical = 8204 ; free virtual = 20331

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 4d61382b

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.227 ; gain = 74.262 ; free physical = 8204 ; free virtual = 20331

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 5a4b1046

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.227 ; gain = 74.262 ; free physical = 8204 ; free virtual = 20331

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.227 ; gain = 74.262 ; free physical = 8236 ; free virtual = 20364

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route_design completed successfully

route_design: Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak = 2407.230 ; gain = 74.266 ; free physical = 8236 ; free virtual = 20364

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2407.230 ; gain = 0.000 ; free physical = 8237 ; free virtual = 20365

INFO: [Common 17-1381] The checkpoint '/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/impl_1/converter_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report_drc -file converter_drc_routed.rpt -pb converter_drc_routed.pb -rpx converter_drc_routed.rpx

Command: report_drc -file converter_drc_routed.rpt -pb converter_drc_routed.pb -rpx converter_drc_routed.rpx

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/impl_1/converter_drc_routed.rpt.

report_drc completed successfully

INFO: [runtcl-4] Executing : report_methodology -file converter_methodology_drc_routed.rpt -pb converter_methodology_drc_routed.pb -rpx converter_methodology_drc_routed.rpx

Command: report_methodology -file converter_methodology_drc_routed.rpt -pb converter_methodology_drc_routed.pb -rpx converter_methodology_drc_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 8 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/impl_1/converter_methodology_drc_routed.rpt.

report_methodology completed successfully

INFO: [runtcl-4] Executing : report_power -file converter_power_routed.rpt -pb converter_power_summary_routed.pb -rpx converter_power_routed.rpx

Command: report_power -file converter_power_routed.rpt -pb converter_power_summary_routed.pb -rpx converter_power_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report_power completed successfully

INFO: [runtcl-4] Executing : report_route_status -file converter_route_status.rpt -pb converter_route_status.pb

INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file converter_timing_summary_routed.rpt -pb converter_timing_summary_routed.pb -rpx converter_timing_summary_routed.rpx -warn_on_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report_incremental_reuse -file converter_incremental_reuse_routed.rpt

INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report_clock_utilization -file converter_clock_utilization_routed.rpt

INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file converter_bus_skew_routed.rpt -pb converter_bus_skew_routed.pb -rpx converter_bus_skew_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

INFO: [Common 17-206] Exiting Vivado at Wed Mar 8 16:13:57 2023...

**** Running vivado*

with args -log converter.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source converter.tcl -notrace

******* Vivado v2018.2 (64-bit)*

***** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018*

***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018*

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source converter.tcl -notrace

Command: open_checkpoint converter_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1277.113 ; gain = 0.000 ; free physical = 9149 ; free virtual = 21276

INFO: [Netlist 29-17] Analyzing 4 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.23 . Memory (MB): peak = 2079.062 ; gain = 0.004 ; free physical = 8293 ; free virtual = 20420

Restored from archive | CPU: 0.220000 secs | Memory: 0.938538 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.23 . Memory (MB): peak = 2079.062 ; gain = 0.004 ; free physical = 8293 ; free virtual = 20420

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

open_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:11 . Memory (MB): peak = 2079.062 ; gain = 801.953 ; free physical = 8292 ; free virtual = 20419

Command: write_bitstream -force converter.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write_bitstream

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

```
set_property CFGBVS value1 [current_design]
#where value1 is either VCCO or GND

set_property CONFIG_VOLTAGE value2 [current_design]
#where value2 is the voltage provided to configuration bank 0
```

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.

INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./converter.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

write_bitstream completed successfully

write_bitstream: Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 2550.902 ; gain = 471.840 ; free physical = 8223 ; free virtual = 20358

INFO: [Common 17-206] Exiting Vivado at Wed Mar 8 16:15:38 2023...

5.4 synthesis.log

**** Running vivado*

with args -log converter.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source converter.tcl

******* Vivado v2018.2 (64-bit)*

***** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018*

***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018*

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source converter.tcl -notrace

Command: synth_design -top converter -part xc7a100tcsg324-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 16412

Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.582 ; gain = 85.805 ; free physical = 8991 ; free virtual = 21117

INFO: [Synth 8-638] synthesizing module 'converter' [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/sources_1/imports/Lab3/converter.vhd:10]

INFO: [Synth 8-256] done synthesizing module 'converter' (1#1) [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/sources_1/imports/Lab3/converter.vhd:10]

Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.223 ; gain = 130.445 ; free physical = 9002 ; free virtual = 21128

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.223 ; gain = 130.445 ; free physical = 9002 ; free virtual = 21128

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.223 ; gain = 130.445 ; free physical = 9002 ; free virtual = 21128

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/constrs_1/imports/Lab3/ct.xdc]

Finished Parsing XDC File [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/constrs_1/imports/Lab3/ct.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.srcs/constrs_1/imports/Lab3/ct.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/converter_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/converter_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1760.977 ; gain = 0.000 ; free physical = 8724 ; free virtual = 20851

Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1760.977 ; gain = 445.199 ; free physical = 8812 ; free virtual = 20939

Start Loading Part and Timing Information

Loading part: xc7a100tcsg324-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1760.977 ; gain = 445.199 ; free physical = 8812 ; free virtual = 20939

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1760.977 ; gain = 445.199 ; free physical = 8812 ; free virtual = 20939

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1760.977 ; gain = 445.199 ; free physical = 8804 ; free virtual = 20931

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start RTL Component Statistics

Detailed RTL Component Info :

+---Adders :

2 Input 3 Bit Adders := 1

+---Muxes :

2 Input 3 Bit Muxes := 1

Finished RTL Component Statistics

Start RTL Hierarchical Component Statistics

Hierarchical RTL Component report

Module converter

Detailed RTL Component Info :

+---Adders :

2 Input 3 Bit Adders := 1

+---Muxes :

2 Input 3 Bit Muxes := 1

Finished RTL Hierarchical Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

Finished Part Resource Summary

Start Cross Boundary and Area Optimization

Warning: Parallel synthesis criteria is not met

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1760.977 ; gain = 445.199 ; free physical = 8793 ; free virtual = 20921

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:14 ; elapsed = 00:00:48 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:48 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:14 ; elapsed = 00:00:48 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Report Check Netlist:

```
+------+-----------------+-------+---------+-------+-----------------+
|      |Item             |Errors |Warnings |Status |Description      |
+------+-----------------+-------+---------+-------+-----------------+
|1     |multi_driven_nets|      0|        0|Passed |Multi driven nets|
+------+-----------------+-------+---------+-------+-----------------+
```

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Report RTL Partitions:

```
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
```

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Start Writing Synthesis Report

Report BlackBoxes:

+-+--------------+----------+

| |*BlackBox name* |*Instances* |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |*Cell* |*Count* |

+------+-----+------+

|*1* |*LUT3* | *1*|

|*2* |*LUT4* | *1*|

|*3* |*IBUF* | *4*|

|*4* |*OBUF* | *4*|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |*Instance* |*Module* |*Cells* |

+------+---------+-------+------+

|*1* |*top* | | *10*|

+------+---------+-------+------+

Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8672 ; free virtual = 20801

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:08 ; elapsed = 00:00:18 . Memory (MB): peak = 1772.969 ; gain = 142.438 ; free physical = 8727 ; free virtual = 20856

Synthesis Optimization Complete : Time (s): cpu = 00:00:15 ; elapsed = 00:00:49 . Memory (MB): peak = 1772.969 ; gain = 457.191 ; free physical = 8737 ; free virtual = 20866

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 4 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

14 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:16 ; elapsed = 00:00:50 . Memory (MB): peak = 1821.977 ; gain = 518.848 ; free physical = 8722 ; free virtual = 20851

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint '/nfs/home/j/j_gai/coen313/LABS/Lab3/lab3/lab3.runs/synth_1/converter.dcp' has been generated.

INFO: [runtcl-4] Executing : report_utilization -file converter_utilization_synth.rpt -pb converter_utilization_synth.pb

report_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.11 . Memory (MB): peak = 1846.000 ; gain = 0.000 ; free physical = 8723 ; free virtual = 20852

INFO: [Common 17-206] Exiting Vivado at Wed Mar 8 16:12:15 2023...