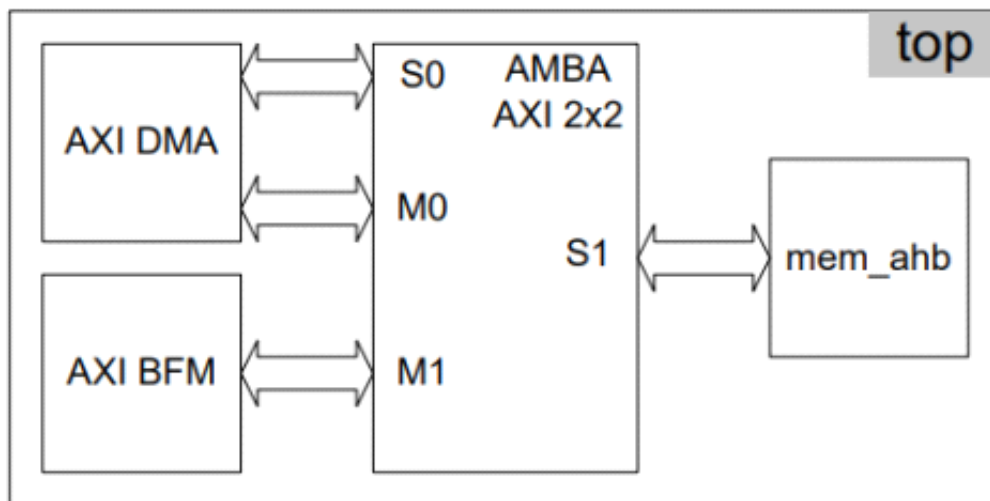


# 10\_axi dma -sent

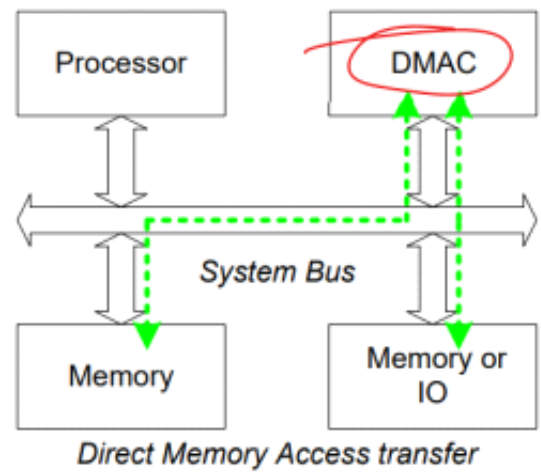
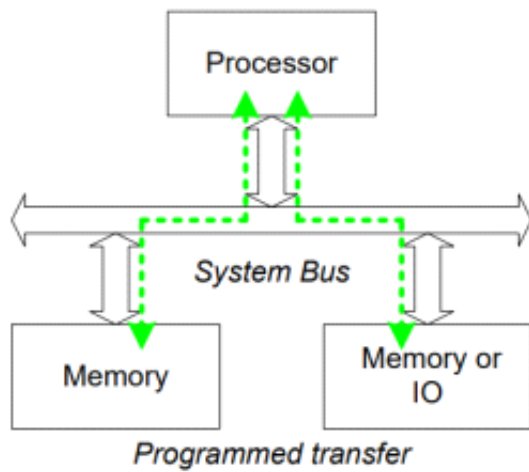
2022년 8월 25일 목요일 오후 3:14



## ❏ Test-bench includes

- ◆ DMA
- ◆ BFM: Controlling DMA
- ◆ Memory

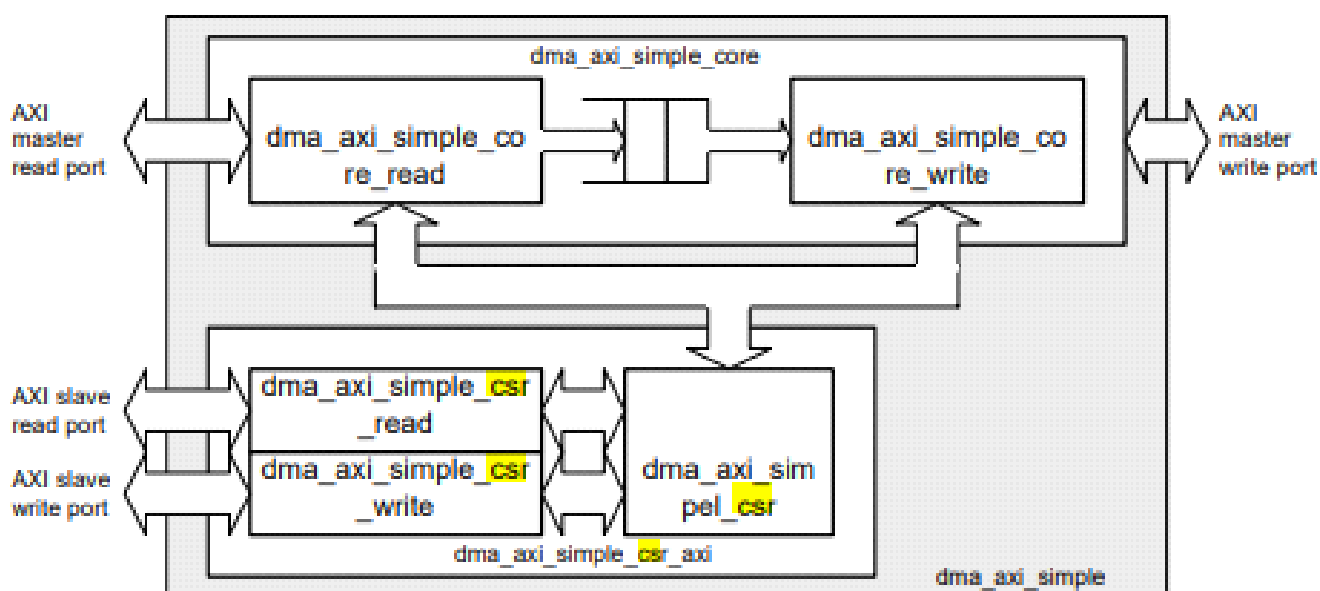
# Data transfer



```
//-----
// +-----+           +-----+
// | BFM |           | DMA |
// | MID[WIDTH_CID] --BFM_MID[WIDTH_CID]-- | |
// | AxID[WIDTH_ID] --BFM_AxID[WIDTH_ID]--+->| S_AxID[WIDTH_SID] |
// | |           | |
// -----
// +-----+           +-----+
// | DMA |           | MEM |
// | MID[WIDTH_CID] --MEM_MID[WIDTH_CID]-- | |
// | AxID[WIDTH_ID] --MEM_AxID[WIDTH_ID]--+->| AxID[WIDTH_SID] |
// | |           | |
// | |
```

## DMA CSR (1/3)

Name	Address offset		description
		Bit#	
NAME0	+000h	RO	DMA
NAME1	+004h	RO	AXI
NAME2	+008h	RO	
NAME3	+00Ch	RO	
COMP0	+010h	RO	DYNA
COMP1	+014h	RO	LITH
COMP2	+018h	RO	
COMP3	+01Ch	RO	
VERSION	+020h	RO	Version (0x2015_0712)
RESERVED	+024h		Reserved
	+028h		Reserved
	+02Ch		Reserved



```
//
localparam CSRA_NAME0    = 32'hA000_0000 + 8'h00,
           CSRA_NAME1    = 32'hA000_0000 + 8'h04,
           CSRA_NAME2    = 32'hA000_0000 + 8'h08,
           CSRA_NAME3    = 32'hA000_0000 + 8'h0C,
           CSRA_COMP0    = 32'hA000_0000 + 8'h10,
           CSRA_COMP1    = 32'hA000_0000 + 8'h14,
           CSRA_COMP2    = 32'hA000_0000 + 8'h18,
           CSRA_COMP3    = 32'hA000_0000 + 8'h1C,
           CSRA_VERSION  = 32'hA000_0000 + 8'h20,
           CSRA_CONTROL  = 32'hA000_0000 + 8'h30,
           CSRA_NUM      = 32'hA000_0000 + 8'h40,
           CSRA_SOURCE   = 32'hA000_0000 + 8'h44,
           CSRA_DEST     = 32'hA000_0000 + 8'h48;
//
```

```
xterm-adki@mylife
Main Options VT Options VT Fonts
# Loading work.mem_axi_dpram_sync
# run -all
# ** Warning: (vsim-8233) ../../rtl/verilog/dma_axi_simple_fifo_sync_small.v(155): Index xxxx into array dimension [0:15] is out of bounds.
# Time: 0 ps Iteration: 0 Instance: /top/u_dma/u_core/u_fifo
# top.u_mem_axi INFO 1024K (1048576) byte memory
#           140 top.u_bfm_axi.csr_test NAME0    A:0xa0000000 D:0x444d4120
#           210 top.u_bfm_axi.csr_test NAME1    A:0xa0000004 D:0x41584920
#           280 top.u_bfm_axi.csr_test NAME2    A:0xa0000008 D:0x20202020
#           350 top.u_bfm_axi.csr_test NAME3    A:0xa000000c D:0x20202020
#           420 top.u_bfm_axi.csr_test COMP0    A:0xa0000010 D:0x44594e41
#           490 top.u_bfm_axi.csr_test COMP1    A:0xa0000014 D:0x4c495448
#           560 top.u_bfm_axi.csr_test COMP2    A:0xa0000018 D:0x20202020
#           630 top.u_bfm_axi.csr_test COMP3    A:0xa000001c D:0x20202020
#           700 top.u_bfm_axi.csr_test VERSION  A:0xa0000020 D:0x20150712
#           770 top.u_bfm_axi.csr_test CONTROL  A:0xa0000030 D:0x00000000
#           840 top.u_bfm_axi.csr_test NUM      A:0xa0000040 D:0x00000000
#           910 top.u_bfm_axi.csr_test SOURCE   A:0xa0000044 D:0x00000000
#           980 top.u_bfm_axi.csr_test DEST     A:0xa0000048 D:0x00000000
#           1640 top.u_bfm_axi.one_dma_test OK
#           4120 top.u_bfm_axi.one_dma_test OK
#           4920 top.u_bfm_axi.one_dma_test OK
#           11460 top.u_bfm_axi.one_dma_test OK
#           12190 top.u_bfm_axi.one_dma_test OK
#           13060 top.u_bfm_axi.one_dma_test OK
#           14070 top.u_bfm_axi.one_dma_test OK
# ** Note: Data structure takes 6422592 bytes of memory
# Process time 0.05 seconds
# $finish : ../../bench/verilog/top.v(767)
# Time: 14165 ns Iteration: 2 Instance: /top
[adki@mylife]
```

