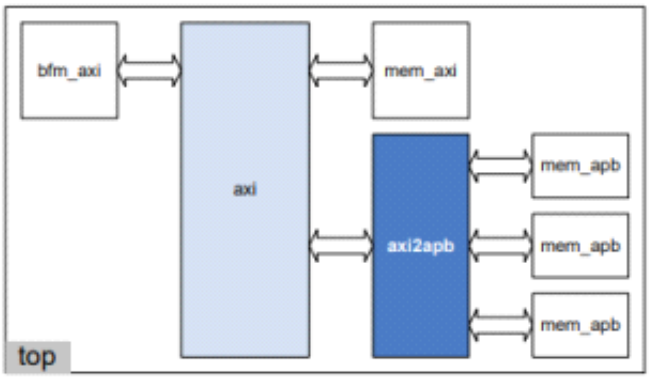
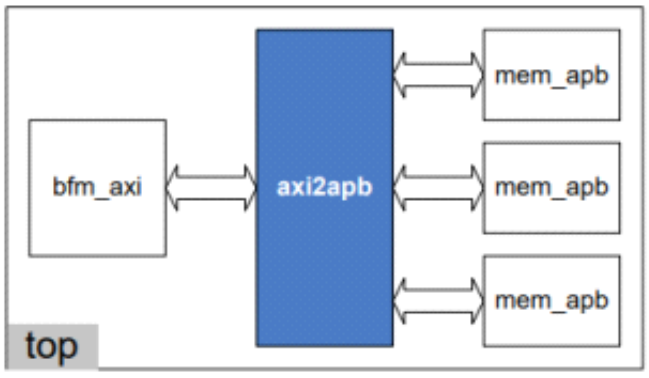
axi_to_apb

2022년 8월 22일 월요일 오후 3:24

AMBA AXI-to-APB design & verification

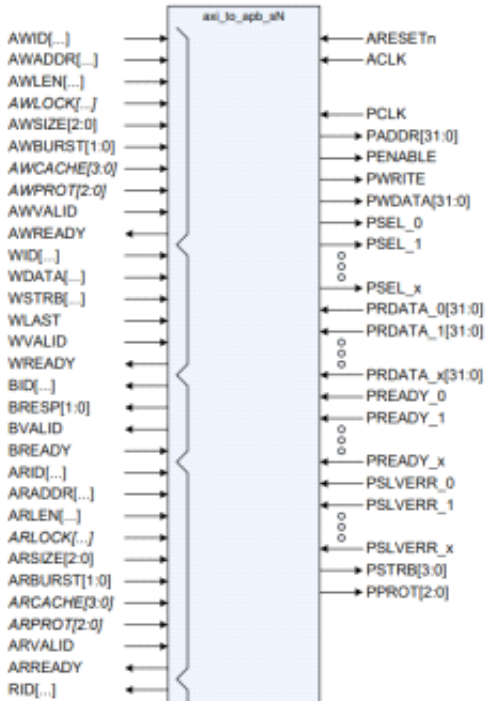


- Test-bench includes 'BFM', 'AMBA AXI', and 'MEMORY'.
- BFM generates test-pattern and test-vector.

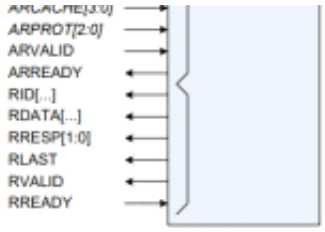


 AXI to APB (2)

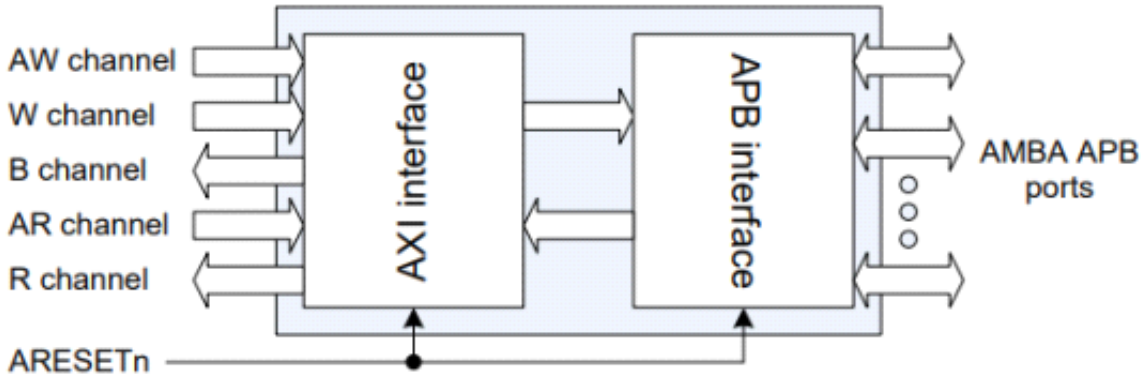
AXI-to-APB bus bridge



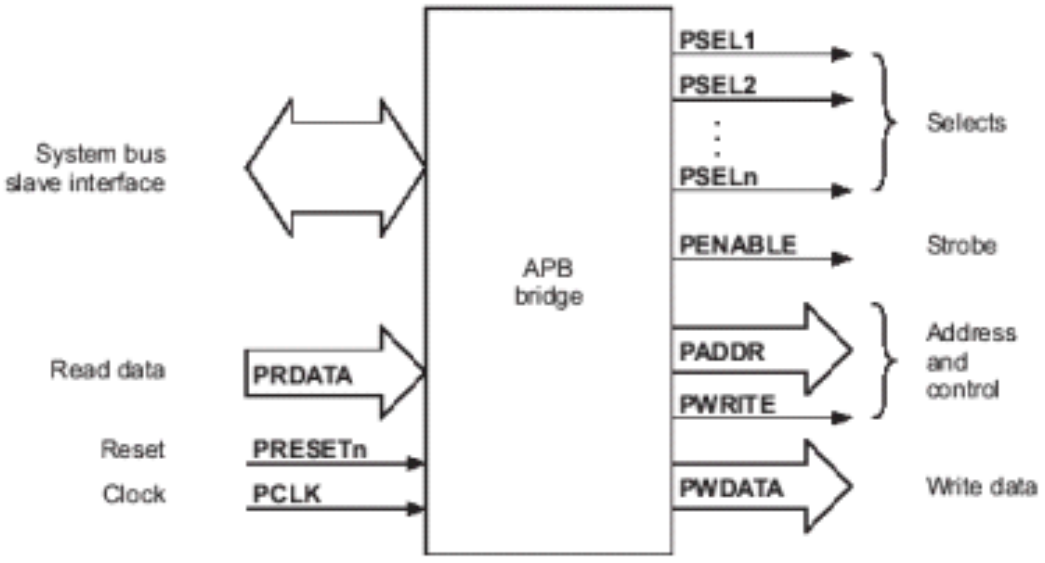
- ACLK and PCLK can be asynchronous

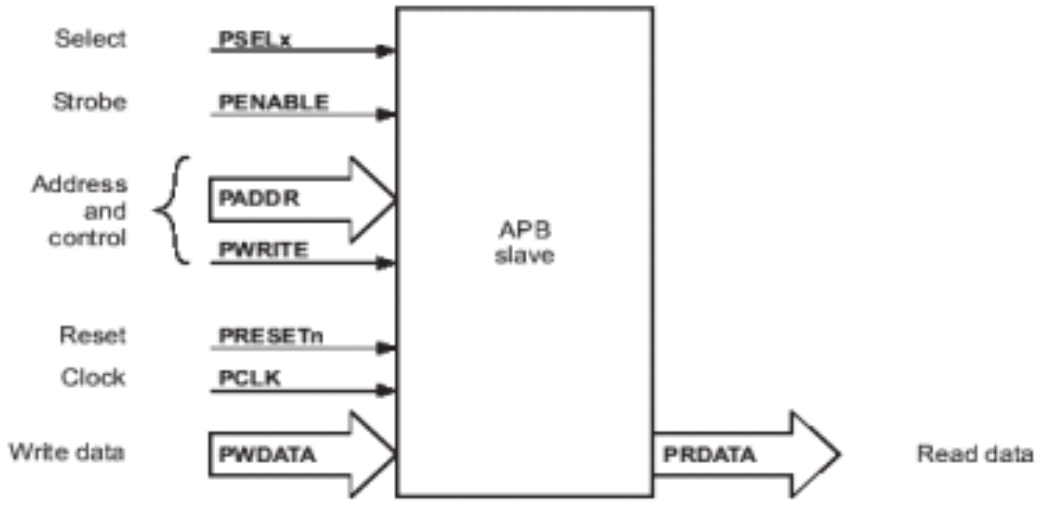


AXI-to-APB internal



Name	Description
PCLK Bus clock	The rising edge of **PCLK** is used to time all transfers on the APB.
PRESETn APB reset	The APB bus reset signal is active LOW and this signal will normally be connected directly to the system bus reset signal.
PADDR[31:0] APB address bus	This is the APB address bus, which may be up to 32-bits wide and is driven by the peripheral bus bridge unit.
PSELx APB select	A signal from the secondary decoder, within the peripheral bus bridge unit, to each peripheral bus slave x. This signal indicates that the slave device is selected and a data transfer is required. There is a **PSELx** signal for each bus slave.
PENABLE APB strobe	This strobe signal is used to time all accesses on the peripheral bus. The enable signal is used to indicate the second cycle of an APB transfer. The rising edge of **PENABLE** occurs in the middle of the APB transfer.
PWRITE APB transfer direction	When HIGH this signal indicates an APB write access and when LOW a read access.
PRDATA APB read data bus	The read data bus is driven by the selected slave during read cycles (when **PWRITE** is LOW). The read data bus can be up to 32-bits wide.
PWDATA APB write data bus	The write data bus is driven by the peripheral bus bridge unit during write cycles (when **PWRITE** is HIGH). The write data bus can be up to 32-bits wide.


System bus
slave interface
Read data
Reset
Clock
PRDATA
PRESETn
PCLK
APB
bridge
PSEL1
PSEL2
PSELn
Selects
PENABLE
Strobe
PADDR
PWRITE
Address
and
control
PWDATA
Write data


Select
Strobe
Address
and
control
Reset
Clock
Write data
PSELx
PENABLE
PADDR
PWRITE
PRESETn
PCLK
PWDATA
APB
slave
PRDATA
Read data

Protection type signals

PPROT[2:0]	Protection level
[0]	1 = privileged access 0 = normal access
[1]	1 = nonsecure access 0 = secure access
[2]	1 = instruction access 0 = data access

There is one write strobe for each eight bits of the write data bus, so **PSTRB[n]** corresponds to **PWDATA[(8n + 7):(8n)]**. Figure below shows this relationship on a 32-bit data bus.