

Jeongmin Shin

Smartphone R&D 1Team
Mobile eXperience (MX) Division, Samsung Electronics Ltd.
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EDUCATION

Ulsan National Institute of Science and Technology (UNIST) (<i>Full-Scholarship</i>)	Ulsan, South Korea
M.S. Electrical Engineering	Aug. 2022 ~ Aug. 2024
■ Advisor: Kyuho Jason Lee	
■ Research Interest: A low Power 3D point matching processor with low volume of external memory access (EMA) and on-chip data transaction	
- HW-SW co-design	
- Eliminating EMA by using memory allocation prediction schemes	
- PIM architect to support searching/clustering in-memory with low volume of on-chip data transaction	
- A low power 3D point clouds matching processor in mobile environments	
- Digital Custom IP Design	
Kwangwoon University (KW)	Seoul, South Korea
B.S, Computer Engineering	Mar. 2016 ~ Feb.2020

PROFESSIONAL EXPERIENCE

Engineer in Samsung Electronics, Mobile eXperience (MX) Division	Jul. 2024 ~ Present
■ AP technical team for Galaxy S26	
- Validation and performance analysis for Samsung LSI's AP	
Teaching Assistance in Electrical Engineering, UNIST	
■ 2022 Digital Logic and Laboratory	
- Digital circuit design in Simulation & FPGA level	
■ 2024 VLSI Design	
- Digital circuit design using Synopsys Design Compiler, IC Compiler for P&R, Samsung 28nm	
IT Specialist & Signal Officer in Republic of Korea (ROK) Army	Mar. 2020 ~ June.2022
■ IT Specialist Officer in ROK Army Logistics Command	Nov. 2020 ~ June. 2022
- Army Logistics Data Management using SQL	
■ Dispatched to ROK-US Combined Forces Command	Jul. 2021 ~ Aug. 2021
- Battle simulation in ROK-US Combined Commander Training (CCPT)	
KW-LG Electronics	
■ Internship at LG Electronics, Yangjae R&D Campus	Jan. 2019 ~ Feb. 2019
■ Industry-university Collaborative Project (KW-LG Electronics)	Oct. 2018 ~ May. 2019
- Built C software framework for a mobile web browser blocking harmful sites	

PUBLICATIONS

Journal Papers

- *C²IM-NN: A Low-power 3D Point Clouds Matching Processor with 1D-CNN Prediction and CAM-based In-memory kNN Searching*, IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
Jeongmin Shin, Hoichang Jeong, Seungbin Kim, Keonhee Park, Sangho Lee, and Kyuho Lee
- *A 701.7 TOPS/W Compute-in-Memory Processor With Time-Domain Computing for Spiking Neural Network*, IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
Keonhee Park, Hoichang Jeong, Seungbin Kim, **Jeongmin Shin**, and Kyuho Lee
- *An Energy-Efficient Processor for Real-Time Semantic LiDAR SLAM in Mobile Robots*, IEEE Journal of Solid-State Circuits (JSSC)
Jueun Jung, Seungbin Kim, Bokyoung Seo, Wuyoung Jang, Sangho Lee, **Jeongmin Shin**, Donghyeon Han, and Kyuho Jason Lee
- *HYTEC: Compact and Energy-Efficient Analog-Digital Hybrid CIM With Transpose Ternary eDRAM*, IEEE Journal of Solid-State Circuits (JSSC)
Hoichang Jeong, Seungbin Kim, **Jeongmin Shin**, and Kyuho Jason Lee

Conference Papers

- *A Low-power 3D Point Clouds Matching Processor with 1D-CNN Prediction and CAM-based In-memory kNN Searching*, 2024 IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)
Jeongmin Shin, Hoichang Jeong, Seungbin Kim, Keonhee Park, Sangho Lee, and Kyuho Lee
- *A 0.81 mJ/frame, Real-time LiDAR Odometry and Mapping Processor with Memory-efficient kNN and Reconfigurable Architecture*, 2024 IEEE European Solid-State Electronics Research Conference (ESSERC)
Seungbin Kim, Jeongmin Shin, Sangho Lee, Jueun Jung, and Kyuho Jason Lee
- *A 273.48 TOPS/W and 1.58 Mb/mm² Analog-Digital Hybrid CIM Processor with Transpose Ternary-eDRAM Bitcell*, 2024 IEEE Asian Solid-State Circuits Conference (A-SSCC)
Hoichang Jeong, Seungbin Kim, Jeongmin Shin, Keonhee Park, and Kyuho Jason Lee
- *LSPU: A Fully-Integrated Real-Time LiDAR-SLAM SoC with Point-Neural-Network Segmentation and Multi-level kNN Acceleration*, 2024 IEEE International Solid-State Circuits Conference (ISSCC)
Jueun Jung, Seungbin Kim, Bokyoung Seo, Wuyoung Jang, Sangho Lee, Jeongmin Shin, Donghyeon Han, and Kyuho Jason Lee

MAJOR RESEARCH EXPERIENCE

ML/AI Algorithm

- Online incremental learning support vector machine (an industry-university collaboration project between LG Electronics and Kwangwoon Univ.)
- Invented 1D-convolution neural network (CNN) using temporal and spatial locality in 3D point clouds to predict memory allocation through the number of points in each partitioned space (TCAS-I)
- Invented an on-chip clustering algorithm considering data distribution (TCAS-I)
- Developed an algorithm to track the memory allocation through the hash page-based memory management in every frame of LiDAR sensors (ISSCC'24)

System-on-Chip Design

- Processing in-memory (PIM) architect of 3D point matching processor with content addressable memory (CAM) based in-memory k-nearest neighbor (kNN) Searching (TCAS-I)
- System architect of 3D point matching processor with hash page-based memory management unit (ISSCC'24)
- Participated in the design of 3 MPWs (Multi Project Wafer) over 2 years
- Digital Custom IP design

Computer Architecture

- 5-stage pipeline 32-bit RISC core including full hazard handling (structural, data, and control), verification with verilog testbench simulation

AWARDS

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| ■ Demonstration Session Award, IEEE ISSCC 2024 | Feb. 2025 |
| ■ Best Student Paper Award, IEEE AICAS 2024 | April. 2024 |
| ■ Full Scholarship for Graduate Student (M.S.) | Aug. 2022 ~ Aug. 2024 |
| ■ Republic of Korea Army Headquarters Deputy Chief of Staff for Logistics Award | Dec. 2021 |
| ■ Most Improved Student Award, Software Convergence University, KW | Sep. 2018 |

SKILLS

- Programming Languages: Verilog HDL, C/C++
- EDA Tools: Synopsys Design Compiler, IC Compiler for P&R

LANGUAGES

- Competent in English