Raspberry Pi
ADC(SPI,I2C)

PMOD 전성현

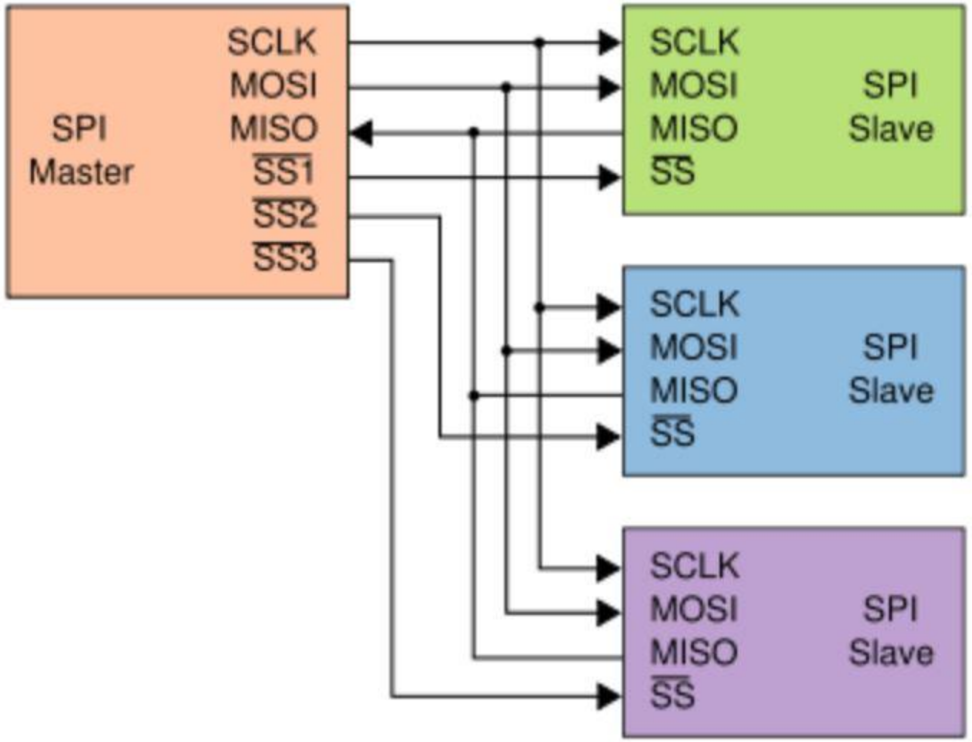
목차

SPI

- 1대 다수의 통신을 지원하는 동기식 통신 방식
- 전이중 통신방식
- 4개의 핀으로 통신(SCLK, MOSI, MISO, SS)
- I2C, UART 등 비동기식 통신 방식보다 속도가 빠름
- 마스터와 슬레이브가 존재하며 1개의 마스터에 여러 개의 슬레이브가 개별적으로 연결
- 하드웨어가 단순하지만, 노이즈에 취약하고 짧은 거리에서 동작

SPI

- SCLK : Serial Clock (output from master) (Clock 전송 신호)
- MOSI: Master Output(출력), Slave Input.(입력)
- MISO : Master Input, Slave Output.
- SS : Slave Select. (active low, master에 연결할 slave를 select)



SPI

```
pi@raspberrypi:~ $ ls -l /dev/spi*
/dev/spidev0.0
/dev/spidev0.1
```

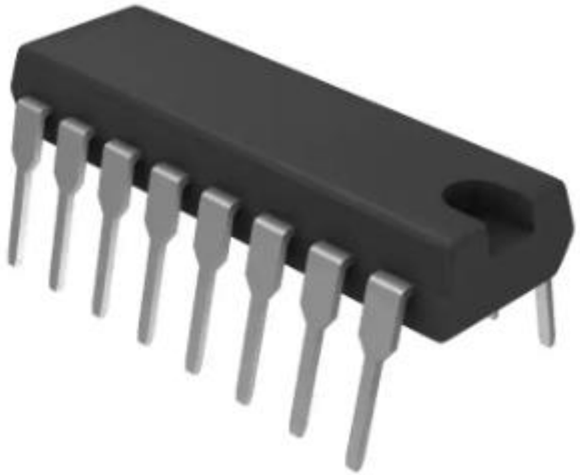
- int wiringPiSPISetup (int channel, int speed)

1. SPI 초기화
2. Channel : 채널 선택(0 or 1)
3. Speed : 속도 지정 (50kHz ~ 32MHz)

- int wiringPiSPIDataRW (int channel, unsigned char *data, int len)

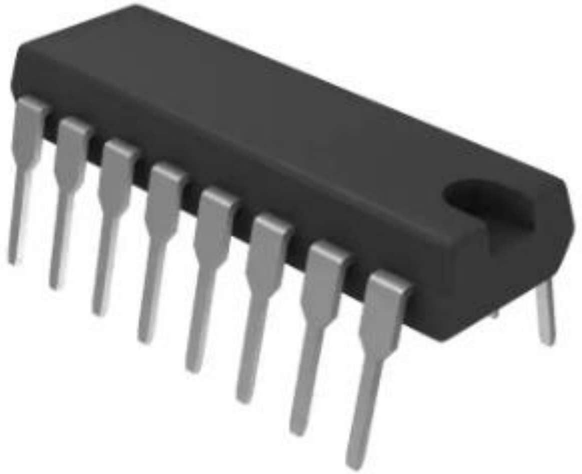
1. Read, Write 동시에 실행
2. Channel : 초기화된 채널 선택
3. *data : 3개의 byte(8비트) 버퍼에 있던 데이터가 자동으로 전송되며, 수신된 데이터는 버퍼에 덮어쓰기 된다.
4. Len : 버퍼의 크기

MCP3208-CI/P



- MCP3208은 8채널, 12비트 A/D Converter
- 라즈베리파이에는 내장된 ADC가 없어서 외부 ADC를 이용하여 센서 값을 얻을 수 있습니다.
- 라즈베리파이와 MCP3208은 SPI(serial peripheral interface) 환경에서 통신이 이루어집니다.

MCP3208-CI/P



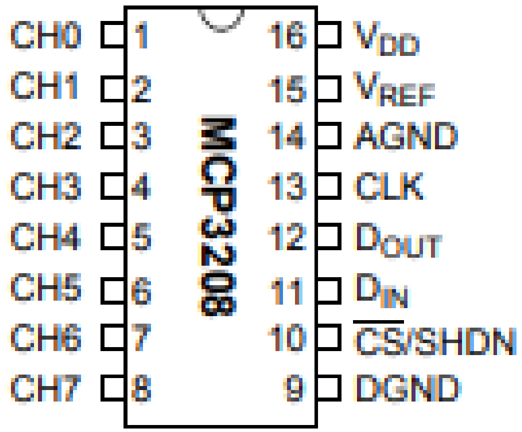
Features

- 12-bit resolution
- ± 1 LSB max DNL
- ± 1 LSB max INL (MCP3204/3208-B)
- ± 2 LSB max INL (MCP3204/3208-C)
- 4 (MCP3204) or 8 (MCP3208) input channels
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100 ksps max. sampling rate at V_{DD} = 5V
- 50 ksps max. sampling rate at V_{DD} = 2.7V
- Low power CMOS technology:
  - 500 nA typical standby current, 2 µA max.
  - 400 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- Available in PDIP, SOIC and TSSOP packages

- 12-bit 분해능
- 싱글 엔드 입력 또는 차동 입력 아날로그 입력 가능
- SPI Interface
- 단일 공급 전원 : 2.7V - 5.5V
- 샘플링 속도 : 50 ksps ~ 100 ksps
- 작동 온도 : -40도~85도
- PDIP, SOIC, TSSOP 패키지 사용가능

MCP3208-CI/P

PDIP, SOIC

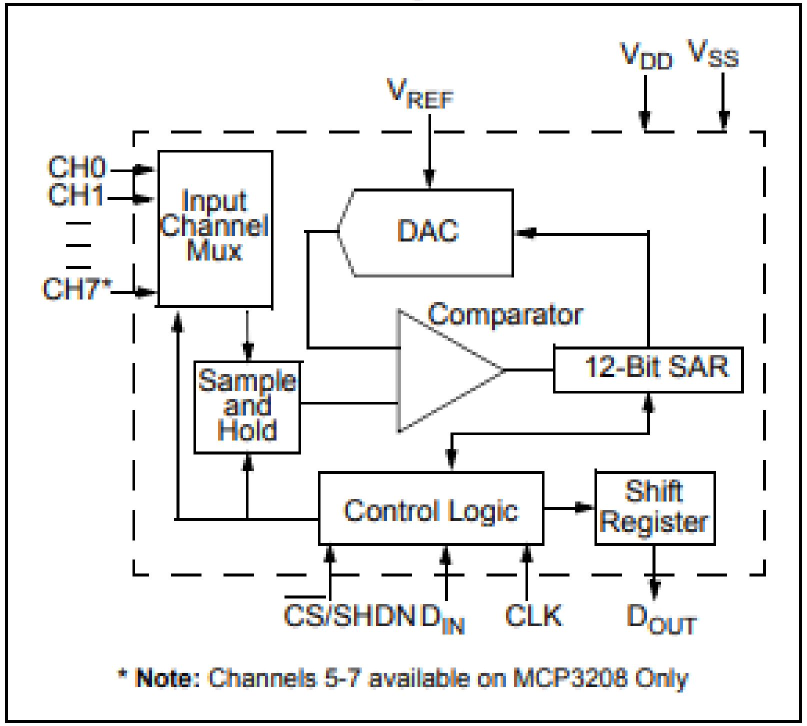


CH0	Analog Input
CH1	Analog Input
CH2	Analog Input
CH3	Analog Input
CH4	Analog Input
CH5	Analog Input
CH6	Analog Input
CH7	Analog Input

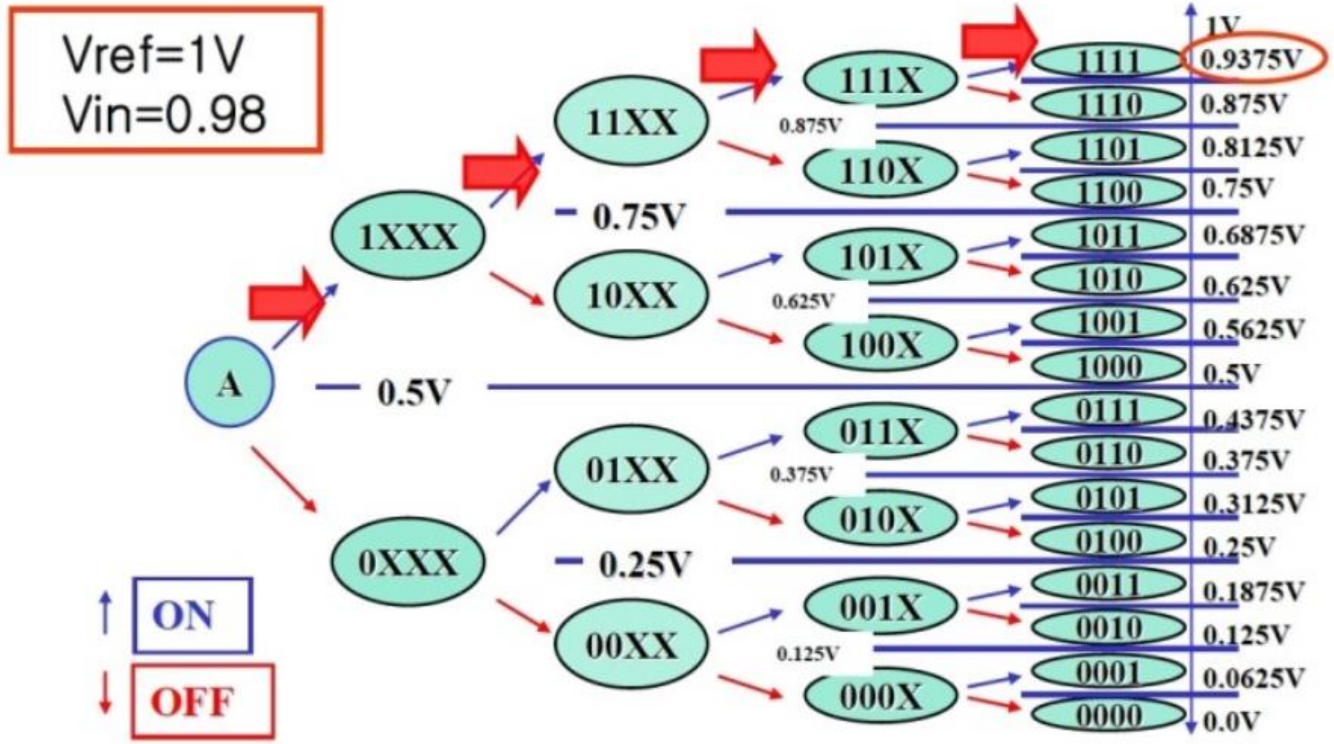
DGND	Digital Ground
$\overline{CS}$/SHDN	Chip Select/Shutdown Input
D_{IN}	Serial Data In
D_{OUT}	Serial Data Out
CLK	Serial Clock
AGND	Analog Ground
V_{REF}	Reference Voltage Input
V_{DD}	+2.7V to 5.5V Power Supply

MCP3208-CI/P

Functional Block Diagram



- SAR A/D 변환기의 개념도



MCP3208-CI/P

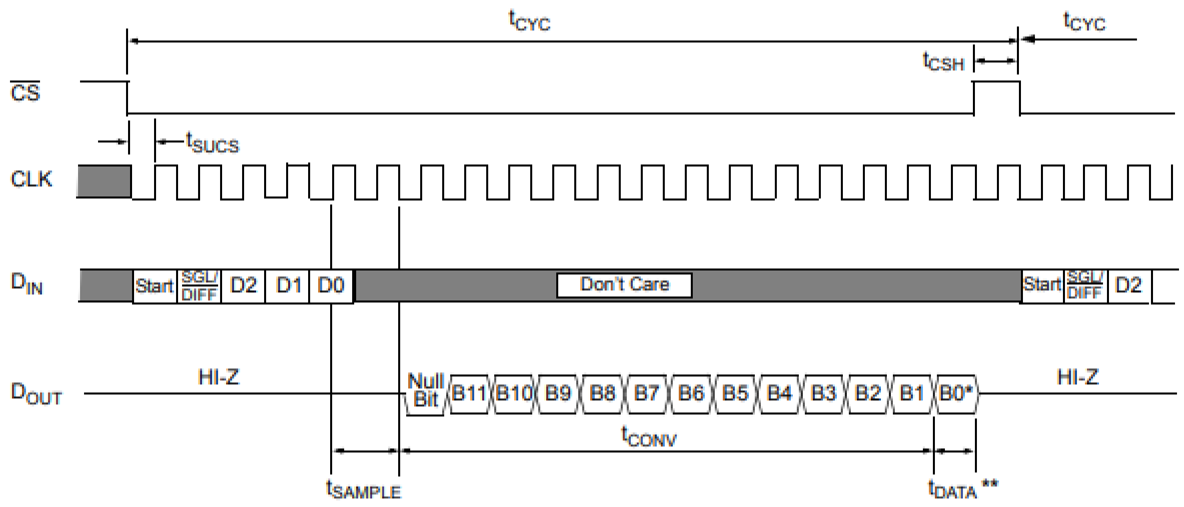
- 입력신호에 따른 작동 방식

Control Bit Selections				Input Configuration	Channel Selection
Single /Diff	D2	D1	D0		
1	0	0	0	single-ended	CH0
1	0	0	1	single-ended	CH1
1	0	1	0	single-ended	CH2
1	0	1	1	single-ended	CH3
1	1	0	0	single-ended	CH4
1	1	0	1	single-ended	CH5
1	1	1	0	single-ended	CH6
1	1	1	1	single-ended	CH7

Control Bit Selections				Input Configuration	Channel Selection
Single /Diff	D2	D1	D0		
0	0	0	0	differential	CH0 = IN+ CH1 = IN-
0	0	0	1	differential	CH0 = IN- CH1 = IN+
0	0	1	0	differential	CH2 = IN+ CH3 = IN-
0	0	1	1	differential	CH2 = IN- CH3 = IN+
0	1	0	0	differential	CH4 = IN+ CH5 = IN-
0	1	0	1	differential	CH4 = IN- CH5 = IN+
0	1	1	0	differential	CH6 = IN+ CH7 = IN-
0	1	1	1	differential	CH6 = IN- CH7 = IN+

MCP3208-CI/P

- Serial communications



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D converter will output LSB first data, followed by zeros indefinitely (see Figure 5-2 below).

** t_{DATA}: during this time, the bias current and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-1: *Communication with the MCP3204 or MCP3208.*

1. CS핀에 LOW가 입력되면 통신시작
2. D_{IN}핀으로 시작비트, 싱글입력채널/차동입력채널 선택, 채널번호(멀티플렉서 조절) 선택
3. DOUT핀으로 데이터 출력

MCP3208-CI/P

- Serial communications

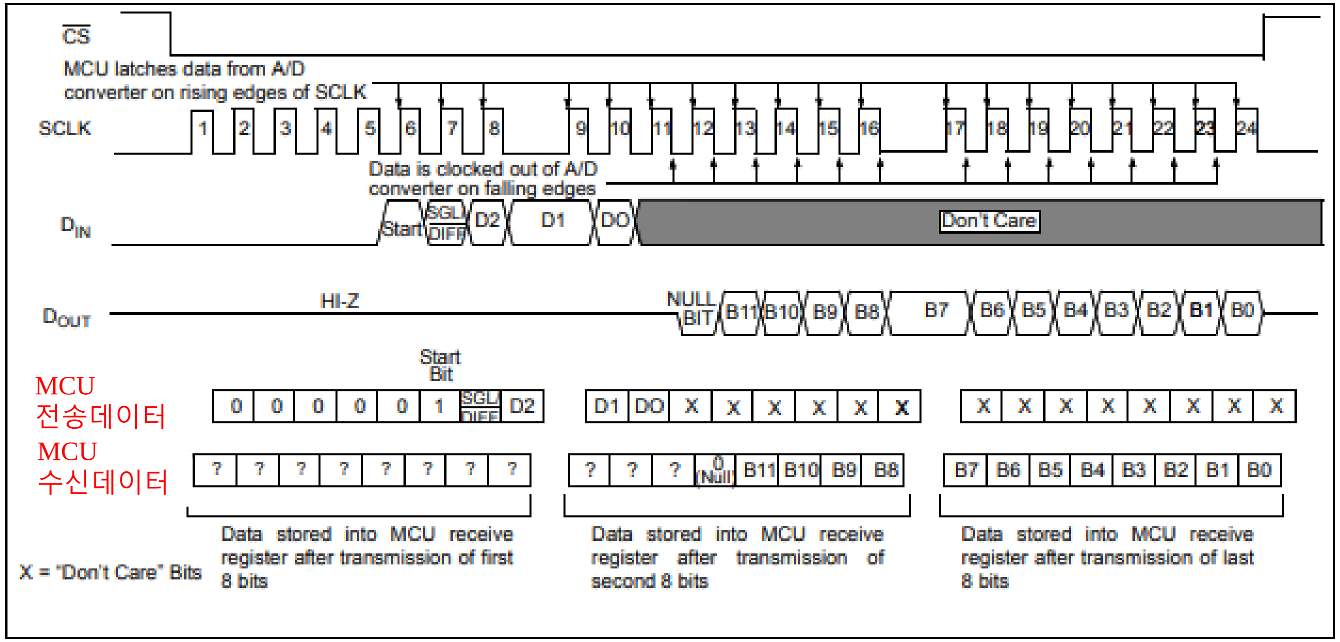


FIGURE 6-1: *SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).*

```
unsigned char buff[3];
buff[0] = 0x06 | ((adcChannel & 0x07) >> 2);
buff[1] = ((adcChannel & 0x07) << 6);
buff[2] = 0x00;
```

start　싱글 엔드 1

buff[0] = 0000 0$\boxed{1}\boxed{1}$ch(2)
buff[1] = ch(1)ch(0)00 0000
buff[2] = 0000 0000

```
digitalWrite(CS_MCP3208, 0);
wiringPiSPIDataRW(SPI_CHANNEL, buff, 3);
buff[1] = 0x0f & buff[1];
adcValue = ( buff[1] << 8) | buff[2];
digitalWrite(CS_MCP3208, 1);
```

12BIT ADC값 저장

MCP3208-CI/P

- 변환 공식

$$\text{Digital Output Code} = \frac{4096 \times V_{IN}}{V_{REF}}$$

Where:

V_{IN} = analog input voltage

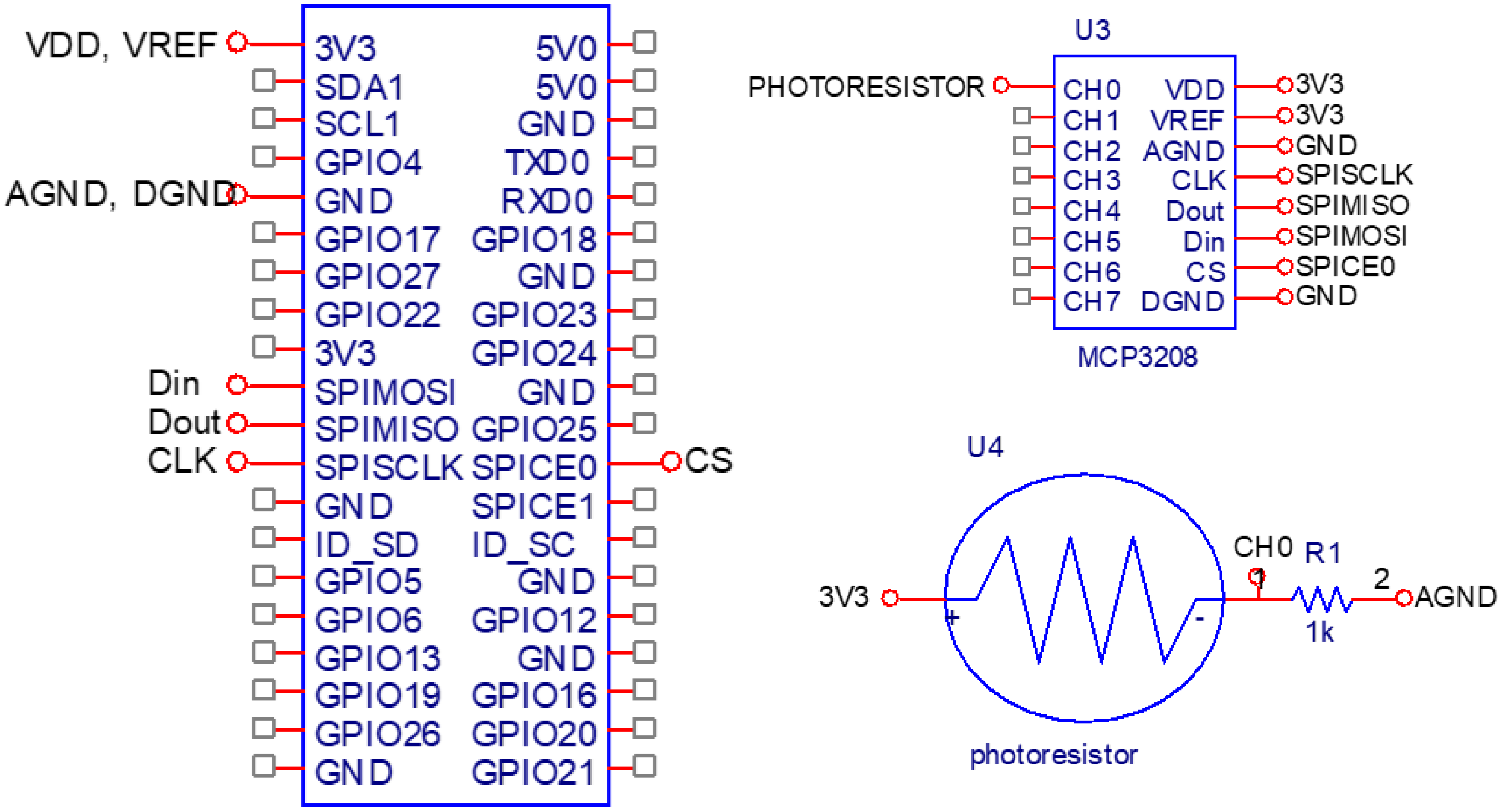
V_{REF} = reference voltage

- 동작속도

1. MCP3208은 인가되는 전압에 따라서 동작속도가 달라진다.
2. 2.7V ~ 5.5V를 입력 받을 수 있다.
3. 2.7V에서는 50ksps로 초당 50k의 샘플링이 이루어진다.
4. 5V에서는 100ksps로 초당 100k의 샘플링이 이루어진다.
5. 하나의 데이터를 수신할 때 20개의 SCLK을 사용한다.
6. 100ksps로 샘플링 할 때 인가해 주어야 하는 SPI CLK주파수는 2MHz이다.

SPI

회로도

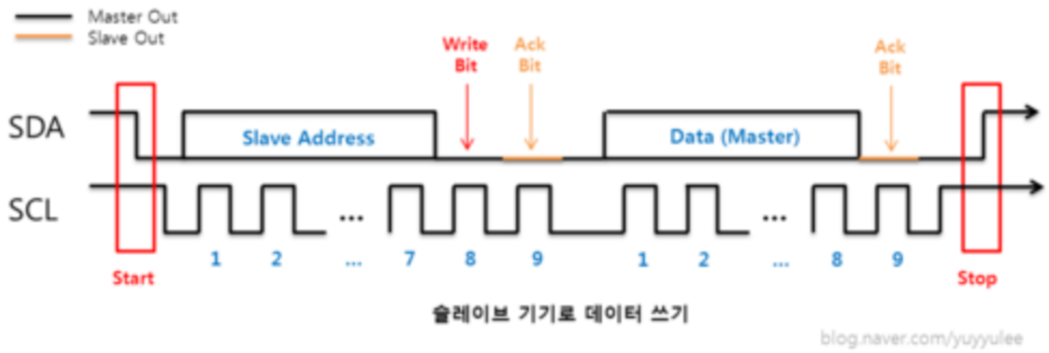


VDD, VREF
AGND, DGND
Din
Dout
CLK
CS
3V3
SDA1
SCL1
GPIO4
GND
GPIO17
GPIO27
GPIO22
3V3
SPIMOSI
SPIMISO
SPISCLK
GND
ID_SD
GPIO5
GPIO6
GPIO13
GPIO19
GPIO26
GND
5V0
5V0
GND
TXD0
RXD0
GPIO18
GND
GPIO23
GPIO24
GND
GPIO25
SPICE0
SPICE1
ID_SC
GND
GPIO12
GND
GPIO16
GPIO20
GPIO21
U3
PHOTORESISTOR
CH0 VDD 3V3
CH1 VREF 3V3
CH2 AGND GND
CH3 CLK SPISCLK
CH4 Dout SPIMISO
CH5 Din SPIMOSI
CH6 CS SPICE0
CH7 DGND GND
MCP3208
U4
3V3
+
-
CH0
R1
1
2
1k
AGND
photoresistor

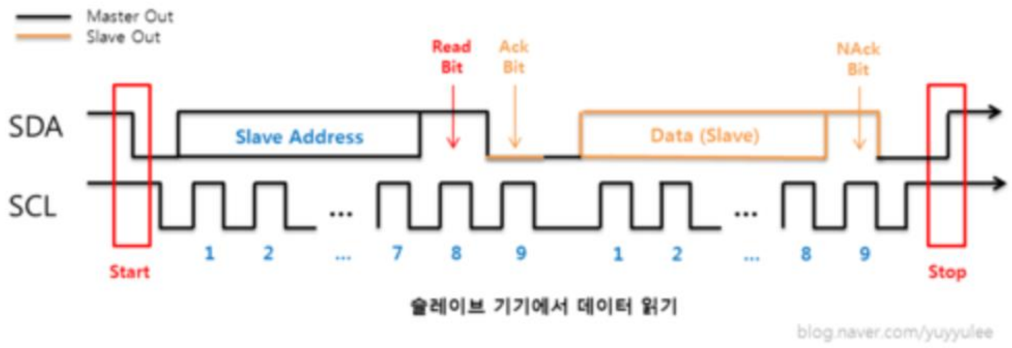
I2C

- n:n 통신을 지원하는 동기식 통신 방식
- 반이중 통신방식
- 2개의 신호선으로 통신(SCL, SDA)
- 속도가 제한적
- 마스터와 슬레이브가 존재하며 1개의 마스터에 여러 개의 슬레이브가 개별적으로 연결
- 통신방식에 의해 HIGH상태를 만들어주기 위하여 풀업 회로를 구성해 주어야 함

I2C



- SCL신호가 HIGH일 때 SDA신호가 LOW로 떨어질 때 통신 시작
- 클럭 신호에 맞춰서 슬레이브 주소 확인
- Write Bit로 쓰기모드(LOW)
- Ack Bit로 준비 완료(LOW)
- 클럭 신호에 맞춰서 데이터 쓰기
- Ack Bit로 데이터 끝 알림(LOW)
- SCL신호가 HIGH일 때 SDA신호가 HIGH로 상승할 때 통신 종료



- SCL신호가 HIGH일 때 SDA신호가 LOW로 떨어질 때 통신 시작
- 클럭 신호에 맞춰서 슬레이브 주소 확인
- Read Bit로 읽기모드(HIGH)
- Ack Bit로 준비 완료(LOW)
- 클럭 신호에 맞춰서 데이터 읽기
- Ack Bit로 데이터 끝 알림(HIGH)
- SCL신호가 HIGH일 때 SDA신호가 HIGH로 상승할 때 통신 종료

wiringPiI2C.h

- int wiringPiI2CSetup(int devld);

- int wiringPiI2CRead(int fd);

- int wiringPiI2CWrite(int fd, int data);

- int wiringPiI2CWriteReg8(int fd, int reg, int data);

- int wiringPiI2CReadReg8(int fd, int reg);

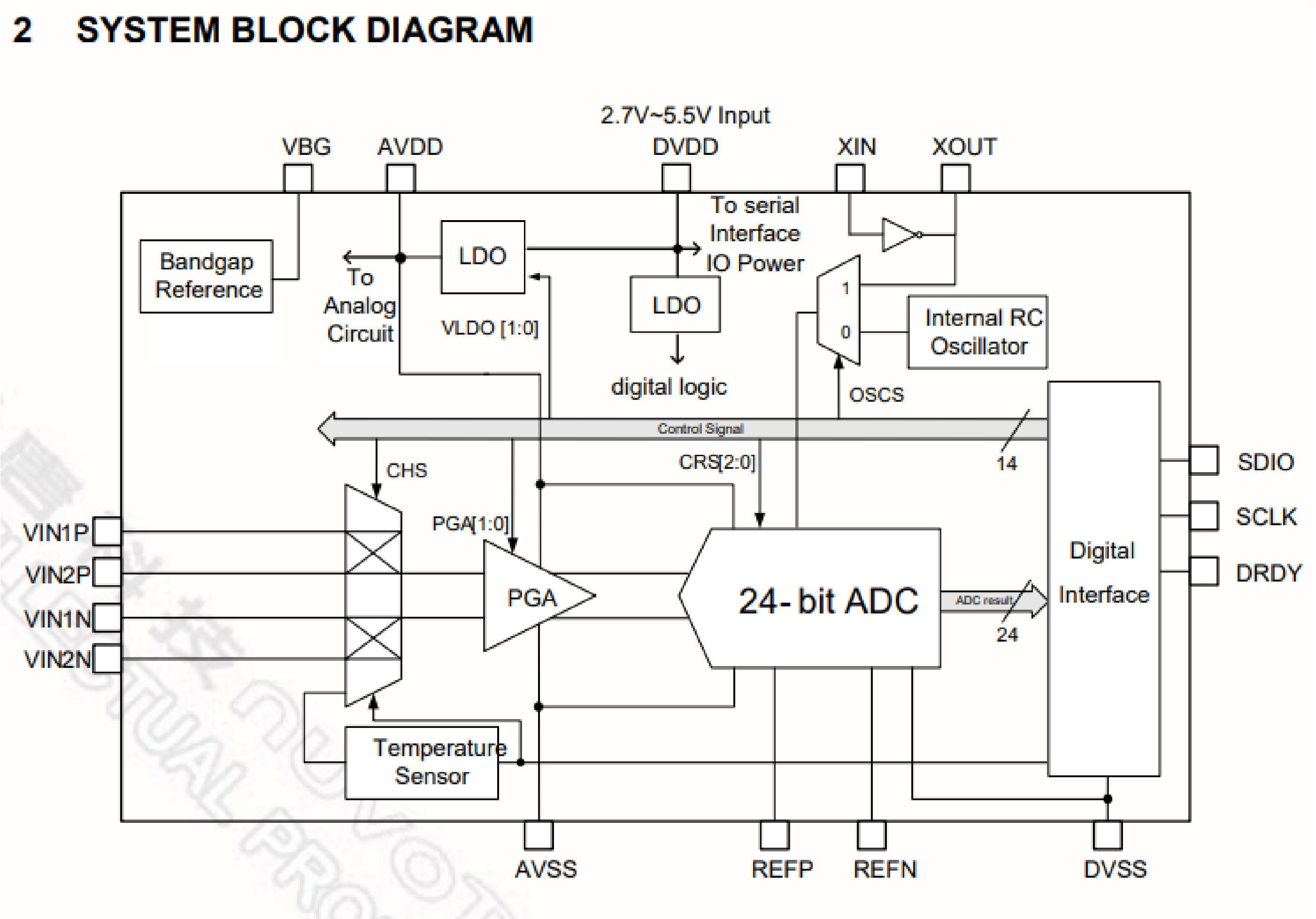
NAU7802

- NAU7802는 24비트 A/D Converter 입니다. (유효한 비트는 23비트)
- 라즈베리파이에는 내장된 ADC가 없어서 외부 ADC를 이용하여 센서 값을 얻을 수 있습니다.
- 라즈베리파이와 NAU7802은 I2C(Inter-Integrated Circuit) 인터페이스입니다.

NAU7802

- Supply Power : 2.7V ~ 5.5V
- 저전력 24-Bit ADC
- I2C Interface
- Sigma-Delta ADC
- 외부 기준 차동 입력 :0.1V ~ 5V
- System Clock : 외부 수정 발진자(4.9152Mhz) or 내부 수정 발진자(4.9152Mhz)
- 작동 온도 : -40℃ ~ 85℃
- PGA(Programmable Gain Amplifier) : 1 ~ 128
- Slave로만 동작, 표준모드(0~100Khz), 고속모드(0~400Khz)

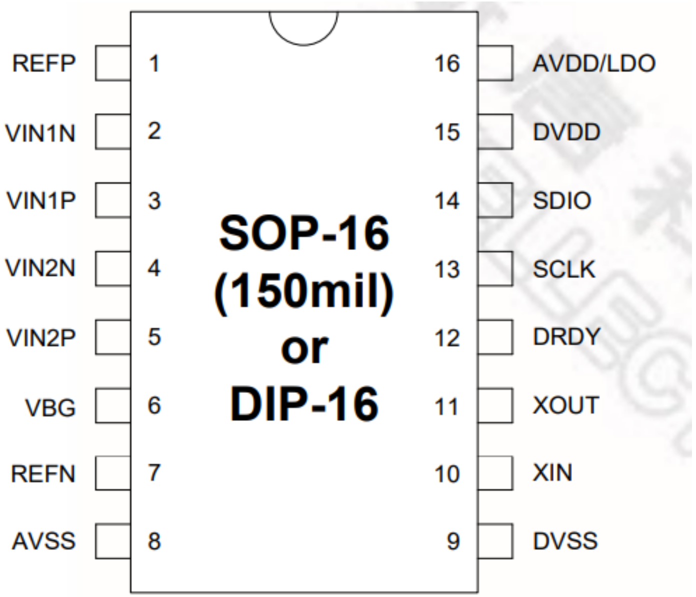
NAU7802



- Control Signal 신호에 의해서 제어
- VIN1P – VIN1N = 차동 입력 신호
- PGA에서 신호 증폭
- 24비트 ADC는 기준전압(REFP-REFN)에 의해 구동
- 내부, 외부 클럭신호 사용
- 적분형(델타시그마변조방식)변환
- 데이터 입/출력

NAU7802

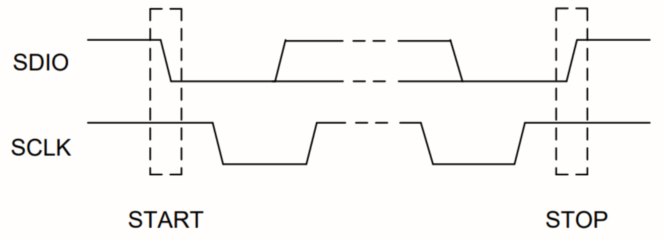
1	REFP	AI	Positive reference input
2	VIN1N	AI	Inverting Input #1
3	VIN1P	AI	Non-Inverting Input #1
4	VIN2N	AI	Inverting Input #2
5	VIN2P	AI	Non-Inverting Input #2
6	VBG	A	High impedance Reference Voltage Output and Bypass
7	REFN	AI	Negative Reference Input
8	AVSS	P	Analog Ground

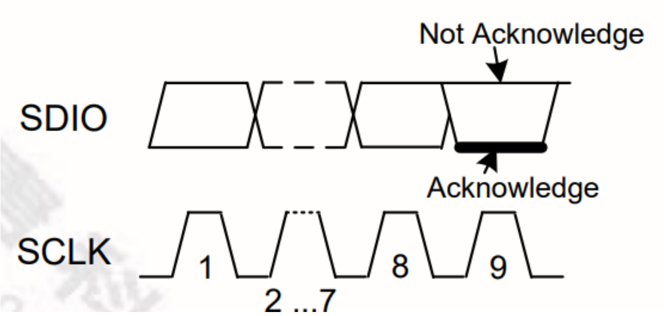


9	DVSS	P	Digital ground
10	XIN	I	External crystal oscillator input. Typically 4.9152 MHz
11	XOUT	O	External crystal oscillator output.
12	DRDY	O	Data Ready Output indicating a conversion is complete and new data are available for readout. (CMOS Driver high / low)
13	SCLK	I	Serial Data Clock Input (CMOS open drain output)
14	SDIO	I/O	Data Input / Output for serial communication with host (CMOS open drain output)
15	DVDD	P	Digital power supply: 2.7V ~ 5.5V
16	AVDD/LDO	P	Analog power supply: 1. From programmable LDO output, low ESR 1 ohm or less capacitor recommended 2. LDO off: external power supply: 2.7V ~ 5.5V

Note : **TYPE P**: Power, **AI**: Analog input, **AO**: Analog output, **I**: input, **O**: output, **I/O**: bi-directional

NAU7802

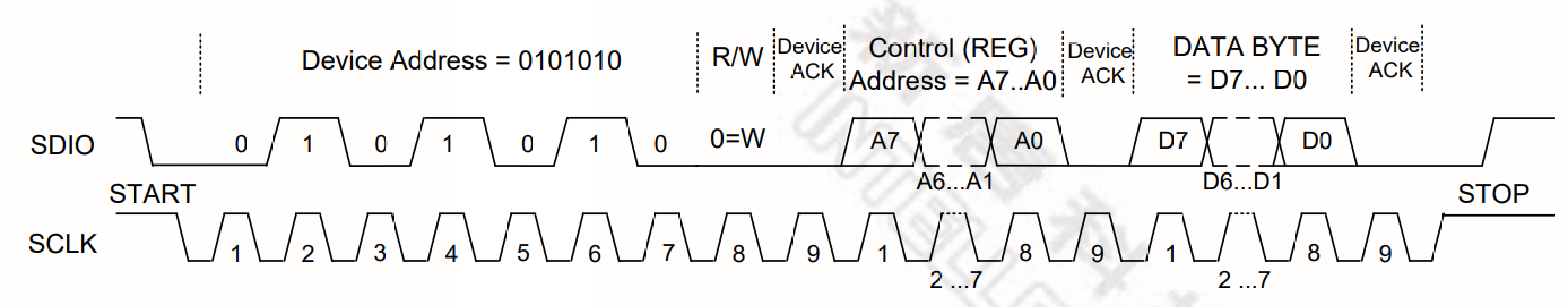




0	1	0	1	0	1	0	R/W	Device Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Figure 3: Slave Address Byte, Control Address Byte, and Data Byte

NAU7802


Device Address = 0101010
R/W
Device ACK
Control (REG) Address = A7..A0
Device ACK
DATA BYTE = D7... D0
Device ACK
SDIO
0 1 0 1 0 1 0
0=W
A7
A0
D7
D0
A6...A1
D6...D1
START
STOP
SCLK
1 2 3 4 5 6 7 8 9 1
2 ...7
8 9 1
2 ...7
8 9

I2C

NAU7802 Register Setting

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	PU_CTRL	AVDDS	OSCS	CR	CS	PUR	PUA	PUD	RR	0x00
0x01	CTRL1	CRP		VLDO[2:0]			GAINS[2:0]			0x00
0x02	CTRL2	CHS	CRS[1:0]				CALS	CALMOD[1:0]		0x00
0x03	OCAL1_B2	CH1 OFFSET Calibration[23:16]								0x00
0x04	OCAL1_B1	CH1 OFFSET Calibration[15:8]								0x00
0x05	OCAL1_B0	CH1 OFFSET Calibration[7:0]								0x00
0x06	GCAL1_B3	CH1 GAIN Calibration[31:24]								0x00
0x07	GCAL1_B2	CH1 GAIN Calibration[23:16]								0x80
0x08	GCAL1_B1	CH1 GAIN Calibration[15:8]								0x00
0x09	GCAL1_B0	CH1 GAIN Calibration[7:0]								0x00
0x0A	OCAL2_B2	CH2 OFFSET Calibration[23:16]								0x00
0x0B	OCAL2_B1	CH2 OFFSET Calibration[15:8]								0x00
0x0C	OCAL2_B0	CH2 OFFSET Calibration[7:0]								0x00
0x0D	GCAL2_B3	CH2 GAIN Calibration[31:24]								0x00
0x0E	GCAL2_B2	CH2 GAIN Calibration[23:16]								0x80
0x0F	GCAL2_B1	CH2 GAIN Calibration[15:8]								0x00
0x10	GCAL2_B0	CH2 GAIN Calibration[7:0]								0x00
0x11	I2C Control	CRSD	FDR	SPE/WPD		SI	BOPGA	TS / BGPCP		0x00
0x12	ADCO_B2	ADC_OUT[23:16]								RO
0x13	ADCO_B1	ADC_OUT[15:8]								RO
0x14	ADCO_B0	ADC_OUT[7:0]								RO
0x15	OTP_B1	OTP[15:8]								RO
0x16	OTP_B0	OTP[7:0]								RO
0x1F		Device Revision Code								RO

REG0x00:PU_CTRL

Bit	Name	Description
7	AVDDS	**AVDD source select** 1 = Internal LDO 0 = AVDD pin input (default)
6	OSCS	**System clock source select** 1 = External Crystal 0 = Internal RC oscillator (default)
5	CR	**Cycle ready** (Read only Status) 1 = ADC DATA is ready
4	CS	**Cycle start** Synchronize conversion to the rising edge of this register
3	PUR	**Power up ready** (Read Only Status) 1 = Power Up ready 0 = Power down, not ready
2	PUA	**Power up analog circuit** 1 = Power up the chip analog circuits (PUD must be 1) 0 = Power down (default)
1	PUD	**Power up digital circuit** 1 = Power up the chip digital logic 0 = power down (default)
0	RR	**Register reset** 1 = Register Reset, reset all register except RR 0 = Normal Operation (default) RR is a level trigger reset control. RR=1, enter reset state, RR=0, leave reset state back to normal state.

wiringPiI2CWriteReg8(fd, device 주소, bit data)

wiringPiI2CWriteReg8 (fd, 0x00, 0x01);

// RR(1)모든 레지스터 초기화

wiringPiI2CWriteReg8 (fd, 0x00, 0x96);

// RR(0) 표준동작, PUD(1) 디지털회로 전원 ON ,PUA(1) 아날로그회로 전원 ON,CS(1) ADC 변환시작, AVDDS(1) 내부AVDD사용

I2C

NAU7802 Register Setting

REG0x01:CTRL1

Bit	Name	Description
7	CRP	**Conversion Ready Pin Polarity (16 Pin Package Only)** 1=CRDY pin is LOW Active (Ready when 0) 0=CRDY pin is High Active(Ready when 1) (default)
6	DRDY_SEL	Select the function of DRDY pin 1: DRDY output the Buffered Crystal Clock if OSCS=1 output the internal OSC clock if OSCS= 0 0: DRDY output the conversion ready (default)
5:3	VLDO	LDO Voltage 111 = 2.4 110 = 2.7 101 = 3.0 100 = 3.3 011 = 3.6 010 = 3.9 001 = 4.2 000 = 4.5 (default)
2:0	GAINS	**Gain select** 111 = x128 110 = x64 101 = x32 100 = x16 011 =x8 010 = x4 001 = x2 000 = x1 (default)

REG0x02:CTRL2

Bit	Name	Description
7	CHS	**Analog input channel select** 1 = Ch2 0 = Ch1 (default)
6:4	CRS	**Conversion rate select** 111 = 320SPS 011 = 80SPS 010 = 40SPS 001 = 20SPS 000 = 10SPS (default)
3	CAL_ERR	Read Only calibration result 1: there is error in this calibration 0: there is no error
2	CALS	Write 1 to this bit will trigger calibration based on the selection in CALMOD[1:0] This is an "Action" register bit. When calibration is finished, it will reset to 0 While this bit is still 1, the chip is still calibrating. An I2C write to this bit will be ignored and no additional calibration will be triggered
1:0	CALMOD	11 = Gain Calibration System 10 = Offset Calibration System 01 = Reserved 00 = Offset Calibration Internal (default)

wiringPiI2CWriteReg8 (fd, 0x01, 0x11);
//VLDO 011(3.6V), 실제로 측정되는 값이 3.3V임
wiringPiI2CWriteReg8(fd, 0x02, (Channel<< 7));
//CHS(0)(default)>> CH1,CHS(1)>>CH2
wiringPiI2CWriteReg8 (fd, 0x15, 0x30);
//ADC 레지스터 부분, 클럭을 꺼짐('1')상태 설정

I2C

NAU7802 Register Setting

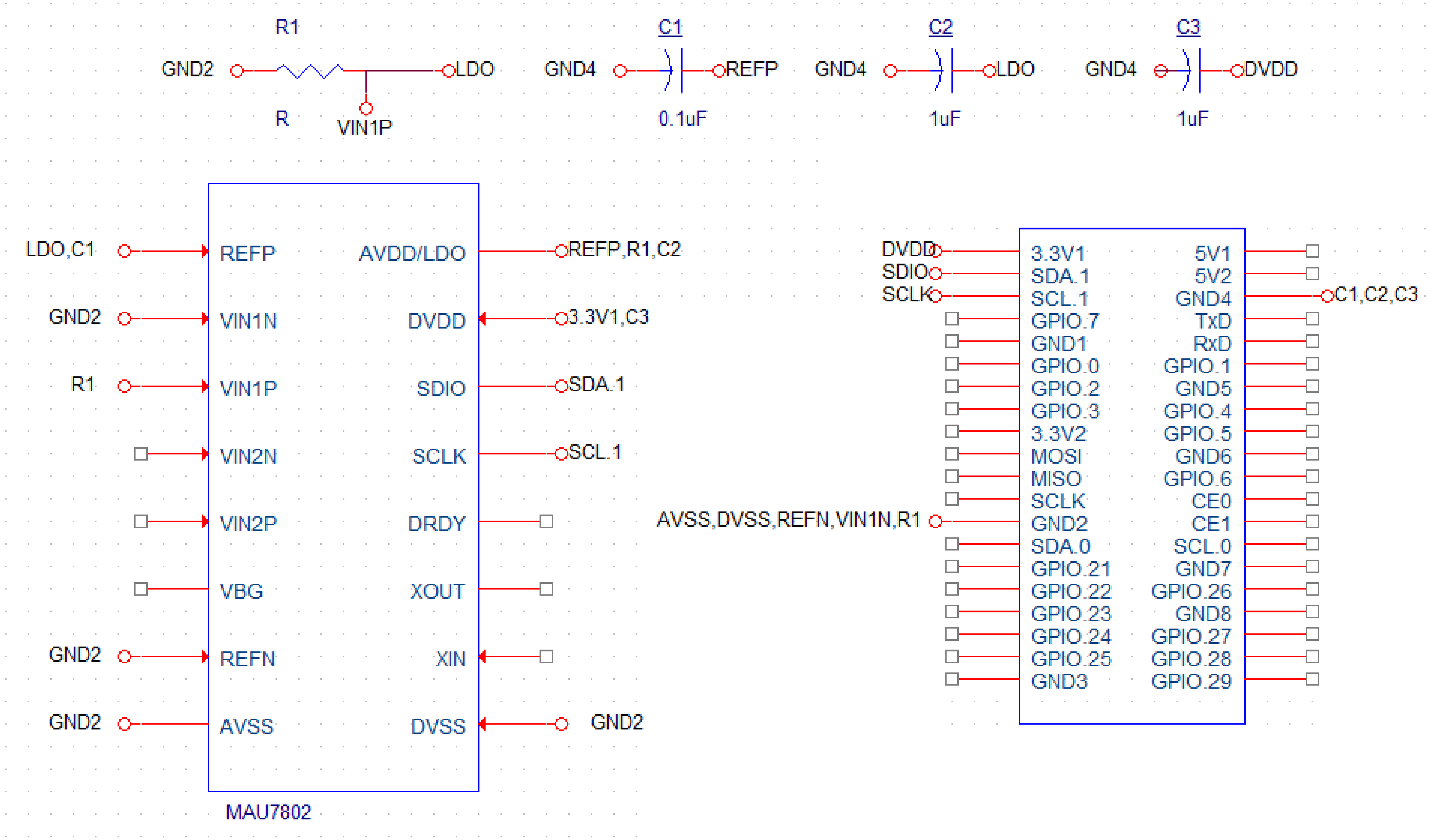
Bit	Name	Description
7	AVDDS	**AVDD source select** 1 = Internal LDO 0 = AVDD pin input (default)
6	OSCS	**System clock source select** 1 = External Crystal 0 = Internal RC oscillator (default)
5	CR	**Cycle ready** (Read only Status) 1 = ADC DATA is ready
4	CS	**Cycle start** Synchronize conversion to the rising edge of this register
3	PUR	**Power up ready** (Read Only Status) 1 = Power Up ready 0 = Power down, not ready
2	PUA	**Power up analog circuit** 1 = Power up the chip analog circuits (PUD must be 1) 0 = Power down (default)
1	PUD	**Power up digital circuit** 1 = Power up the chip digital logic 0 = power down (default)
0	RR	**Register reset** 1 = Register Reset, reset all register except RR 0 = Normal Operation (default) RR is a level trigger reset control. RR=1, enter reset state, RR=0, leave reset state back to normal state.

```
do
{
        st = wiringPiI2CReadReg8(fd,0x00);
}
while( st & 0x28 == 0x00 );
  // CR(1) ADC DATA ready, PUR(1) Power Up ready
data_H = wiringPiI2CReadReg8(fd, 0x12);
  //23:16 상위 비트  읽는 순서 중요!
data_M = wiringPiI2CReadReg8(fd, 0x13);
  //15:8 중간 비트
data_L = wiringPiI2CReadReg8(fd, 0x14);
  //7:0 하위 비트
```

11.9 REG0x12-REG0x14: ADC Conversion Result

REG0x12 (Read Only)	ADCO_B2	ADC Conversion Result bit 23 to bit 16
REG0x13 (Read Only)	ADCO_B1	ADC Conversion Result bit 15 to bit 8
REG0x14 (Read Only)	ADCO_B0	ADC Conversion Result bit 7 to bit 0

회로도


R1
GND2
LDO
R
VIN1P
C1
GND4
REFP
0.1uF
C2
GND4
LDO
1uF
C3
GND4
DVDD
1uF
LDO,C1
REFP
AVDD/LDO
REFP,R1,C2
GND2
VIN1N
DVDD
3.3V1,C3
R1
VIN1P
SDIO
SDA.1
VIN2N
SCLK
SCL.1
VIN2P
DRDY
VBG
XOUT
GND2
REFN
XIN
GND2
AVSS
DVSS
GND2
MAU7802
DVDD
SDIO
SCLK
3.3V1
SDA.1
SCL.1
GPIO.7
GND1
GPIO.0
GPIO.2
GPIO.3
3.3V2
MOSI
MISO
SCLK
GND2
SDA.0
GPIO.21
GPIO.22
GPIO.23
GPIO.24
GPIO.25
GND3
5V1
5V2
GND4
TxD
RxD
GPIO.1
GND5
GPIO.4
GPIO.5
GND6
GPIO.6
CE0
CE1
SCL.0
GND7
GPIO.26
GND8
GPIO.27
GPIO.28
GPIO.29
C1,C2,C3
AVSS,DVSS,REFN,VIN1N,R1