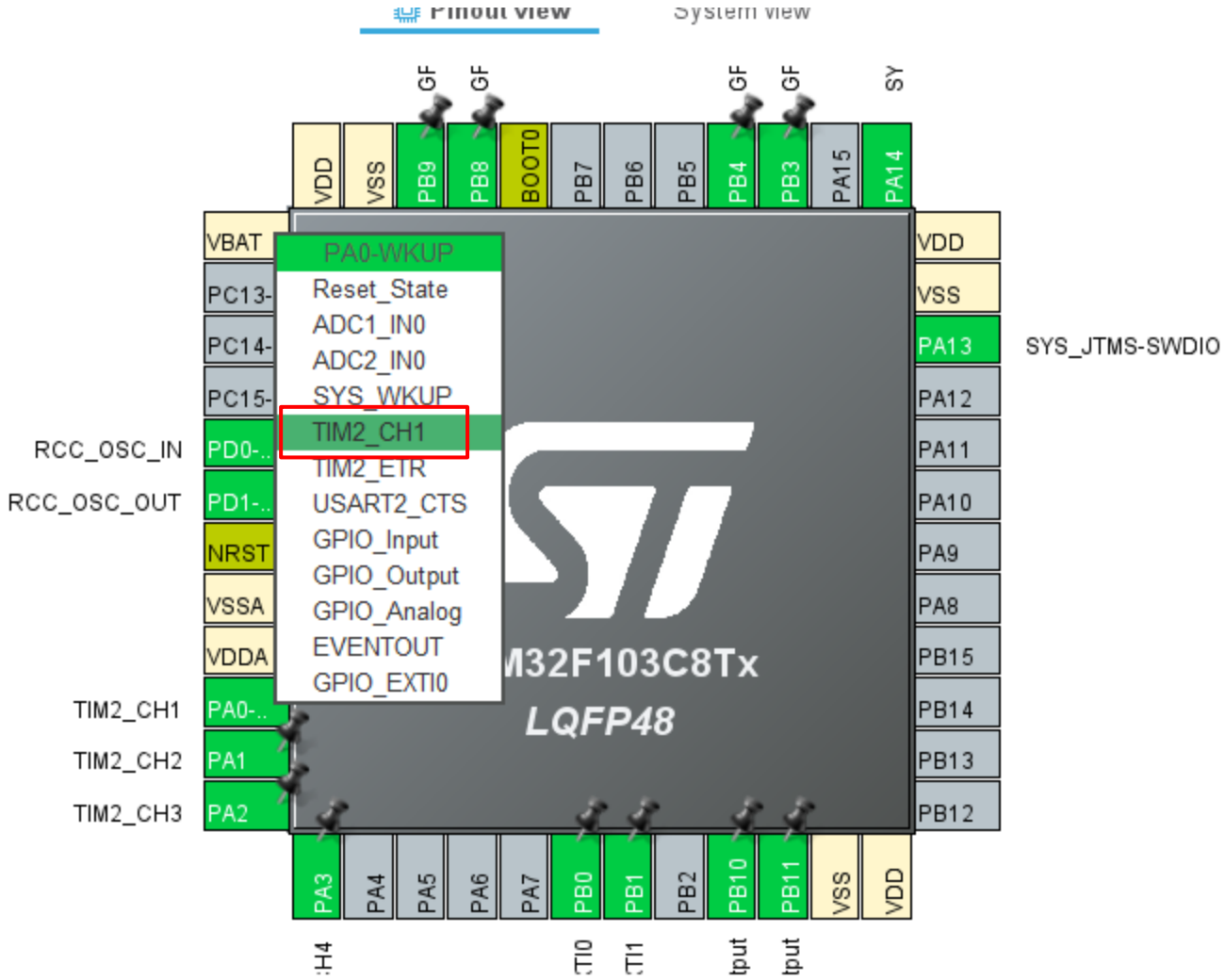
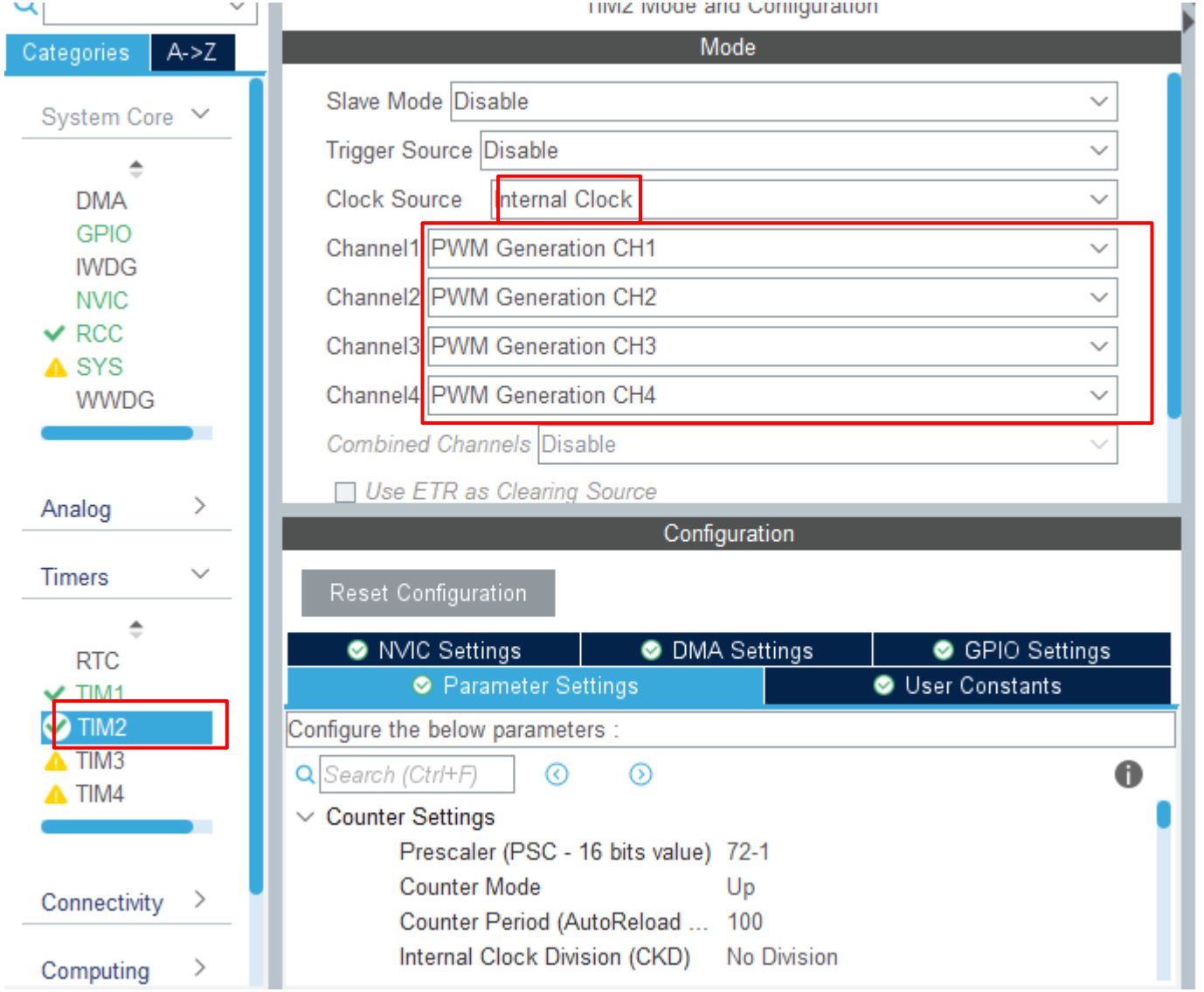
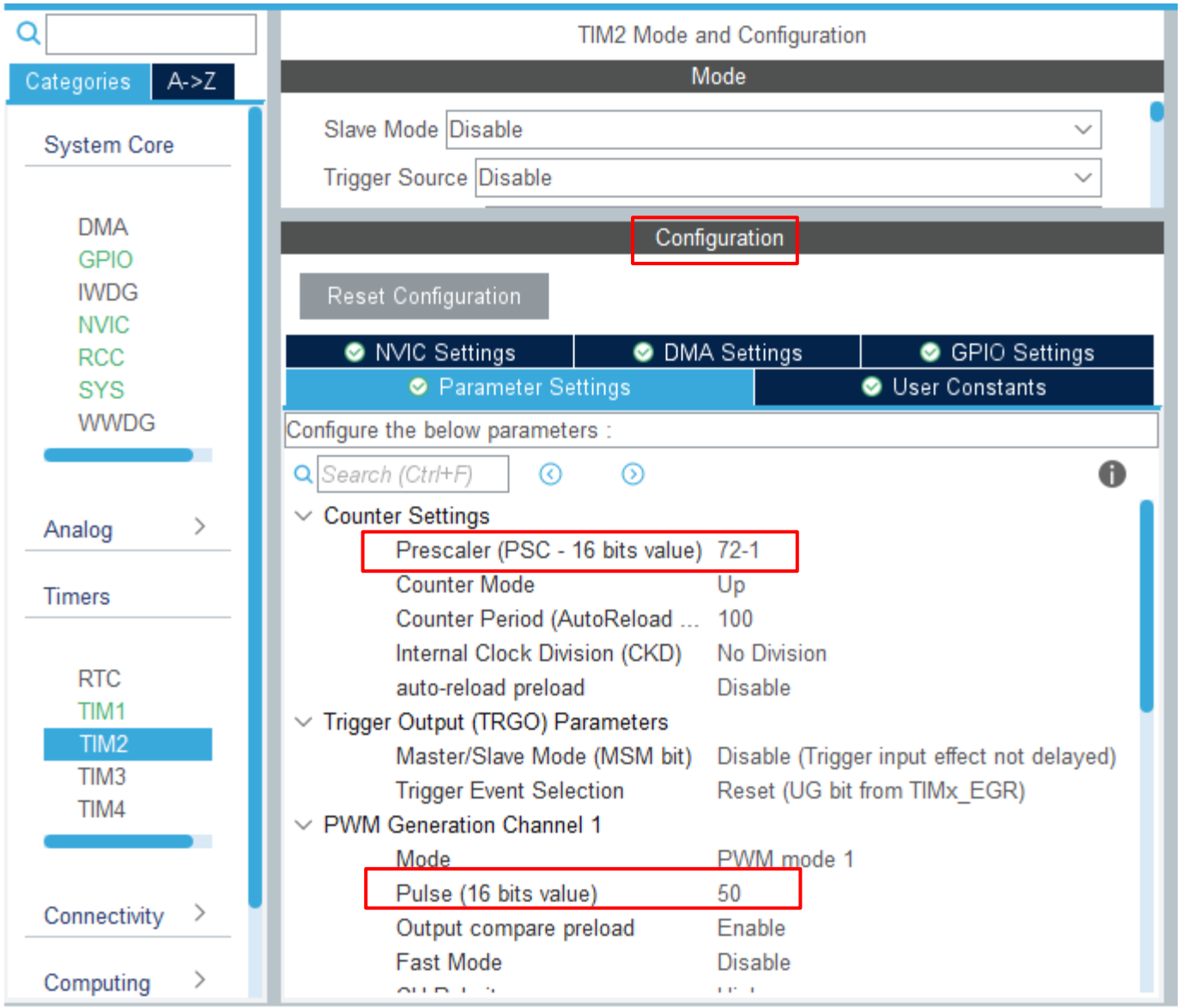
STM32 세미나
3.타이머 카운터


Pinout view
System view
VDD
VSS
PB9
PB8
BOOT0
PB7
PB6
PB5
PB4
PB3
PA15
PA14
VBAT
PC13-
PC14-
PC15-
PD0-..
PD1-..
NRST
VSSA
VDDA
PA0-..
PA1
PA2
PA0-WKUP
Reset_State
ADC1_IN0
ADC2_IN0
SYS_WKUP
TIM2_CH1
TIM2_ETR
USART2_CTS
GPIO_Input
GPIO_Output
GPIO_Analog
EVENTOUT
GPIO_EXTI0
M32F103C8Tx
LQFP48
VDD
VSS
PA13
PA12
PA11
PA10
PA9
PA8
PB15
PB14
PB13
PB12
SYS_JTMS-SWDIO
RCC_OSC_IN
RCC_OSC_OUT
TIM2_CH1
TIM2_CH2
TIM2_CH3
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB10
PB11
VSS
VDD


TIM2 Mode and Configuration
Categories
A->Z
System Core
DMA
GPIO
IWDG
NVIC
RCC
SYS
WWDG
Analog
Timers
RTC
TIM1
TIM2
TIM3
TIM4
Connectivity
Computing
Mode
Slave Mode
Disable
Trigger Source
Disable
Clock Source
Internal Clock
Channel1
PWM Generation CH1
Channel2
PWM Generation CH2
Channel3
PWM Generation CH3
Channel4
PWM Generation CH4
Combined Channels
Disable
Use ETR as Clearing Source
Configuration
Reset Configuration
NVIC Settings
DMA Settings
GPIO Settings
Parameter Settings
User Constants
Configure the below parameters :
Search (Ctrl+F)
Counter Settings
Prescaler (PSC - 16 bits value)
72-1
Counter Mode
Up
Counter Period (AutoReload ...
100
Internal Clock Division (CKD)
No Division


Categories
A->Z
System Core
DMA
GPIO
IWDG
NVIC
RCC
SYS
WWDG
Analog
Timers
RTC
TIM1
TIM2
TIM3
TIM4
Connectivity
Computing
TIM2 Mode and Configuration
Mode
Slave Mode
Disable
Trigger Source
Disable
Configuration
Reset Configuration
NVIC Settings
DMA Settings
GPIO Settings
Parameter Settings
User Constants
Configure the below parameters :
Search (Ctrl+F)
Counter Settings
Prescaler (PSC - 16 bits value)
72-1
Counter Mode
Up
Counter Period (AutoReload ...
100
Internal Clock Division (CKD)
No Division
auto-reload preload
Disable
Trigger Output (TRGO) Parameters
Master/Slave Mode (MSM bit)
Disable (Trigger input effect not delayed)
Trigger Event Selection
Reset (UG bit from TIMx_EGR)
PWM Generation Channel 1
Mode
PWM mode 1
Pulse (16 bits value)
50
Output compare preload
Enable
Fast Mode
Disable

Pinout & Configuration | Clock Configuration | Project Manager

Resolve Clock Issues

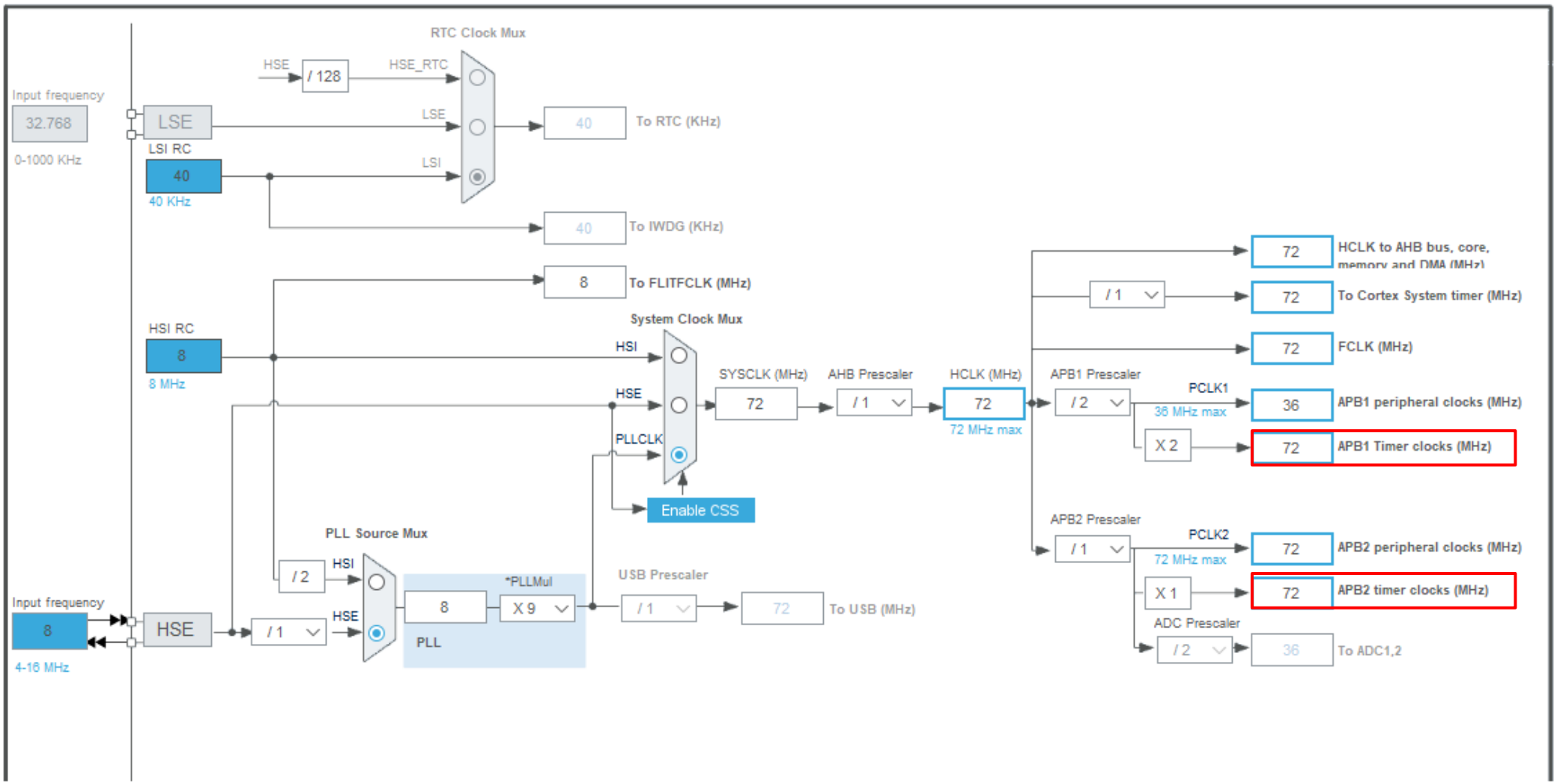


Table 19. Peripheral current consumption

Peripherals		µA/MHz
AHB (up to 72 MHz)	DMA1	16.53
	BusMatrix(1)	8.33
APB1 (up to 36 MHz)	APB1-Bridge	10.28
	TIM2	32.50
	TIM3	31.39
	TIM4	31.94
	SPI2	4.17
	USART2	12.22
	USART3	12.22
	I2C1	10.00
	I2C2	10.00
	USB	17.78
	CAN1	18.06
	WWDG	2.50
	PWR	1.67
	BKP	2.50
	IWDG	11.67

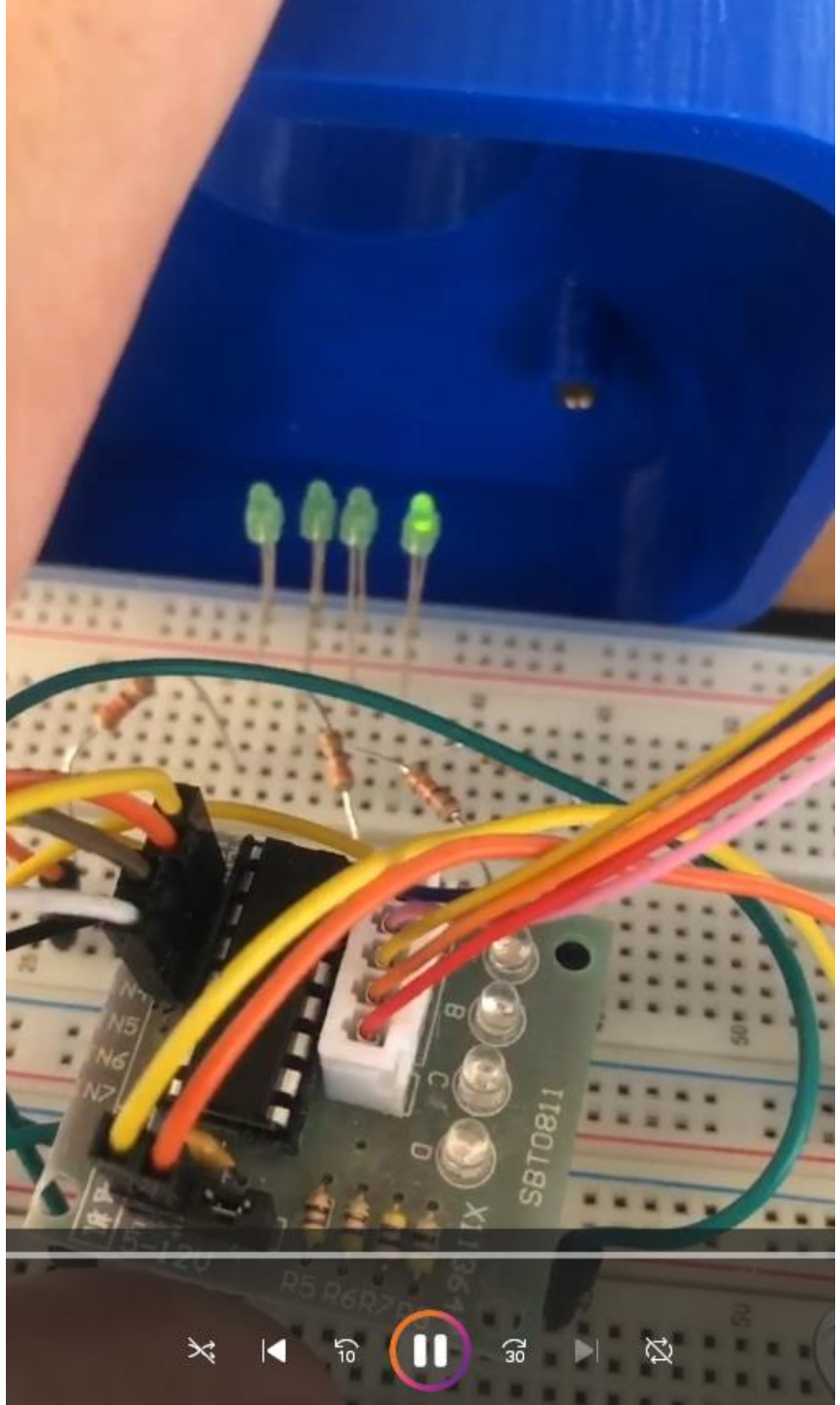
Table 19. Peripheral current consumption (continued)

Peripherals		µA/MHz
APB2 (up to 72 MHz)	APB2-Bridge	3.75
	GPIOA	6.67
	GPIOB	6.53
	GPIOC	6.53
	GPIOD	6.53
	GPIOE	6.39
	SPI1	4.72
	USART1	11.94
	TIM1	23.33
	ADC1(2)	17.50
	ADC2(2)	16.07

```
HAL_TIM_PWM_Start(&htim2, TIM_CHANNEL_1);
HAL_TIM_PWM_Start(&htim2, TIM_CHANNEL_2);
HAL_TIM_PWM_Start(&htim2, TIM_CHANNEL_3);
HAL_TIM_PWM_Start(&htim2, TIM_CHANNEL_4);
```

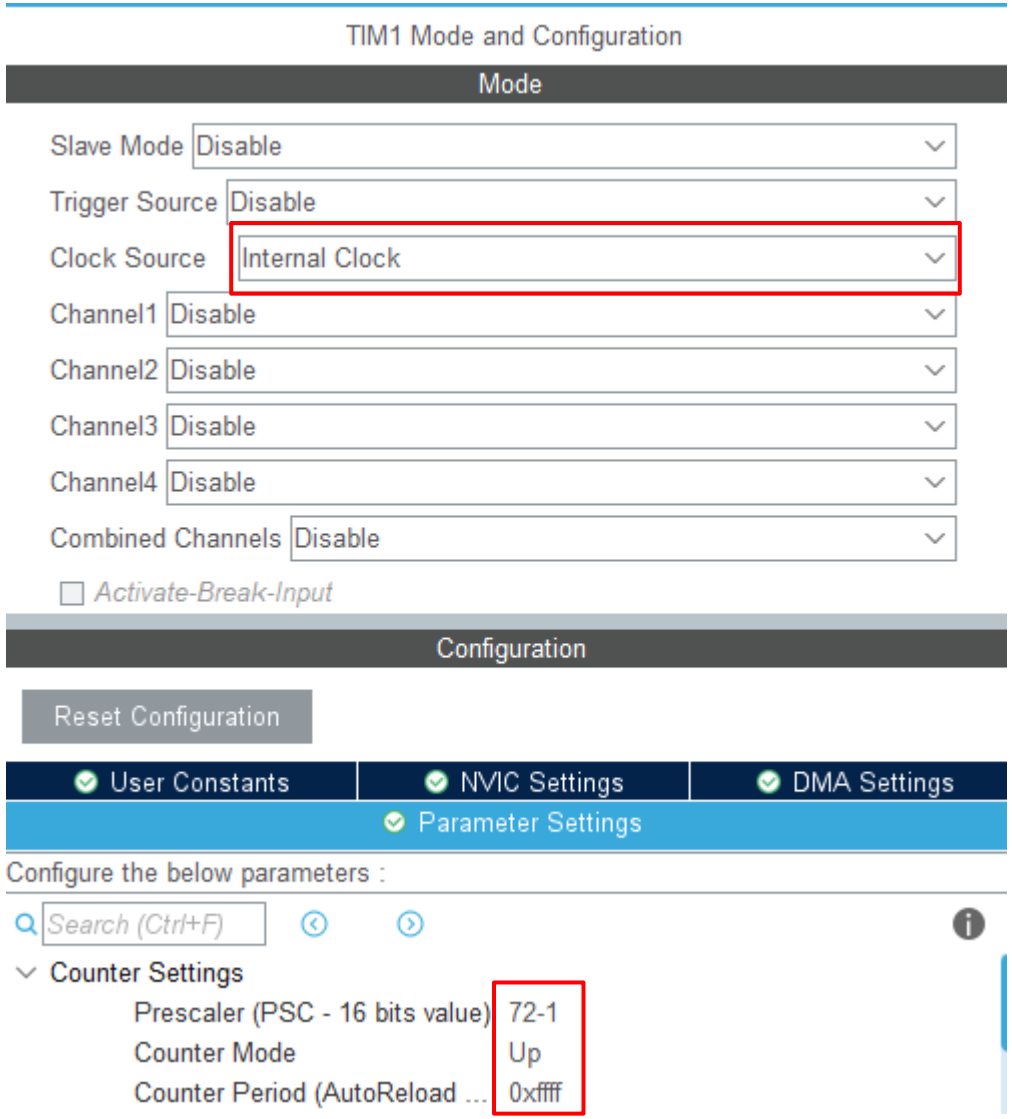
```
typedef struct
{
  __IO uint32_t CR1;             /*!< TIM control register 1,                    Address offset: 0x00 */
  __IO uint32_t CR2;             /*!< TIM control register 2,                    Address offset: 0x04 */
  __IO uint32_t SMCR;            /*!< TIM slave Mode Control register,           Address offset: 0x08 */
  __IO uint32_t DIER;            /*!< TIM DMA/interrupt enable register,         Address offset: 0x0C */
  __IO uint32_t SR;              /*!< TIM status register,                       Address offset: 0x10 */
  __IO uint32_t EGR;             /*!< TIM event generation register,             Address offset: 0x14 */
  __IO uint32_t CCMR1;           /*!< TIM  capture/compare mode register 1,      Address offset: 0x18 */
  __IO uint32_t CCMR2;           /*!< TIM  capture/compare mode register 2,      Address offset: 0x1C */
  __IO uint32_t CCER;            /*!< TIM capture/compare enable register,       Address offset: 0x20 */
  __IO uint32_t CNT;             /*!< TIM counter register,                      Address offset: 0x24 */
  __IO uint32_t PSC;             /*!< TIM prescaler register,                    Address offset: 0x28 */
  __IO uint32_t ARR;             /*!< TIM auto-reload register,                  Address offset: 0x2C */
  __IO uint32_t RCR;             /*!< TIM  repetition counter register,          Address offset: 0x30 */
  __IO uint32_t CCR1;            /*!< TIM capture/compare register 1,            Address offset: 0x34 */
  __IO uint32_t CCR2;            /*!< TIM capture/compare register 2,            Address offset: 0x38 */
  __IO uint32_t CCR3;            /*!< TIM capture/compare register 3,            Address offset: 0x3C */
  __IO uint32_t CCR4;            /*!< TIM capture/compare register 4,            Address offset: 0x40 */
  __IO uint32_t BDTR;            /*!< TIM break and dead-time register,          Address offset: 0x44 */
  __IO uint32_t DCR;             /*!< TIM DMA control register,                  Address offset: 0x48 */
  __IO uint32_t DMAR;            /*!< TIM DMA address for full transfer register, Address offset: 0x4C */
  __IO uint32_t OR;              /*!< TIM option register,                       Address offset: 0x50 */
}TIM_TypeDef;
```

```
if(a==1)htim2.Instance-> CCR4 = i;else htim2.Instance-> CCR4 = 0;
if(b==1)htim2.Instance-> CCR3 = i;else htim2.Instance-> CCR3 = 0;
if(c==1)htim2.Instance-> CCR2 = i;else htim2.Instance-> CCR2 = 0;
if(d==1)htim2.Instance-> CCR1 = i;else htim2.Instance-> CCR1 = 0;
```


SBT0811

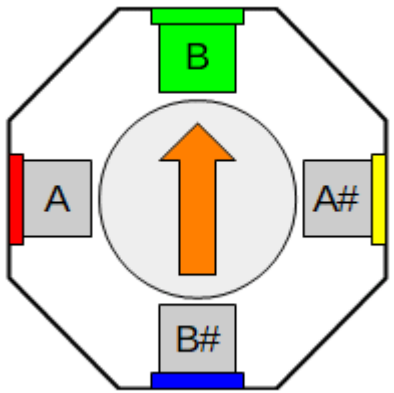
28BJY-48구동

STM32	모터드라이버
PB8	IN1
PB9	IN2
PB10	IN3
PB11	IN4


TIM1 Mode and Configuration
Mode
Slave Mode
Disable
Trigger Source
Disable
Clock Source
Internal Clock
Channel1
Disable
Channel2
Disable
Channel3
Disable
Channel4
Disable
Combined Channels
Disable
Activate-Break-Input
Configuration
Reset Configuration
User Constants
NVIC Settings
DMA Settings
Parameter Settings
Configure the below parameters :
Search (Ctrl+F)
Counter Settings
Prescaler (PSC - 16 bits value)
72-1
Counter Mode
Up
Counter Period (AutoReload ...
0xffff

스텝모터의 구동방식

- Wave Drive
- Full Drive
- Half Drive



Wave Drive Stepping Sequence				
Step	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Full Drive Stepping Sequence				
Step	A	B	C	D
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1
4	1	0	0	1

Half Drive Stepping Sequence				
Step	A	B	C	D
1	1	0	0	0
2	1	1	0	0
3	0	1	0	0
4	0	1	1	0
5	0	0	1	0
6	0	0	1	1
7	0	0	0	1
8	1	0	0	1