Mnemonic, Operands	Description	Cycles	16-Bit Instruction MSB LSB	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS					
ADDWF f,d,a	Add W and f	1	0010 01da ffff ffff	C,DC,Z,OV,N	1,2
ADDWFC f,d,a	Add W and Carry bit to f	1	0010 00da ffff ffff	C,DC,Z,OV,N	1,2
ANDWF f,d,a	AND W with f	1	0001 01da ffff ffff	Z,N	1,2
CLRF f,a	Clear f	1	0110 101a ffff ffff	Z	2
COMF f,d,a	Complement f	1	0001 11da ffff ffff	Z,N	1,2
CPFSEQ f,a	Compare f with W, skip =	1 (2 or 3)	0110 001a ffff ffff		4
CPFSGT f,a	Compare f with W, skip >	1 (2 or 3)	0110 010a ffff ffff		4
CPFSLT f,a	Compare f with W, skip <	1 (2 or 3)	0110 000a ffff ffff		1,2
DECF f,d,a	Decrement f	1	0000 01da ffff ffff	C,DC,Z,OV,N	1-4
DECFSZ f,d,a	Decrement f, Skip if 0	1 (2 or 3)	0010 11da ffff ffff		1-4
DCFSNZ f,d,a	Decrement f, Skip if Not 0	1 (2 or 3)	0100 11da ffff ffff		1,2
INCF f,d,a	Increment f	1	0010 10da ffff ffff	C,DC,Z,OV,N	1-4
INCFSZ f,d,a	Increment f, Skip if 0	1 (2 or 3)	0011 11da ffff ffff		4
INFSNZ f,d,a	Increment f, Skip if Not 0	1 (2 or 3)	0100 10da ffff ffff		1,2
IORWF f,d,a	Inclusive OR W with f	1	0001 00da ffff ffff	Z,N	1,2
MOVF f,d,a	Move f	1	0101 00da ffff ffff	Z,N	1
MOVFF f_s,f_d	Move f_s (source) 1st word to f_d (destination) 2nd word	2	1100 ffff ffff ffff / 1111 ffff ffff ffff		4
MOVWF f,a	Move W to f	1	0110 111a ffff ffff		
MULWF f,a	Multiply W with f	1	0000 001a ffff ffff		
NEGF f,a	Negate f	1	0110 110a ffff ffff	C,DC,Z,OV,N	1,2
RLCF f,d,a	Rotate Left f through Carry	1	0011 01da ffff ffff	C,Z,N	
RLNCF f,d,a	Rotate Left f (No Carry)	1	0100 01da ffff ffff	Z,N	1,2
RRCF f,d,a	Rotate Right f through Carry	1	0011 00da ffff ffff	C,Z,N	
RRNCF f,d,a	Rotate Right f (No Carry)	1	0100 00da ffff ffff	Z,N	
SETF f,a	Set f	1	0110 100a ffff ffff		
SUBFWB f,d,a	Subtract f from W w/borrow	1	0101 01da ffff ffff	C,DC,Z,OV,N	1,2
SUBWF f,d,a	Subtract W from f	1	0101 11da ffff ffff	C,DC,Z,OV,N	
SUBWFB f,d,a	Subtract W from f w/borrow	1	0101 10da ffff ffff	C,DC,Z,OV,N	1,2
SWAPF f,d,a	Swap nibbles in f	1	0011 10da ffff ffff		4
TSTFSZ f,a	Test f, skip if 0	1 (2 or 3)	0110 011a ffff ffff		1,2
XORWF f,d,a	Exclusive OR W with f	1	0001 10da ffff ffff	Z,N	
BIT-ORIENTED FILE REGISTER OPERATIONS					
BCF f,b,a	Bit Clear f	1	1001 bbba ffff ffff		1,2
BSF f,b,a	Bit Set f	1	1000 bbba ffff ffff		1,2
BTFSC f,b,a	Bit Test f, Skip if Clear	1 (2 or 3)	1011 bbba ffff ffff		3,4
BTFSS f,b,a	Bit Test f, Skip if Set	1 (2 or 3)	1010 bbba ffff ffff		3,4
BTG f,b,a	Bit Toggle f	1	0111 bbba ffff ffff		1,2

Note 1: When a PORT register is modified as a function of itself (e.g., `MOVF PORTB,1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

4: Some instructions are 2-word instructions. The second word of these instructions will be executed as a `NOP`, unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

5: If the Table Write starts the write cycle to internal memory, the write will continue until terminated.

Mnemonic, Operands	Description	Cycles	16-Bit Instruction MSB LSB	Status Affected	Notes
CONTROL OPERATIONS					
BC n	Branch if Carry	1 (2)	1110 0011 nnnn nnnn		
BN n	Branch if Negative	1 (2)	1110 0110 nnnn nnnn		
BNC n	Branch if Not Carry	1 (2)	1110 0011 nnnn nnnn		
BNN n	Branch if Not Negative	1 (2)	1110 0111 nnnn nnnn		
BNOV n	Branch if Not Overflow	1 (2)	1110 0101 nnnn nnnn		
BNZ n	Branch if Not Zero	2	1110 0001 nnnn nnnn		
BOV n	Branch if Overflow	1 (2)	1110 0100 nnnn nnnn		
BRA n	Branch Unconditionally	1 (2)	1101 0nnn nnnn nnnn		
BZ n	Branch if Zero	1 (2)	1110 0000 nnnn nnnn		
CALL n,s	Call subroutine 1st word / 2nd word	2	1110 110s kkkk kkkk / 1111 kkkk kkkk kkkk		
CLRWDT --	Clear Watchdog Timer	1	0000 0000 0000 0100	TO,PD	
DAW --	Decimal Adjust W	1	0000 0000 0000 0111	C	
GOTO n	Goto address 1st word / 2nd word	2	1110 1111 kkkk kkkk / 1111 kkkk kkkk kkkk		
NOP --	No Operation	1	0000 0000 0000 0000		
NOP --	No Operation (Note 4)	1	1111 xxxx xxxx xxxx		4
POP --	Pop top of return stack	1	0000 0000 0000 0110		
PUSH --	Push top of return stack	1	0000 0000 0000 0101		
RCALL n	Relative Call	2	1101 1nnn nnnn nnnn		
RESET	Software device RESET	1	0000 0000 1111 1111	All	
RETFIE s	Return from interrupt	2	0000 0000 0001 000s	GIE/GIEH, PEIE/GIEL	
RETLW k	Return with literal in W	2	0000 1100 kkkk kkkk		
RETURN s	Return from Subroutine	2	0000 0000 0001 001s		
SLEEP --	Go into Standby mode	1	0000 0000 0000 0011	TO,PD	
LITERAL OPERATIONS					
ADDLW k	Add literal and W	1	0000 1111 kkkk kkkk	C,DC,Z,OV,N	
ANDLW k	AND literal with W	1	0000 1011 kkkk kkkk	Z,N	
IORLW k	Inclusive OR literal with W	1	0000 1001 kkkk kkkk	Z,N	
LFSR f,k	Move literal (12-bit) 2nd word to FSRx 1st word	2	1110 1110 00ff kkkk / 1111 0000 kkkk kkkk		
MOVLB k	Move literal to BSR<3:0>	1	0000 0001 0000 kkkk		
MOVLW k	Move literal to W	1	0000 1110 kkkk kkkk		
MULLW k	Multiply literal with W	1	0000 1101 kkkk kkkk		
RETLW k	Return with literal in W	2	0000 1100 kkkk kkkk		
SUBLW k	Subtract W from literal	1	0000 1000 kkkk kkkk	C,DC,Z,OV,N	
XORLW k	Exclusive OR literal with W	1	0000 1010 kkkk kkkk	Z,N	
DATA MEMORY <-> OPERATIONS					
TBLRD *	Table Read	2	0000 0000 0000 1000		
TBLRD *+	Table Read post-increment		0000 0000 0000 1001		
TBLRD *-	Table Read post-decrement		0000 0000 0000 1010		
TBLRD +*	Table Read pre-increment		0000 0000 0000 1011		
TBLWT *	Table Write	2	0000 0000 0000 1100		5
TBLWT *+	Table Write post-increment		0000 0000 0000 1101		
TBLWT *-	Table Write post-decrement		0000 0000 0000 1110		
TBLWT +*	Table Write pre-increment		0000 0000 0000 1111		

f = 8-bit register file address
d = destination, W (0) or f (1)
a = access bit, (0) access bank or (1) bank selected by BSR
b = bit address within an 8-bit file register

W = WREG (accumulator)
k = literal, constant, or label
x = don't care
n = relative address (branch) or a direct address
s = Fast Call/Return select bit (0) normal, (1) fast mode

C = Carry Status bit
DC = Digit Carry Status bit
Z = Zero Status bit
OV = Overflow Status bit
N = Negative Status bit
TO = Time-out bit
PO = Power-down bit