Jacob Peake

Portfolio

GitHub Profile
LinkedIn Profile

Education

Imperial College London Oct 2021 - Jun 2025
Master of Engineering, Computer Engineering MEng

Winstanley College Sep 2019 - Jun 2021
A-Levels: Mathematics(A) Physics(A*) Further Mathematics(A) Extended Project(A*)*

Experience

Karman Space Programme Feb 2023 - Present
Avionics Engineer *Part-Time*

- Designing & Implementing the Avionics System for the first non-commercial, non-governmental reusable rocket to space.
- Leading Software Development with C++, C, FreeRTOS, & STM32 to meet high-performance, low-power, real-time requirements - and implementing a Novel Dual-Modular Redundant System Architecture to provide robustness.
- Leading the integration of Software, Hardware, Control & Telemetry Systems to produce an elegant, coherent, solution.
- Collaborating with Leading Experts (such as European Space Agency), & creating 150-page Technical Design Reviews.

Qualcomm Jul 2023 - Sept 2023
Firmware Engineer *Internship*

- Developing Platform Firmware for the Latest Qualcomm Bluetooth Audio SoC - with significant C Embedded Firmware Development & Development of Automated Test Scripts in Python to validate functionality.
- Communicating within a small team & wider organisation to establish additional functionalities for the SoC.
- Contributing towards the continuous development of the department's processes, capturing system requirements, defining tasks, maintaining relevant design documentation, and translating requirements into software implementation.

Projects

Autonomous Pathfinder Robot (A)
C++, SystemVerilog, FPGA, HTML, CSS, JavaScript

- Designed an Autonomous Pathfinder Robot that navigated & mapped a compex maze - calculating the shortest path from a set start to end point.
- Implemented an in-hardware Vision System (FPGA & SystemVerilog) that detected the maze markings & beacons to enable active obstacle avoidance and triangulate position, along with Dead-Reckoning.
- Developed a Web-Application that displayed the maze representation & communicated with a server & database to store mapping data & send real-time commands.

C Compiler (A)
C++, RISC-V, Lex/Flex, Yacc/Bison

- Designed a C Compiler in C++ that takes C as its source and produces RISC-V assembly as its target language.
- Used Test Scripts of increasing complexity to verify design decisions and ensure correct functionality throughout the development process, as more features added to Lexer, Parser, & Code Generator.
- Managed development using a tracking system to define milestones, give a week-by-week plan and log updates, assessing the estimates given and adjusting accordingly.

RISC-V CPU (A)
SystemVerilog, C++, RTL Design

- Designed a multi-stage pipelined RISC-V processor.
- Wrote C++ testbenches and used a cycle-accurate behavioural model to verify digital hardware.
- Coordinated Development Methodology & allocated tasks & resources to team members to ensure structured approach taken - to meet timing deadlines.

FPGA IoT System (A+)
FPGA, C, Python, Verilog

- Developed an IoT system with multiple FPGA nodes that processes data captured by an accelerometer and interacts with a cloud server to exchange information.
- Used IoT system and PyGame to implement a 'Mario Kart' style game - using FPGA nodes as controllers, using cloud server to sync data between players and storing player information in a NoSQL database.

Webpage Portfolio Design
HTML, CSS, JavaScript, React

- Developed a portfolio website to introduce myself and share my projects, experiences, & thoughts.

Technologies

- **Languages**: C++, C, Python, SystemVerilog, HTML/CSS, JavaScript, MATLAB, SQL *(in order of competency)*
- **Technologies**: FreeRTOS, Embedded Systems, Microcontrollers, STM32, RISC-V, FPGA, Quartus Prime, PyTorch, OpenCV, Unix, Lex/Flex, Yacc/Bison, GCC, LLVM, LaTeX, Git, Perforce
- **Relevant Modules**: Instruction Architectures and Compilers, Information Processing, Software Systems, Discrete Mathematics, Digital & Computer Architecture, Advanced Computer Architecture, Machine Learning