Jacob Peake

https://www.linkedin.com/in/jacob-peake/

Email : jacob.peake21@imperial.ac.uk

Mobile : +44-7956-968583

Education

- **Imperial College London** Oct 2021 - Jun 2025
  Master of Engineering, Computer Engineering MEng
- **Winstanley College** Sep 2019 - Jun 2021
  A-Levels: Mathematics(A) Physics(A*) Further Mathematics(A) Extended Project(A*)*

Experience

- **Qualcomm** Jul 2023 - Sept 2023
  Software Engineer *Internship*
  - Developing Platform Software for the Latest Voice & Music SoC - with significant C & Python development.
  - Contributing towards the continuous development of the department's processes, capturing system requirements, defining tasks, maintaining relevant documentation, and participating in design reviews.
  - Communicating within a small team & wider organisation to establish additional functionalities for the SoC.
- **Karman Space Programme** Feb 2023 - Present
  Avionics Engineer
  - Designing the Avionics System to be implemented into Vega & Aurora Spaceshot Rockets - aiming to be the first student-led team to reach space (100km) with a fully-reusable rocket.
  - Designing, Building & Testing the System Architecture, Sensor System, Telemetry Communication, Guidance, Navigation and Control System, Power Distribution, Camera System, & Software.
  - Producing a Conceptual Design Review, Preliminary Design Review & other academic research literature.

Relevant Projects

- **Autonomous Pathfinder Robot**
  C++, FPGA, HTML, CSS, JavaScript
  - Designed an Autonomous Pathfinder Robot that navigated & mapped a maze - calculating the shortest path from start to end-point.
  - Implemented an in-hardware Vision System (FPGA) that detected the white-maze markings & coloured beacons to enable active obstacle avoidance and triangulate position, along with IMU Dead-Reckoning.
  - Developed a Web-Application that displayed the maze representation & communicated with a server & database to store mapping data & send real-time commands to the robot.
- **C Compiler**
  C++, RISC-V, Flex, Yacc, Bison
  - Designed a C Compiler in C++ that takes C as its source and produces RISC-V assembly as its target language.
  - Used Test Scripts of increasing complexity to verify design decisions and ensure correct functionality throughout the development process, as more features added.
  - Managed development using a tracking system to define milestones, give a week-by-week plan and log updates, assessing the estimates given for reaching milestones and making adjustments accordingly.

- **RISC-V CPU**
  SystemVerilog, C++, RTL Design
  - Designed a multi-stage pipelined processor compliant to the RISC-V ISA using SystemVerilog.
  - Wrote C++ testbenches to verify correctness of digital hardware and used digital design tools such as Verilator and gtkWave to design functionality.
  - Coordinated Development Methodology & allocated tasks & resources to team members to ensure structured approach taken - to meet timing deadlines.
- **FPGA IoT System**
  FPGA, C, Python, Verilog
  - Developed an IoT system with multiple FPGA nodes that processes data captured by an accelerometer and interacts with a cloud server to exchange information.
  - Used IoT system and PyGame to implement a 'Mario Kart' style game- using FPGA nodes as controllers, using cloud server to sync data between players and storing player information in a NoSQL database.
  - Collaborating with 5 fellow peers, ensured progress and developments logged in an orderly fashion, ensured code was version controlled using GitHub and held regular meetings to discuss progress and delegate tasks.
- **Vega Avionics System**
  C++, C, Design
  - Developed the System Architecture, Software, Control System & contributed to the Conceptual Design of the Telemetry System and Camera System.
  - Created a structured testing & prototyping methodology, coordinated with other team members, and presented a Launch Day Protocol to be following before and during vehicle operation.
  - Produced a Conceptual & Preliminary Design Review - which each were presented to a panel of experts within the space industry - allowing critical feedback such that the iterative design process could be followed.
- **Webpage Portfolio Design**
  HTML, CSS, JavaScript
  - Developed a simple porfolio website using HTML, CSS, & Javascript to share my projects, experience, & thoughts.

Technologies

- **Languages**:
  C++, C *(advanced)*
  Python, SystemVerilog, HTML, CSS, Javascript, MATLAB, SQL *(intermediate)*
- **Technologies**: RISC-V, PyTorch, OpenCV, FPGA, Quartus Prime, Unix, Git, Perforce, Jira, LaTeX
- **Skills**: Report & Documentation Writing, Design Process & Design Review Writing, Software Development, Communication, Leadership & Management
- **Relevant Modules**: Instruction Architectures and Compilers, Information Processing, Software Systems, Discrete Mathematics, Programming For Engineers, Digital and Computer Architecture