STM32U5 Nucleo-144 board (MB1549)

Introduction

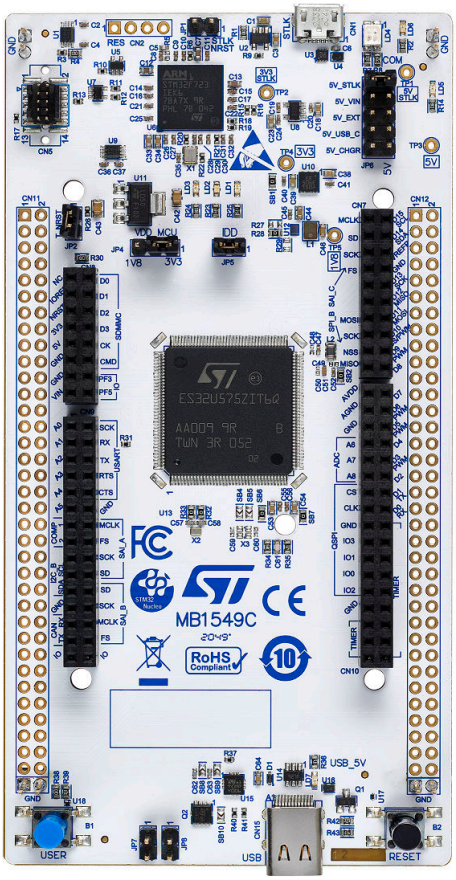
The STM32U5 Nucleo-144 board based on the MB1549 reference board (order codes NUCLEO-U575ZI-Q and NUCLEO-U5A5ZJ-Q) provides an affordable and flexible way for users to try out new concepts and build prototypes by choosing from the various combinations of performance and power-consumption features, provided by the STM32U5 microcontroller.

The ST Zio connector, which extends the ARDUINO® Uno V3 connectivity, and the ST morpho headers provide easy expansion of the functionality of the STM32 Nucleo open development platform with a wide choice of specialized shields.

The STM32U5 Nucleo-144 board does not require any separate probe as it integrates the STLINK-V3E debugger/programmer.

The STM32U5 Nucleo-144 board comes with the STM32 comprehensive free software libraries and examples available with the STM32CubeU5 MCU Package.

Figure 1. STM32U5 Nucleo-144 board



Picture is not contractual.

1 Features

- STM32U5 series microcontroller (Arm® Cortex®-M33 at 160 MHz) in an LQFP144 package
- Internal SMPS to generate V_{core} logic supply, identified by '-Q' suffixed boards(1)
- USB Type-C® sink device FS or HS depending on the microcontroller
- Three user LEDs
- RESET and USER push-buttons
- 32.768 kHz crystal oscillator
- Board connectors:
  - USB Type-C® connector
  - ST Zio connector including ARDUINO® Uno V3
  - ST morpho extension pin headers for full access to all STM32 I/Os
- Flexible power-supply options: ST-LINK USB V_{BUS}, USB connector, or external sources
- On-board STLINK-V3E debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeU5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

1. *SMPS significantly reduces power consumption in Run mode, by generating a V_{core} logic supply from an internal DC/DC converter.*

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order an STM32U5 Nucleo-144 board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board reference	Target STM32
NUCLEO-U575ZI-Q	MB1549	STM32U575ZIT6Q
NUCLEO-U5A5ZJ-Q		STM32U5A5ZJT6Q

2.1 Products and codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

NUCLEO-XXYYZE-Q	Description	Example: NUCLEO-U575ZI-Q
XX	MCU series in STM32 Arm Cortex MCUs	STM32U5 series
YY	MCU product line in the series	STM32U575/585
Z	STM32 package pin count	144 pins
E	STM32 flash memory size: • I for 2 Mbytes • J for 4 Mbytes	2 Mbytes
-Q	STM32 has an internal SMPS function	SMPS

The order code is mentioned on a sticker placed on the top or bottom side of the board.

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

Note: macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.
Linux® is a registered trademark of Linus Torvalds.
Windows is a trademark of the Microsoft group of companies.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

5 Quick start

The STM32U5 Nucleo-144 board is a low-cost and easy-to-use development kit, to quickly evaluate and start development with an STM32U5 series microcontroller in an LQFP 144-pin package. Before installing and using the product, accept the Evaluation Product License Agreement from the www.st.com/epla webpage. For more information on the STM32U5 Nucleo-144 board and software example, visit the www.st.com/stm32nucleo webpage.

5.1 Getting started

Follow the sequence below to configure the STM32U5 Nucleo-144 board and launch the software example (refer to Figure 4 for component location):

1. Check the jumper position on the board (refer to Default board configuration).
2. Connect the STM32U5 Nucleo-144 board to a PC with a USB cable (USB Type-A or USB Type-C® to Micro-B) through the USB connector (CN1) to power the board.
3. The 5V_PWR green (LD5) and COM (LD4) LEDs light up, and the green LED (LD1) blinks.
4. Press the blue user button (B1).
5. Observe how the blinking of the LEDs (LD1, LD2, and LD3) changes, according to the clicks on the button (B1).
6. Download the software examples that help to use the STM32 Nucleo features. These are available on the *www.st.com* website.
7. Develop your application using the available examples.

5.2 Default board configuration

By default, the STM32U5 Nucleo-144 board is configured with VDD_MCU at 3.3 V. It is possible to configure the board with VDD_MCU at 1.8 V. Before switching to 1.8 V, ensure that the extension module and external shield connected to the Nucleo-144 board are 1.8 V compatible.

The default jumper configuration and voltage setting are shown in Table 4.

Table 4. Default jumper configuration

Jumper	Definition	Default position	Comment
JP1	STLK_NRST	OFF	STLINK-V3E is selected as the default debugger.
JP2	T_NRST	ON	RST connected between MCU target and debugger
JP4	VDD	[1-2]	VDD MCU voltage selection 3V3
JP5	I_{DD} measurement	ON	MCU VDD current measurement
JP6	5V power selection	[1-2]	5V from STLINK-V3E
JP7	UCPD_DBCC1	OFF	Refer to Section 6.11.2 UCPD.
JP8	UCPD_DBCC2	OFF	Refer to section Section 6.11.2 UCPD.

Figure 2. **Default board configuration**

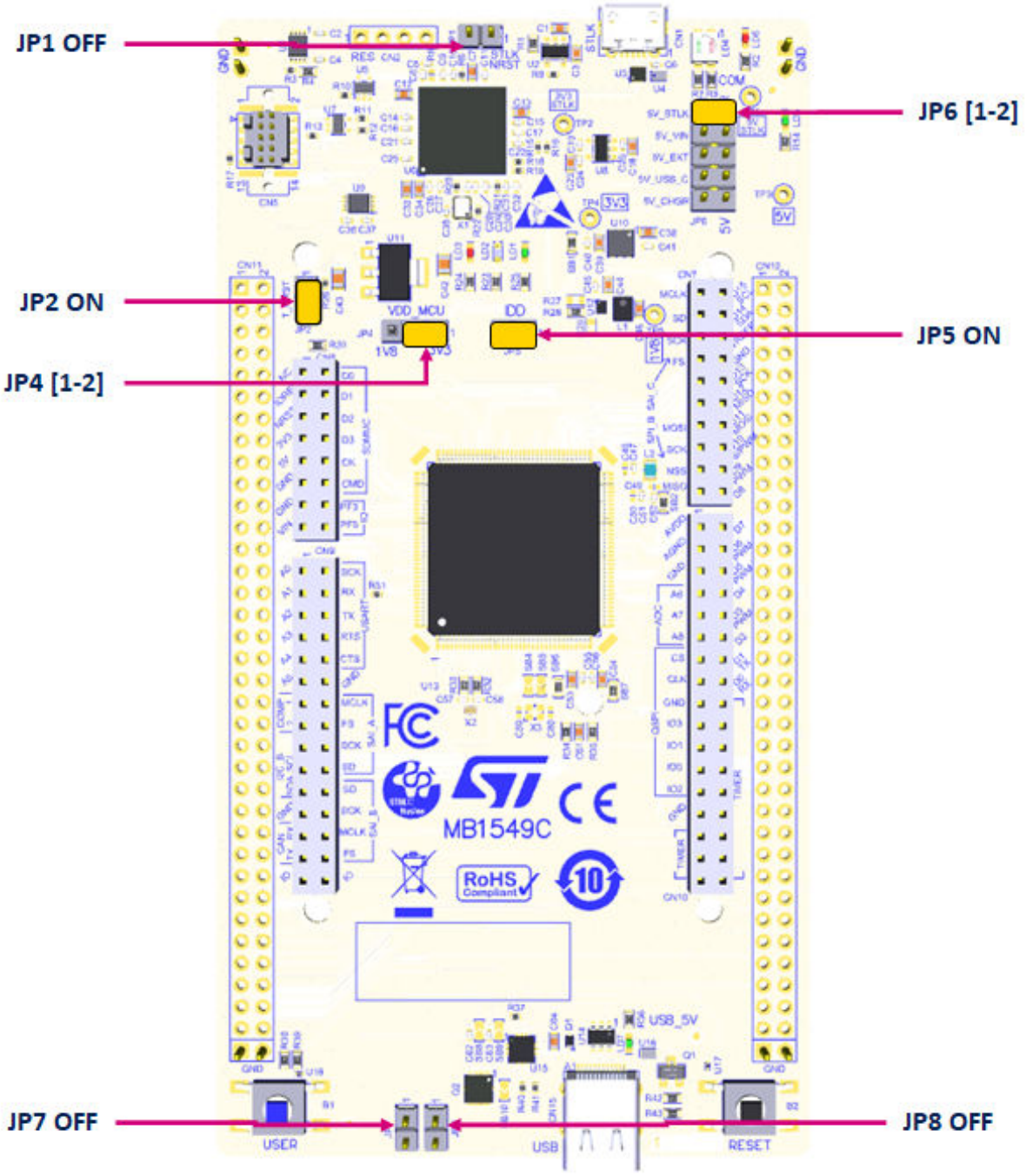


Table 5 explains the other jumper settings and configurations.

Table 5. Jumper configuration

Jumper	Definition	Setting[1]	Comment
JP1	STLK_RST	ON	Use to reset the STLINK-V3E MCU when an external debug probe is used.
		OFF	**STLINK-V3E is selected as the default debugger.**
JP2	T_NRST	**ON**	**STLINK-V3E can reset the target MCU.**
		OFF	STLINK-V3E cannot reset the target MCU. Configuration to use when an external debug probe is used.
JP4	VDD voltage selection	**[1-2]**	**VDD voltage selection is 3V3**
		[2-3]	VDD voltage selection is 1V8
		OFF	No internal VDD power supply (External 3.3 or 1.8 V needed)
JP5	I_{DD} measurement	**ON**	**MCU is powered by the on-board power supplies.**
		OFF	Use an ammeter to measure the VDD_MCU power consumption, or connect a 3.3 or 1.8 V external source on pin 2 (STLINK-PWR tools with STM32CubeMonitor-Power or ULPBench probe as exemple).
JP6	5V Power selection[2]	**[1-2]**	**5V source from STLINK-V3E**
		[3-4]	5V source from ARDUINO® VIN 7-12V
		[5-6]	5V source from 5V_EXT
		[7-8]	5V source from USB Type-C®
		[9-10]	5V source from USB_CHGR. From STLINK-V3E USB connector (CN1) without overcurrent protection.
		OFF	NO 5V power source, configuration when external 3V3 is used.
JP7	UCPD_DBCC1	**OFF**	**UCPD_DBCC1 NOT connected to GND**
		ON	UCPD_DBCC1 connected to GND (For debug purpose)
JP8	UCPD_DBCC2	**OFF**	**UCPD_DBCC2 NOT connected to GND**
		ON	UCPD_DBCC2 connected to GND (For debug purpose)

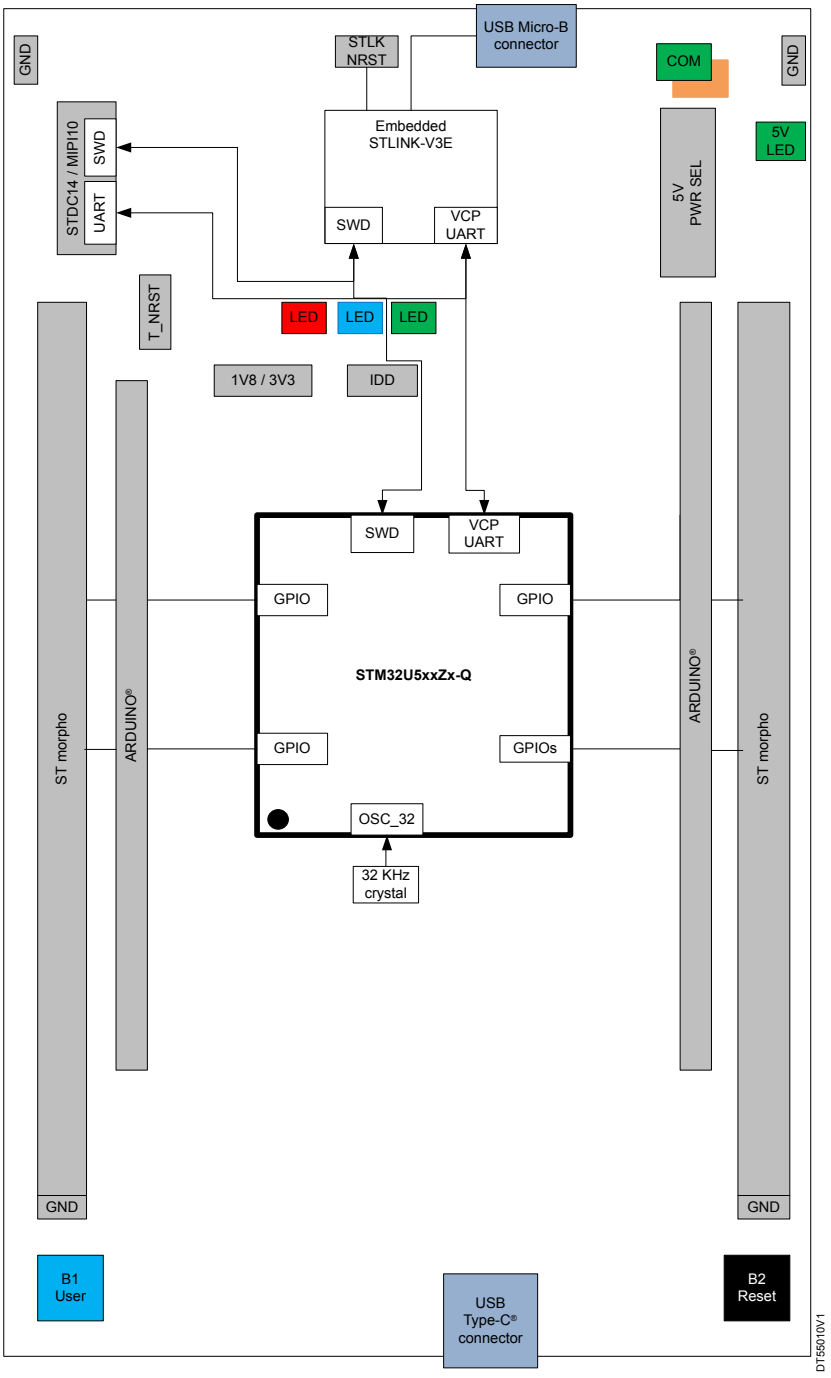
1. *The default configuration is in bold.*
2. *This is recommended to have only one jumper configuration.*

6 Hardware layout and configuration

The STM32U5 Nucleo-144 board is designed around an STM32U5 microcontroller in an LQFP 144-pin package. Figure 3 shows the connections between the STM32 and its peripherals (STLINK-V3E, push-buttons, LEDs, USB ST Zio connectors, and ST morpho headers). Figure 4 and Figure 5 show the location of these features on the STM32U5 Nucleo-144 board.

The mechanical dimensions of the board are shown in Figure 6.

Figure 3. Hardware block diagram



Note: VCP: Virtual COM port
SWD: Serial Wire Debug

6.1 STM32U5 Nucleo-144 board layout

Figure 4. **STM32U5 Nucleo-144 board top layout**

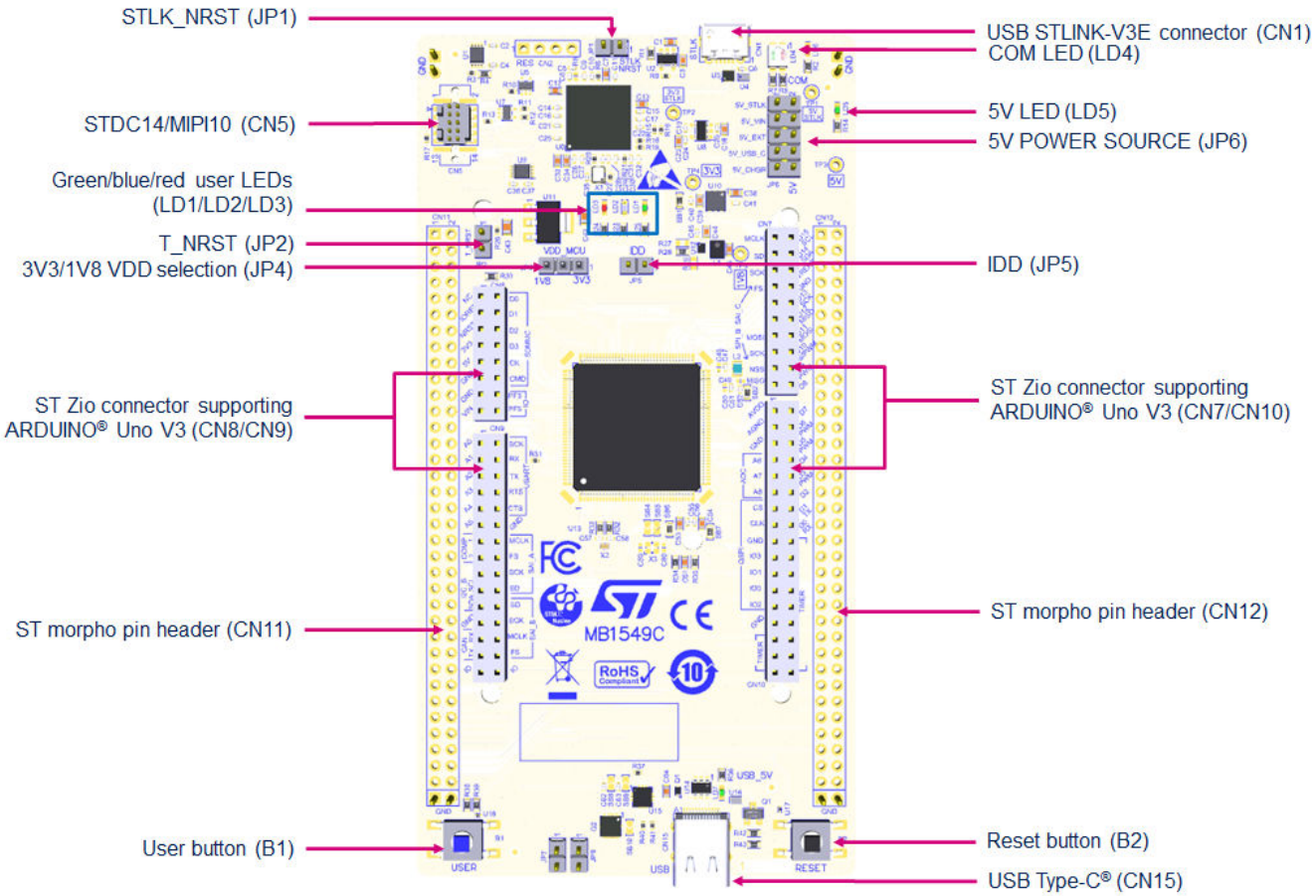
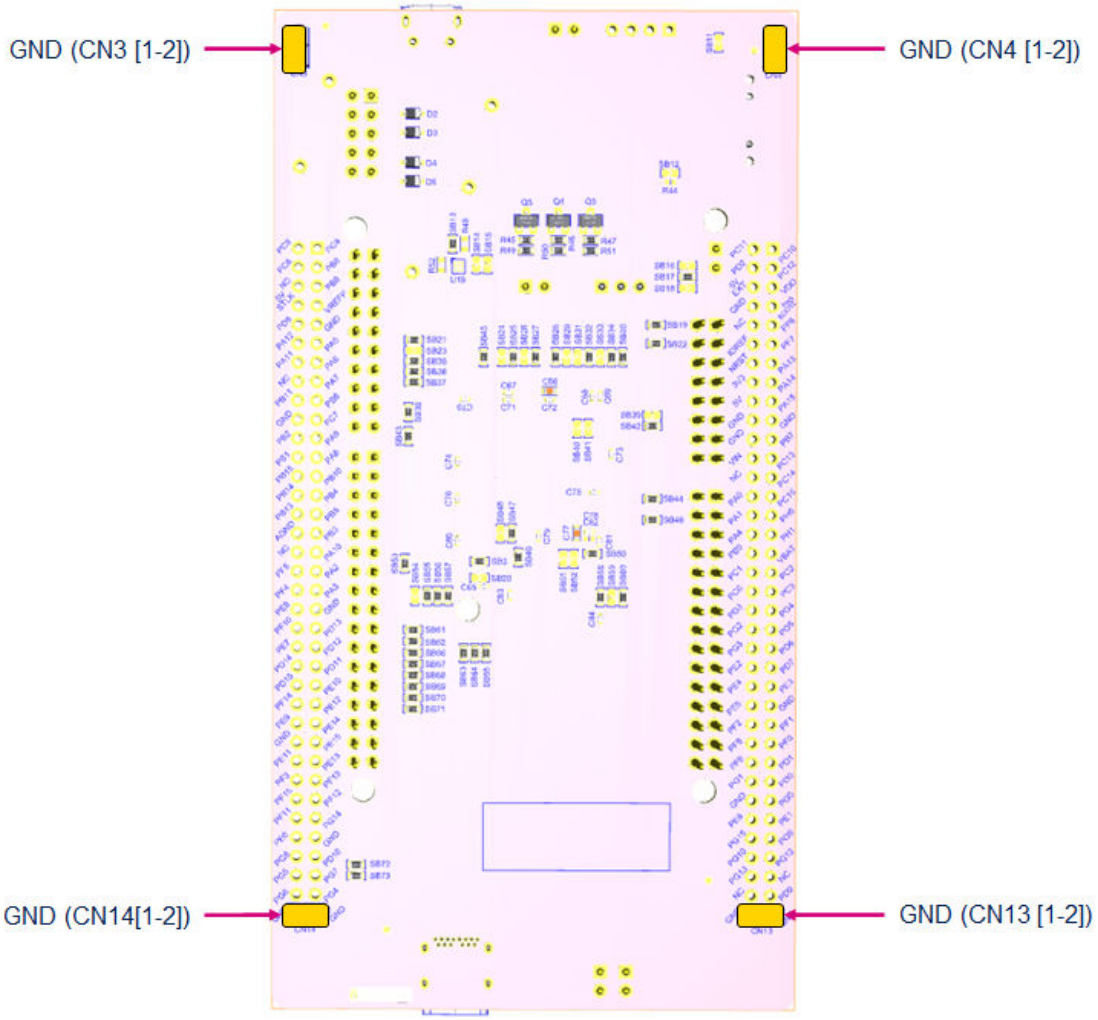
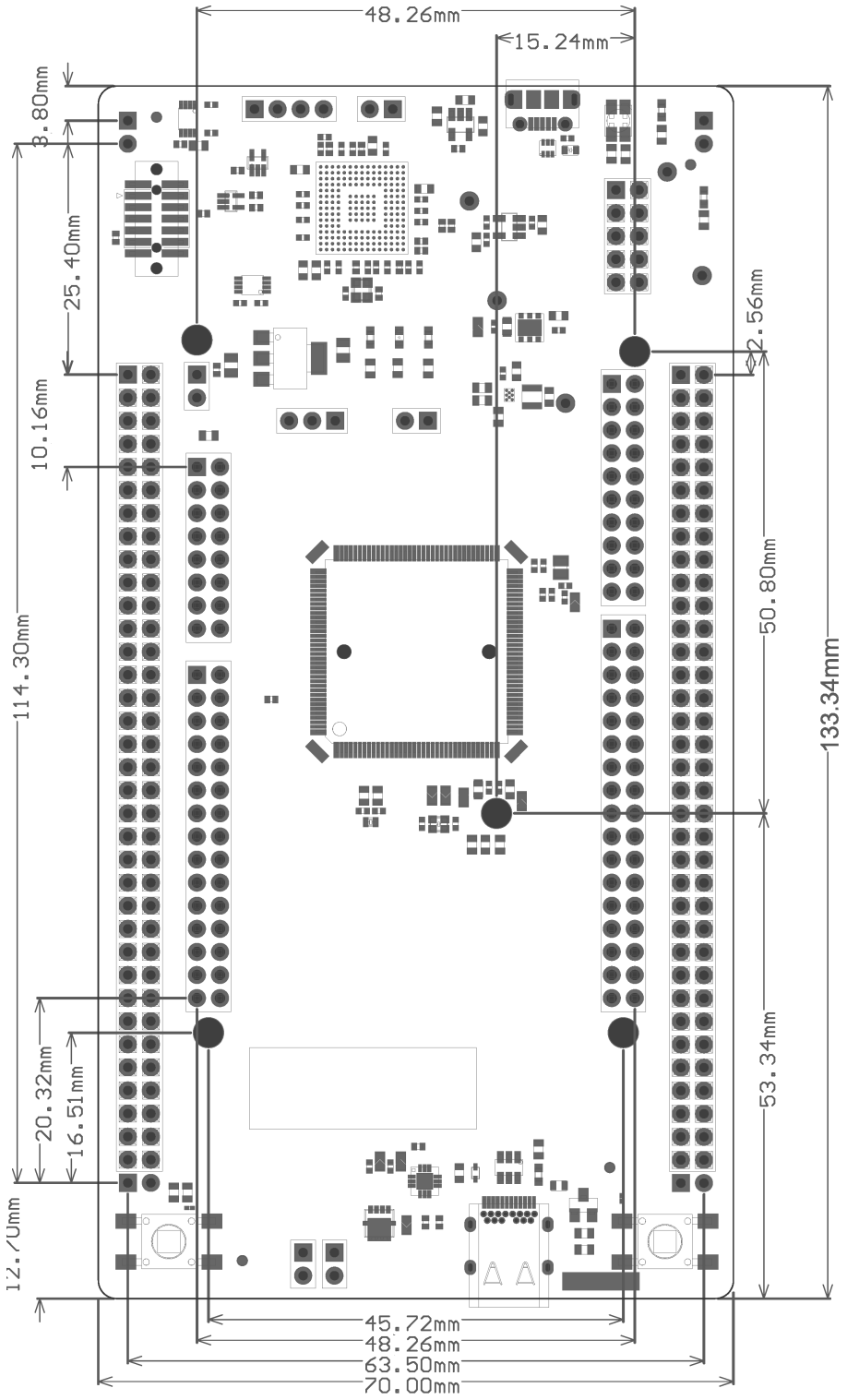


Figure 5. **STM32U5 Nucleo-144 board bottom layout**



6.2 Mechanical drawing

Figure 6. **STM32U5 Nucleo-144 board mechanical drawing (in millimeters)**



6.3 Embedded STLINK-V3E

The chapter below gives some information about the implementation of STLINK-V3E on this STM32U5 Nucleo-144 board. For details information about ST-LINK capabilities, LED management, driver, and firmware for this STLINK-V3E, refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

For information about debugging and programming features of STLINK-V3E, refer to the user manual *STLINK-V3SET debugger/programmer for STM8 and STM32* (UM2448).

6.3.1 Description

There are two different ways to program or debug the onboard STM32 MCU.

- Using the embedded STLINK-V3E
- Using an external debug tool connected to the STDC14/MIPI10 connector (CN5)

Refer to Table 5 to switch between STLINK-V3E or STDC14 configuration.

The STLINK-V3E facility for debugging and flashing is integrated into the STM32 Nucleo-144 board.

Features supported in STLINK-V3E:

- 5 V / 500 mA power supplied by the USB connector (CN1)
- USB 2.0 high-speed compatible interface
- Serial Wire Debug (SWD) with Serial Wire Viewer (SWV)
- Virtual COM port (VCP)
- 1.7 to 3.6 V application voltage
- COM status LED which blinks during communication with the PC
- USB overcurrent protection (U2)

One tricolor LED, (green, orange, and red) provide information about STLINK-V3E communication status (LD4). For details information about this LED, refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

Table 6 describes the USB Micro-B connector (CN1) pinout.

Table 6. USB Micro-B connector (CN1) pinout

Pin	Pin name	Signal name	STLINK-V3E STM32 pin	Function
1	VBUS	5V_USB_CHGR	-	VBUS Power
2	DM	USB_DEV_HS_CN_N	PB14	DM
3	DP	USB_DEV_HS_CN_P	PB15	DP
4	ID	-	-	ID
5	GND	GND	GND	GND

6.3.2 Drivers

The driver installation is not mandatory for Windows® 10 but allocates an ST-specific name to the ST-LINK COM port in the system device manager.

For details information regarding the ST-LINK USB driver, refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

6.3.3 STLINK-V3E firmware upgrade

STLINK-V3E embeds a firmware upgrade (stsw-link007) mechanism through the USB port. As the firmware might evolve during the lifetime of the STLINK-V3E product, to add new functionalities, fix bugs, and support new microcontroller families, it is recommended to visit the *www.st.com* website before starting to use the STM32U5 Nucleo-144 board and periodically, to stay up-to-date with the latest firmware version.

For details information about firmware upgrades, refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

6.3.4 Using an external debug tool to program and debug the on-board STM32

To support an external debug tool, set the jumper (JP1) to reset the STLINK-V3E to avoid I/O conflict, and remove the jumper (JP2) to avoid reset conflict. Then connect the external debug tool through the STDC14/MIPI10 debug connector (CN5).

When using the external debug connector (CN5), the user can supply the STM32U5 Nucleo-144 board with the STLINK-V3E connector (CN1) or select another power supply source as described in Power supply and power selection.

Figure 7. Connecting an external debug tool to program the on-board STM32U5

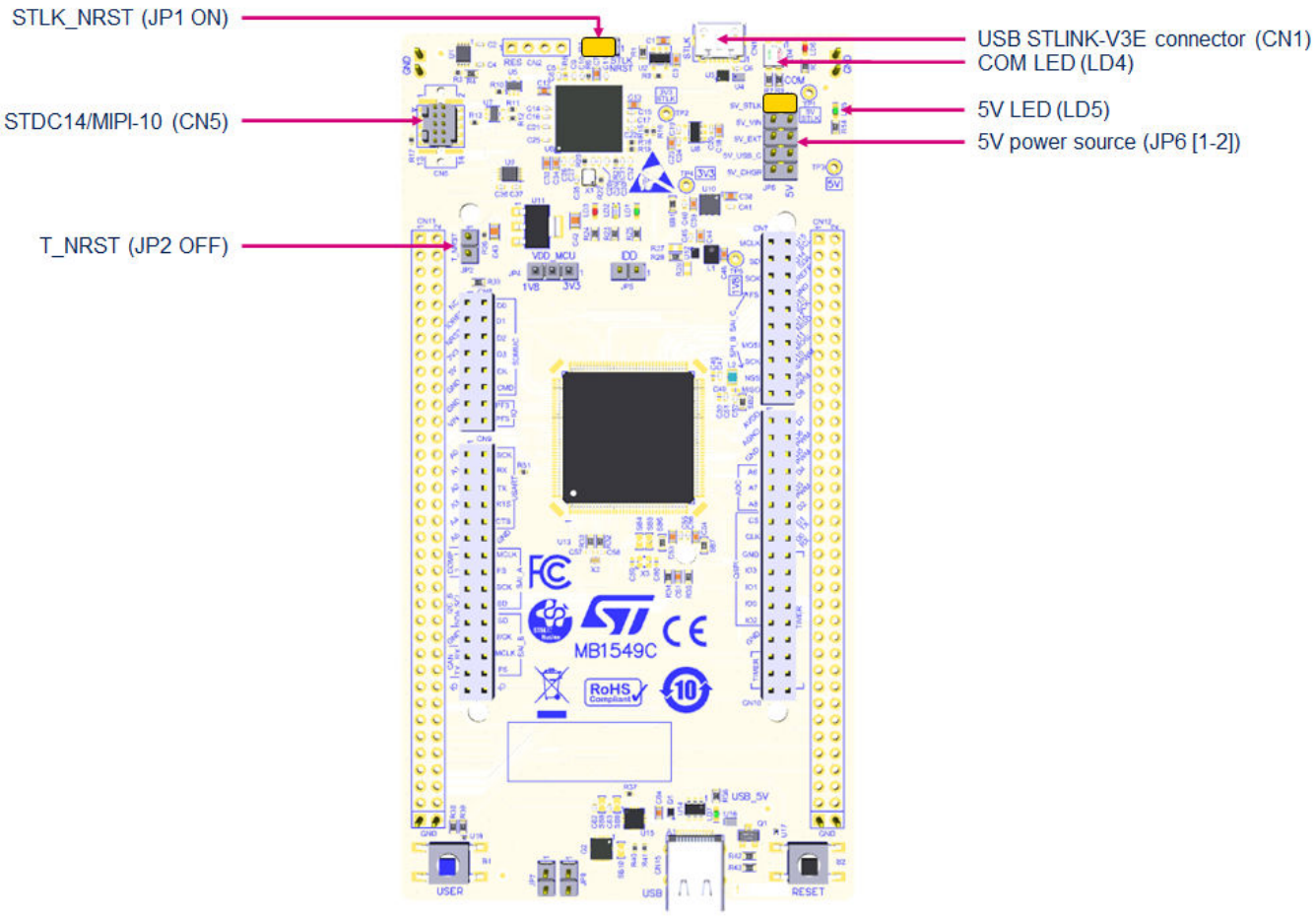


Figure 8 shows the STDC14/MIPI10 connector (CN5).

Figure 8. STDC14/MIPI10 debug connector (CN5)

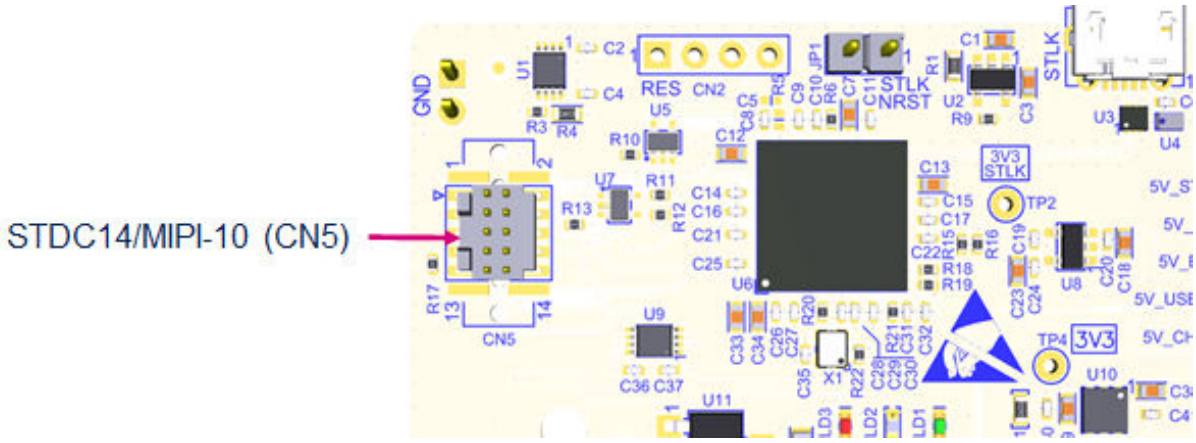


Table 7 describes the STDC14/MIPI10 connector (CN5) pinout.

Table 7. STDC14/MIPI10 debug connector (CN5) pinout

MIPI10 pin	STDC14 pin	CN5	Function
-	1	NC	Reserved(1)
-	2	NC	Reserved(1)
1	3	VDD	Target VDD(2)
2	4	T_SWDIO	Target SWDIO using SWD protocol or target JTMS (T_JTMS) using JTAG protocol
3	5	GND	Ground
4	6	T_SWCLK	Target SWCLK using SWD protocol or target JTCK (T_JTCK) using JTAG protocol
5	7	GND	Ground
6	8	T_SWO	Target SWO using SWD protocol or target JTDO (T_JTDO) using JTAG protocol (SB44 ON)
7	9	NC	T_JRCLK(3)/NC(4)
8	10	T_JTDI	Not used by SWD protocol, target JTDI (T_JTDI) using JTAG protocol, only for external tools (SB39 OFF)
9	11	GNDDetect	GND detect for plug indicator(5)
10	12	T_NRST	Target NRST
-	13	T_VCP_RX	Target RX used for VCP (with UART supporting bootloader)(6)
-	14	T_VCP_TX	Target TX used for VCP (with UART supporting bootloader)(2)

1. *Do not connect to the target. It is not connected to the STM32U5 Nucleo-144 board.*
2. *Input for the external debug tools and output for the STM32U5 Nucleo-144 board.*
3. *Optional loopback of JTCK on the target side.*
4. *NC means not required for the SWD connection, not connected on the STM32U5 Nucleo-144 board.*
5. *Tied to GND. It might be used by the target for the detection of the tool.*
6. *Output for the external debug tools and input for the STM32U5 Nucleo-144 board.*

Two level shifters are used on VCP and SWD interfaces to offer a debug capability with MCU powered by a 1.8 V power source. The level Shifters are used for signals from target MCU (1.8/3.3 V) to STLINK-V3E (3.3 V).

6.4 Power supply and power selection

6.4.1 External power supply input

It is possible to configure the STM32U5 Nucleo-144 board to use any of the following power sources:

- 5V_STLK from STLINK-V3E USB connector (CN1)
- VIN (7 to 12 V) from ARDUINO®-included Zio connector (CN8) or ST morpho connector (CN11) with 5 V adaptation from LDO (U11)
- 5V_EXT from ST morpho connector (CN11)
- 5V_USB_C from USB Type-C® connector (CN15)
- 5V_CHGR from STLINK-V3E USB connector (CN1)
- 3V3 from ARDUINO®-included Zio connector (CN8) or ST morpho connector (CN11)

If VIN, 5V_EXT, or 3V3 is used to power the STM32U5 Nucleo-144 board, this power source must comply with the standard EN-60950-1: 2006+A11/2009 and must be safety extra-low voltage (SELV) with limited power capability.

The power supply capabilities are summarized in Table 8.

Table 8. Power sources capability

Input Power name	Connector pins	Voltage range	Max. current	Limitation
5V_STLK	CN1 pin 1 JP6 [1-2]	4.75 to 5.5 V	500 mA	The maximum current depends on the presence or absence of USB enumeration: • 100 mA without enumeration • 500 mA with enumeration OK
VIN / 5V_VIN	CN8 pin 15 CN11 pin 24 JP6 [3-4]	7 to 12 V	800 mA	From 7 to 12 V only and input current capability is linked to input voltage: • 800 mA input current when VIN = 7 V • 450 mA input current when 7 V < VIN < 9 V • 250 mA input current when 9 V < VIN < 12 V
5V_EXT	CN11 pin 6 JP6 [5-6]	4.75 to 5.5 V	500 mA	The maximum current depends on the power source.
5V_USB_C	CN15 JP6 [7-8]	4.75 to 5.5 V	1 A	The maximum current depends on the USB host used to power the Nucleo.
5V_CHGR	CN1 pin 1 JP6 [9-10]	4.75 to 5.5 V	500 mA	The maximum current depends on the USB wall charger used to power the Nucleo. There is no USB enumeration.
3V3	CN8 pin 7 CN11 pin 16 JP5 pin 2	3.0 to 3.6 V	-	The maximum current depends on the 3V3 source. The 3V3 can be used when the STLINK-V3E part of the PCB is not used. SB1 must be OFF to protect LDO (U10).
VDD	JP4 pin 2	1.71 to 3.6 V	-	It is possible to power only the MCU power supplies pins by applying a voltage source on JP4 pin 2. In this case, only the MCU is powered. External functions like debugging, LED, or the expansion connector are not powered. This option can be used for the MCU power consumption measurement.

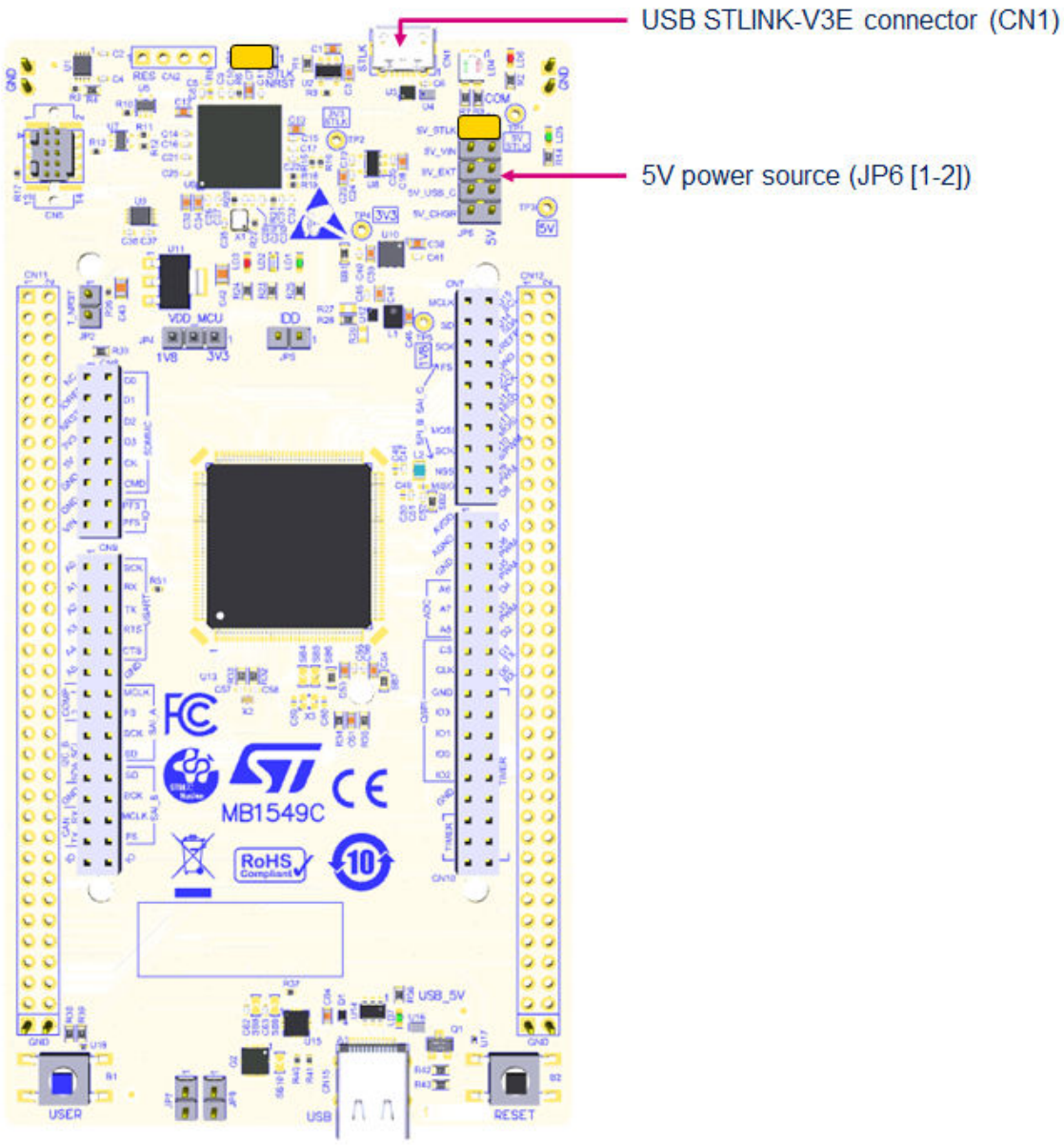
5V_STLK is a 5V DC power with limitations from the STLINK-V3E USB connector (CN1). In this case, the 5V jumper selection (JP6) must be on pin [1-2] to select the 5V_STLK power source on the JP6 connector. This is the default setting. If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the T_PWR_EN signal from STLINK-V3E. This pin is connected to a power switch (U2) with the management of the maximum current delivery.

The STM32U5 Nucleo-144 board and its shield can be powered from the STLINK-V3E USB connector (CN1), but only the STLINK-V3E circuit is powered before USB enumeration because the host PC only provides 100 mA to the board at that time. During the USB enumeration, the STM32U5 Nucleo-144 board requests 500 mA power to the host PC.

- If the host can provide the required power, the U2 power switch is enabled, the green LED (LD5) is turned ON, and the STM32U5 Nucleo-144 board and its shield can consume up to 500 mA.
- If the host is not able to provide the requested current, the enumeration fails. the U2 power switch remains OFF and the MCU part including the extension board is not powered. As a consequence, the green LED (LD5) remains OFF. In this case, it is recommended to use an external power supply.

5V_STLK configuration: 5V jumper selection JP6[1-2] must be connected as shown in Figure 9.

Figure 9. JP6 [1-2]: 5V_STLK power source

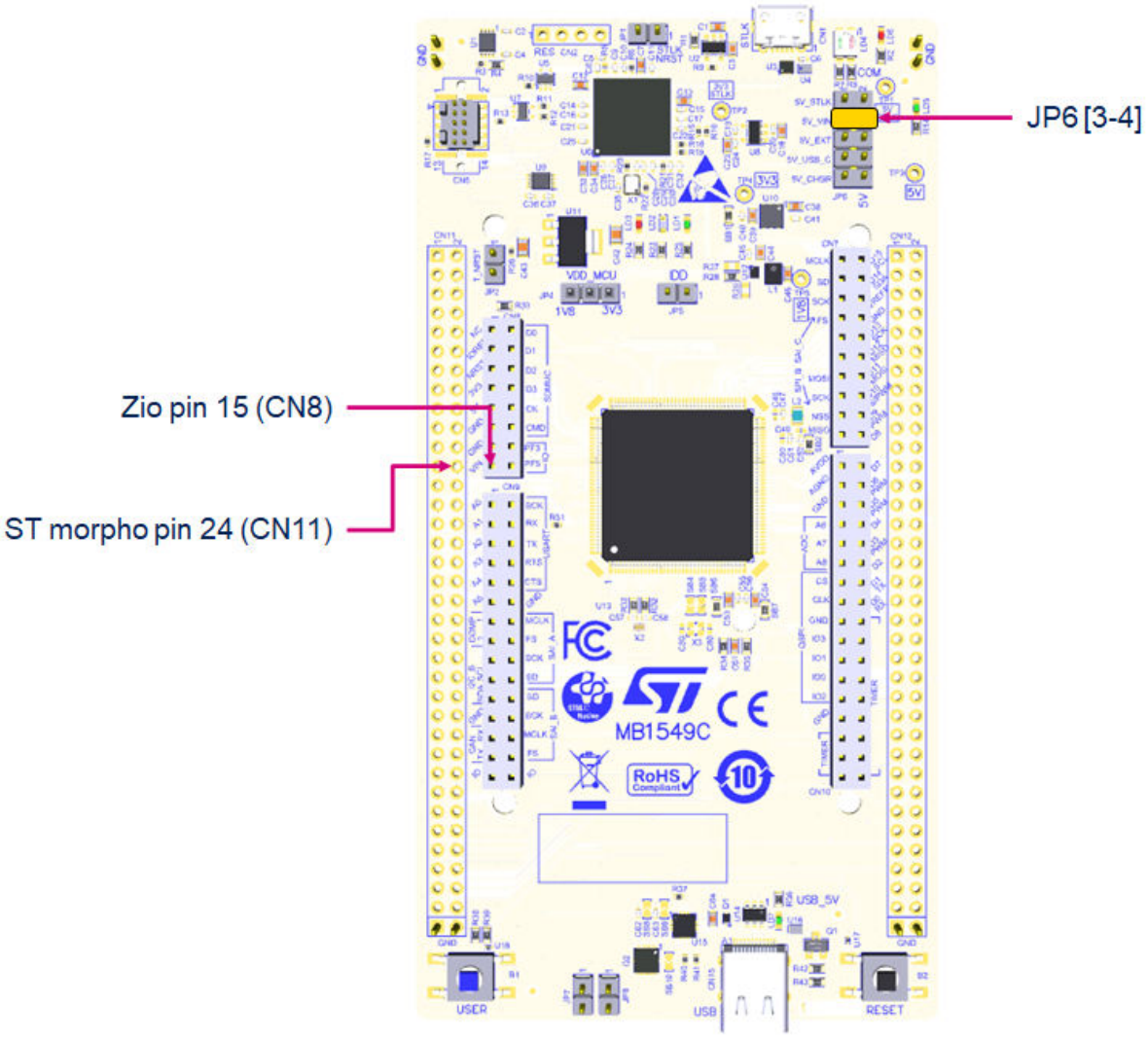


VIN (5V_VIN) is the 7 to 12 V DC power source from the ARDUINO® included Zio connector (CN8) pin 15 (VIN), or from the ST morpho connector (CN11) pin 24. The 5V jumper selection (JP6) must be on pin [3-4] to select the 5V_VIN power source. In that case, the DC power can come from the ARDUINO® Uno V3 battery shield (compatible with the Adafruit PowerBoost 500 shield).

An LDO (U11) is used to provide a fixed 5 V from VIN (7-12V).

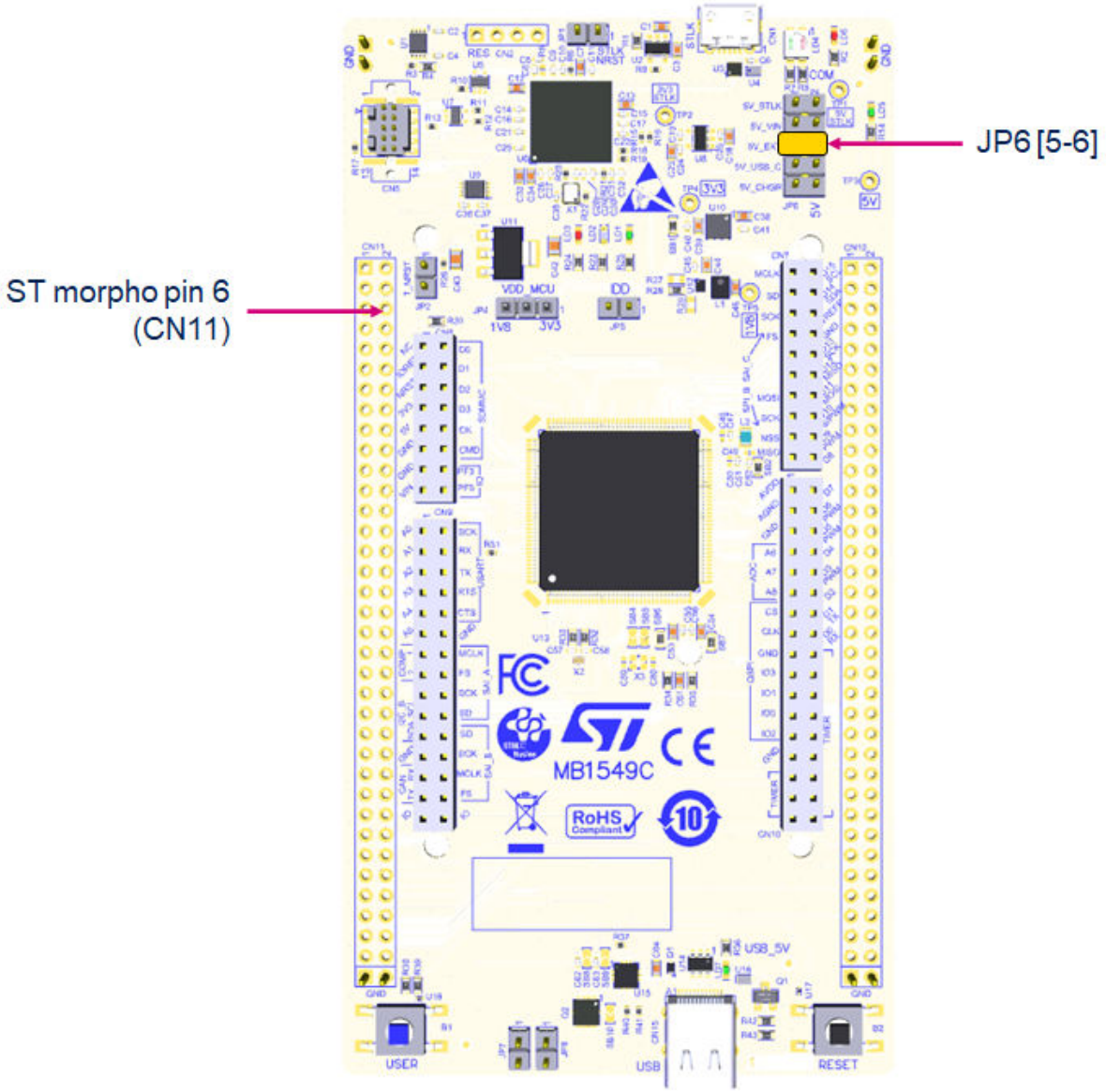
5V_VIN configuration: 5 V jumper selection (JP6) [3-4] must be connected as shown in Figure 10.

Figure 10. JP6 [3-4]: 5V_VIN power source



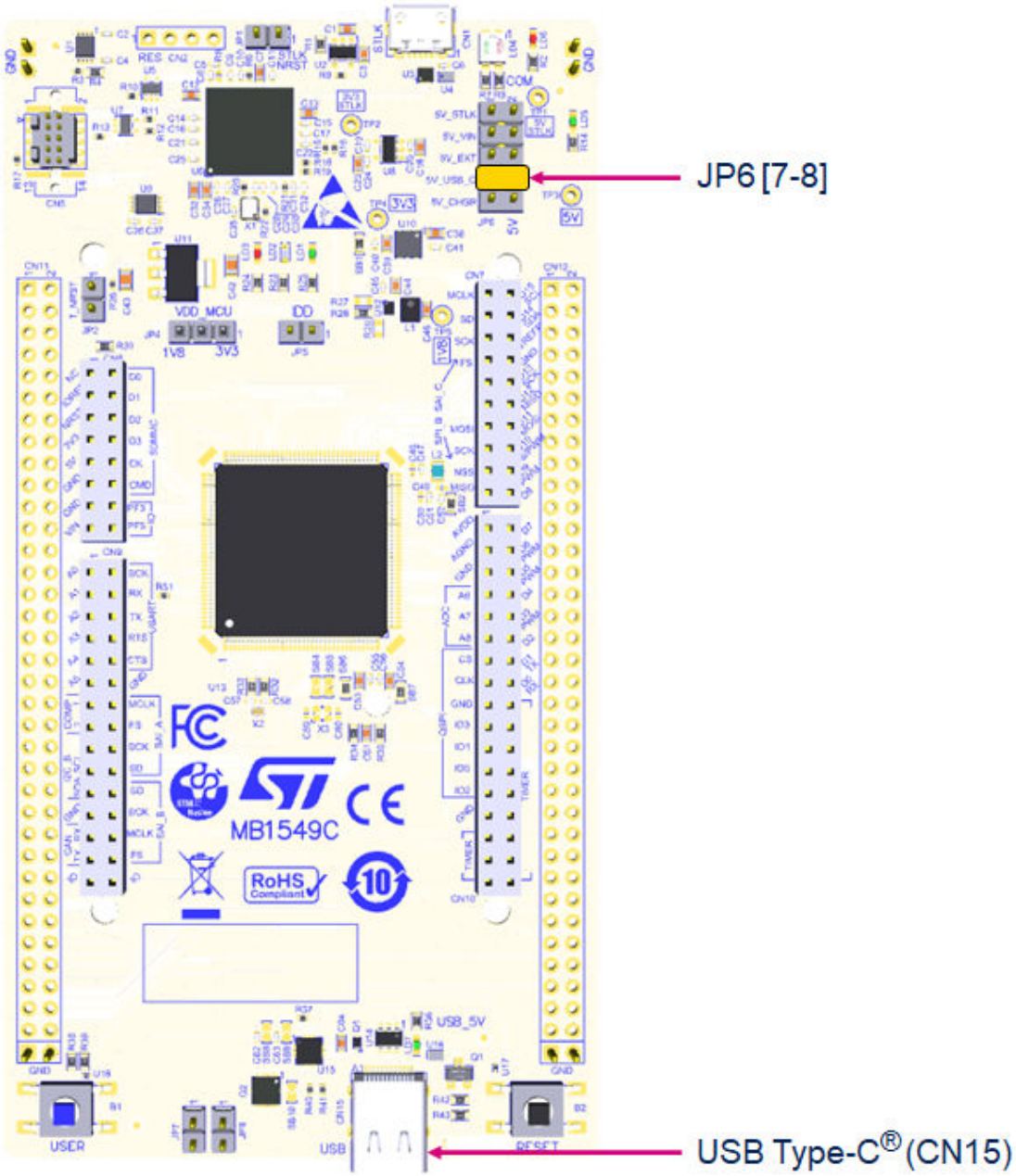
5V_EXT is the DC power coming from an external 5V DC power source from the ST morpho connector (CN11) pin 6. The 5V jumper selection (JP6) must be on pin [5-6] to select the 5V_EXT power source on the JP6 connector, and must be connected as shown in Figure 11.

Figure 11. JP6 [5-6]: 5V_EXT power source



5V_USB_C is the DC power source coming from the 5V USB connector (CN15). The 5V jumper selection (JP6) must be set on [7-8] and must be connected as shown in Figure 12.

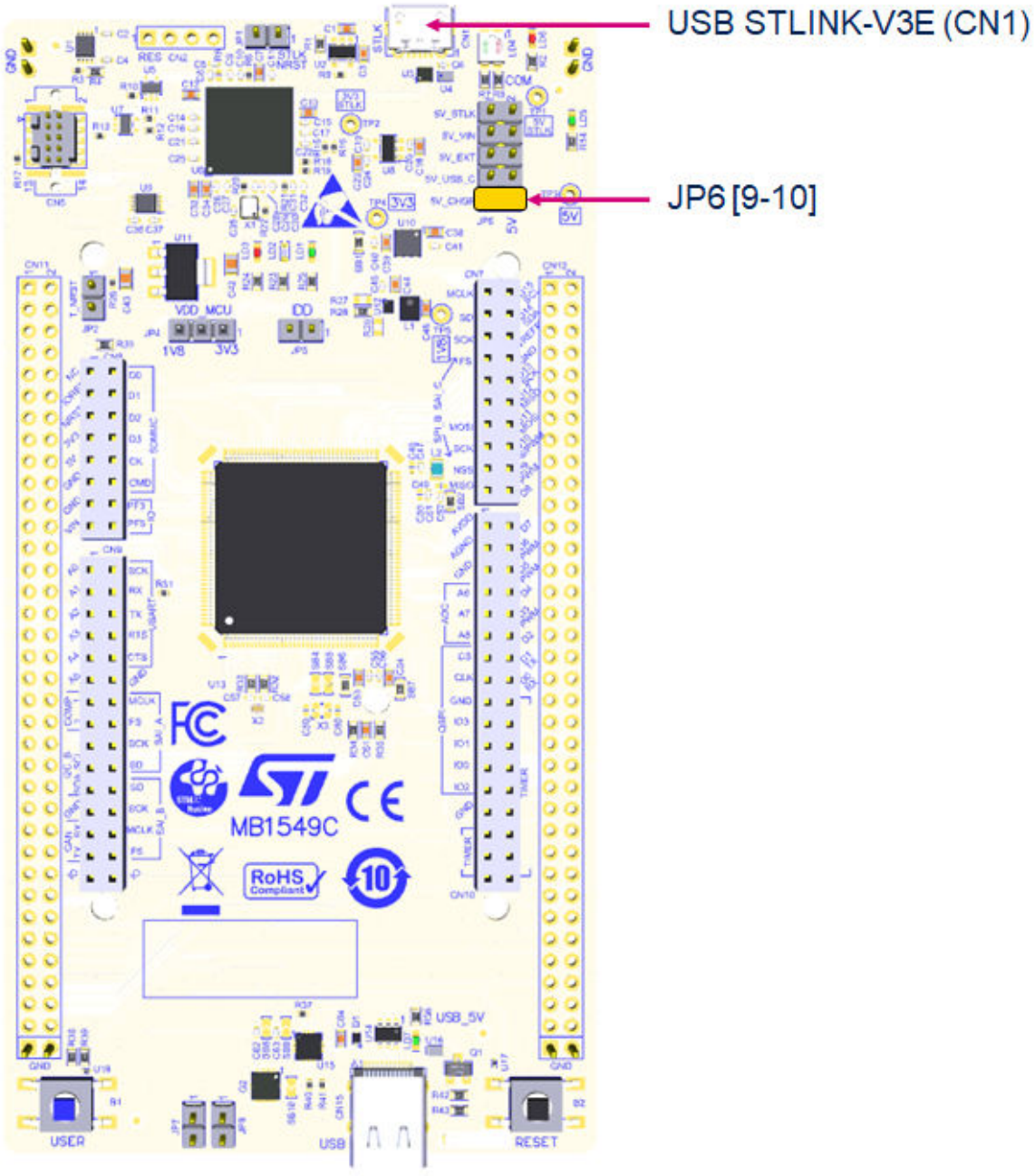
Figure 12. JP6 [7-8]: 5V_USB_C power source



5V_CHGR is when a DC power charger is connected to the USB STLINK-V3E connector (CN1). To select the 5V_CHGR power source, the 5V jumper selection (JP6) must be between pins [9-10]. If an external USB charger powers the STM32U5 Nucleo-144 board, then the debugging feature through (CN1) is not available. If a host computer is connected instead of the charger, the current limitation is no more effective. In this case, the host computer can be damaged, and it is recommended to select 5V_STLK mode.

5V_CHGR configuration: 5V jumper selection JP6[9-10] should be connected as shown in Figure 13.

Figure 13. JP6 [9-10]: 5V_CHGR power source



Note: With this JP6 configuration, the USB_PWR protection is bypassed. This configuration is forbidden to power the board with a computer USB port, as the USB_PWR_protection is bypassed. The reason is that if the board consumes more than 500 mA, it can damage the computer.

External 3V3 power supply input. In some situations, it is interesting to use an external 3.3 V source on the 3V3 input (CN8 pin 7 or CN11 pin 16), for instance in case the 3.3V is provided by an extension board. When the Nucleo-144 is powered with only a 3.3V source, the STLINK-V3E part is not powered, thus programming and debugging are unavailable.

When using the 3V3 input the STLINK-V3E part is not supplied.

For this configuration, it is recommended to remove SB1 to avoid backward voltage to 5 V through U10, and remove JP2 to avoid STM32 MCU reset from the STLINK-V3E part.

VDD power supply input. In some situations, it is interesting to use an external power source from 1.71 to 3.6 V to power only the MCU power supply pins (JP4 pin 2 or JP5 pin 2). In this configuration, external functions like debugging, LED, or the expansion connector are not powered. This option can be used for the optimized MCU power consumption measurement.

6.4.2 Programing/debugging when the power supply is not from STLINK-V3E (5V_STLK)

In case the current consumption of the Nucleo-144 and the expansion boards exceeds the allowed current on the ST-LINK USB connector, the external power 5V_VIN, 5V_EXT, or 5V_USB_C can be used. In such a case, it is still possible to use the embedded ST-LINK for VCP programming and debugging.

In this case, the following power sequence procedure must be respected:

1. Connect the JP6 jumper according to the 5V selected external power source.
2. Connect the external power source according to JP6.
3. Power ON the external power supply.
4. Check that the 5 V green LED (LD5) is turned ON.
5. Connect the PC to the USB connector (CN1) for programming/debugging.

If this sequence is not respected, the board might be powered by V_{BUS} first from STLINK-V3E, and the following risk might be encountered:

- If more than 500 mA current is needed by the board, the PC might be damaged or the current can be limited by the PC. Therefore, the board is not powered correctly.
- 500 mA is requested at enumeration so there is a risk that the request is rejected and enumeration does not succeed if PC cannot provide such current. Consequently, the board is not powered (LD5 LED remains OFF).

6.4.3 Power supply output

- **5V**: Whatever the power source (5V_STLK, 5V_VIN, 5V_EXT, 5V_CHGR, or 5V_USB_C) the generated 5 V is present on CN8 pin 9 or CN11 pin 18 and can be used as an output power supply for an ARDUINO® shield or an extension board. In this case, the maximum current of the power source specified in Table 8 needs to be respected.
- **3V3**: The internal 3V3, on CN8 pin 7 or CN11 pin 16, can be used also as power supply output. The current is limited by the maximum current capability of the U10 regulator (500 mA including the Nucleo and shield boards consumption).

6.4.4 Internal power supply

The Nucleo boards are designed to support two specific voltage configurations:

- VDD at 3.3 V configuration to reach Nucleo-144 low-power mode
- VDD at 1.8 V configuration to demonstrate MCU low-voltage capability

6.4.4.1 3V3

Regardless of the 5 V power source, an LDO is used to deliver a fixed 3.3 V power voltage from 5 V. The maximum current capability of this source is 500 mA. To select the 3.3V voltage for the VDD, set the VDD jumper (JP4) on [1-2].

A solder bridge (SB1) is used to disconnect the LDO output when an external 3.3 V is applied to the Nucleo-144 board, to avoid backward voltage to 5 V through this LDO.

- SB1 ON: U10 LDO output provides a 3V3 power supply (default configuration).
- SB1 OFF: U10 LDO output does not provide 3V3. An external 3.3 V power source is needed.

6.4.4.2 *1V8*

An external SMPS can be used for the MCU to work at 1.8 V. The external SMPS capability is 400mA maximum. Before using the 1.8 V voltage, it is necessary to check that all interfaces connected to the Nucleo-144 board are 1.8 V compatible. To select the 1.8 V for the VDD, set the VDD jumper (JP4) on [2-3].

In this mode, it is possible to keep some MCU voltage domain at 3V3 depending on the application use case. The MCU voltage selection is done according to the solder bridge configuration. Refer to Table 9 for solder bridge configuration.

6.4.4.3 *JP4 VDD voltage selection 1V8/3V3*

The JP4 jumper selects the VDD voltage:

- Set JP4 on [1-2] to set VDD to 3V3.
- Set JP4 on [2-3] to set VDD to 1V8.

The consumption on this jumper includes the MCU power pins connected to the VDD_MCU power line and the other features supplied by VDD, such as the level shifter power supply pins for STLINK-V3E, the user button, the ARDUINO® shield on the IOREF pin, and power supply pins on the ST morpho connector.

6.4.5 MCU power supply

The default configuration of the MCU power pins is described in Table 9.

Table 9. MCU power supplies

Solder bridge configuration	MCU power supply
JP4 [1-2] / JP4 [2-3]	VDD selection: Jumper selection for VDD 3V3 / 1V8
JP5 [1-2] / ammeter	I_{DD}: JP5 ON to supply the MCU or connected with an ammeter to do the current measurement.
SB2 ON	SB for VDDSMPS input voltage
SB3 ON	SB for VREFP input voltage
SB30 ON	SB for VDDUSB input voltage
SB28 ON / SB29 OFF	SB for VDDIO2 PG[2-15] input voltage SB28 ON / SB29 OFF: VDDIO follows 1V8 to 3V3 VDD_MCU. SB28 OFF / SB29 ON: VDDIO fixed to 3V3 whatever the VDD-MCU voltage is.
SB50 ON	SB for VBAT input voltage
SB55 OFF / SB54 ON	SB for VDDA/VREF input voltage SB55 ON / SB54 OFF: VDDA/VREF follows 1V8 to 3V3 VDD_MCU. SB55 OFF / SB54 ON: VDDA/VREF fixed to 3V3 whatever the VDD-MCU voltage is. For more detail about VDDA/VREFP power supply, refer to the MCU datasheet.

Warning: *On this Nucleo-144, the power-on sequence implementation for the 1.8 V use case is given as an example and might not follow the recommended power-on sequencing. Refer to the application note Getting started with STM32U575/585 MCU hardware development (AN5373) and STM32U5xx products datasheets for power on sequencing.*

INTERNAL VCORE SMPS power supply

Power figures in run mode are significantly improved, by generating a V_{core} logic supply from the internal DC/DC converter (this function is only available on '-Q' suffixed boards).

For all general information concerning design recommendations for STM32U5 with internal SMPS and design guide for ultra-low-power applications with performance, refer to the application note *Getting started with STM32U575/585 MCU hardware development* (AN5373) at the *www.st.com* website.

6.4.6 VDD_MCU I_{DD} measurement

The labeled I_{DD} jumper (JP5) is used to measure the consumption of the STM32 microcontroller by removing the jumper and by connecting an ammeter or any other current measurement tool.

- Jumper ON: STM32 Microcontroller is powered (default).
- Jumper OFF: an ammeter or an external 3V3 power source must be connected to power and measure the STM32 microcontroller consumption.

The IDD jumper performs the current measurement for both 3V3 and 1V8 MCU voltage ranges.

6.5 LEDs

User green LED (LD1)

The user green LED (LD1) is connected to the PC7 STM32 I/O (SB21 ON and SB23 OFF, default configuration) or PA5 (SB21 OFF and SB23 ON, optional configuration corresponding to the D13 ST Zio connector). A transistor is used to drive the LED whatever the MCU 1.8/3.3 V voltage range.

User blue LED (LD2)

The user blue LED (LD2) is connected to PB7. A transistor is used to drive the LED whatever the MCU 1.8/3.3 V voltage range.

User red LED (LD3)

The user red LED (LD3) is connected to PG2. A transistor is used to drive the LED whatever the MCU 1.8/3.3 V voltage range.

These user LEDs are ON when the I/O is in the HIGH state, and are OFF when the I/O is in the LOW state.

COM tricolor LED (LD4)

The tricolor (green, orange, and red) LED (LD4) provides information about STLINK-V3E communication status. For details information about this LED refer to the technical note *Overview of ST-LINK derivatives* (TN1235)

Green PWR LED (LD5)

The green LED (LD5) indicates that the Nucleo-144 is powered by a 5 V source, and this source is available on CN8 pin 9 and CN11 pin 18, but also for the LDO and external SMPS input.

Red STLINK-V3E USB OC power switch fault LED (LD6)

The red LED (LD6) indicates that the board power consumption on the USB exceeds 500 mA.

- If 500 mA or more is expected, the board must be supplied by one of the external 5 V sources compatible with more than 500 mA capability.
- If more than 500 mA is not expected, the board must be analyzed to understand the extra consumption.

USB Type-C® green LED (LD7)

The green LED (LD7) is driven by the presence of the 5 V on the USB Type-C® user connector. refer to USB Type-C® FS/HS for more details.

6.6 Push-buttons

Two buttons are available on the Nucleo board.

User button (B1)

The blue button for the user and wake-up functions is connected to PC13 to support the default TAMPER function or to PA0 to support the optional wake-up function of the STM32 microcontroller. When the button is pressed the logic state is HIGH, otherwise, the logic state is LOW.

- To connect the USER button to PC13, SB58 must be ON and SB59 must be OFF. This is the default configuration.
- To connect the USER button to PA0, SB58 must be OFF and SB59 must be ON. This is the optional configuration.

Buttons are implemented using a hardware debounce filter combined with a serial resistor to avoid damaging the STM32 GPIO in case of wrong GPIO setting. This 330 Ω serial resistor (R39) can be replaced by a 0 Ω resistor assuming the GPIO configuration is properly done. The hardware debounce filter is composed of a 100 nF capacitor (C84) with a 100 kΩ pull-down resistor (R38). Both components can be suppressed to reduce the BOM cost assuming that the debounce is handled by firmware.

Warning: *The PC13 I/O used for the user button must be set to INPUT, pull-down (PD) with debouncing. Never set the PC13 to OUTPUT / LOW level to avoid a shortcut when the user button is pressed.*

Reset button (B2)

The black button connected to NRST is used to reset the STM32 microcontroller. When the button is pressed the logic state is LOW, otherwise, the logic state is HIGH.

The blue and black plastic hats placed on these push-buttons can be removed if necessary when a shield or an application board is plugged into the top of the Nucleo board. This avoids pressure on the buttons and consequently a possible permanent target MCU reset.

6.7 OSC clock sources

Three clock sources are described below:

- LSE is the 32.768 kHz crystal for the STM32 embedded RTC.
- MCO is the 8 MHz clock from STLINK-V3E MCU for the STM32 microcontroller.
- HSE is the 16 MHz oscillator for the STM32 microcontroller. This clock is available depending on the target STM32 series microcontroller used on the Nucleo-144 board.

6.7.1 LSE: OSC 32 KHz clock supply

There are three ways to configure the pins corresponding to the low-speed clock (LSE):

LSE on-board oscillator X2 crystal (Default configuration)

To help select the crystal and its associated capacitors, refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867).

As an example, this crystal might have the following characteristics: 32.768 kHz, 9 pF, and 20 ppm. It is then recommended to use NX1610SE_32.768KHZ-EXS00A-MU01499 manufactured by NDK.

In this case, configure the board as follow:

- R32 and R33 ON
- SB51 and SB52 OFF

External oscillator connected to PC14 input

From the external oscillator through pin 25 of the ST morpho connector (CN11). The following configuration is needed:

- R32 and R33 OFF
- SB51 and SB52 ON, for connection from Zio connector CN11 pin 25

LSE not used

PC14 and PC15 are used as GPIOs instead of low-speed clocks. The following configuration is needed:

- R32 and R33 OFF
- SB51 and SB52 ON

6.7.2 OSC clock supply

There are four ways to configure the pins corresponding to the external high-speed clock (HSE):

HSE: on-board oscillator crystal (X3) (configuration depends on the embedded STM32U5 series microcontroller)

To help select the crystal and its associated capacitors (C59, C60), refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867).

As an example, this crystal might have the following characteristics: 16 MHz, 8 pF, and 20 ppm. It is then recommended to use NX2016SA_16MHz_EXS00A-CS07826 manufactured by NDK.

In this case, configure the board as follow:

- SB47 and SB49 OFF. PH0 and PH1 are not connected to CN11 as I/Os.
- SB48 (MCO) OFF
- SB4 and SB5 ON are connected to external HSE.

MCO from STLINK-V3E (default: not connected):

The MCO output of STLINK-V3E MCU is used as an input clock. This frequency cannot be changed. It is fixed at 8 MHz and connected to PH0 OSC_IN of the STM32 microcontroller. To use this clock source, the following configuration is needed:

- SB47 OFF and SB49 ON. Only PH1 can be connected to CN11 as I/O.
- SB48 ON. MCO is connected to PH0 and R5 on the STLINK-V3E side and must be connected to provide the MCO to the STLINK-V3E output.
- SB4 and SB5 OFF. The external crystal is not connected to HSE.
- Resistor (R5) and capacitor (C5) can be adapted for the 8Mhz shape.

External oscillator to PH0 (default: not connected)

The input clock comes from an external clock through PH0, on expansion connector (CN11) pin 29. The following configuration is needed:

- SB47 and SB49 ON. PH0 and PH1 are connected to CN11. PH1 can be used as a GPIO.
- SB48 OFF. MCO is not connected to PH0.
- SB4 and SB5 OFF. The external crystal (X3) is disconnected from PH0 and PH1.

HSE not used (configuration depends on the embedded STM32U5 series microcontroller)

PH0 and PH1 are used as GPIOs instead of crystal inputs. The following configuration is needed:

- SB47 and SB49 ON. PH0 and PH1 are connected to the expansion connector (CN11) as GPIOs.
- SB48 OFF. MCO is not connected to PH0.
- SB4 and SB5 OFF. The external crystal (X3) is disconnected from PH0 and PH1.

6.8 Reset sources

The reset signal of the Nucleo board is active LOW and the reset sources come from:

- The RESET button (B2)
- The embedded STLINK-V3E
- The ARDUINO®-included Zio connector CN8 pin 5
- The ST morpho connector CN11 pin 14

6.9 Virtual COM port (VCP)

An STM32 serial interface is connected to the STLINK-V3E debug interface. The user can choose between a USART or an LPUART interface.

The selection between USART and LPUART is performed by setting related solder bridges.

Refer to the tables below to set the USART or LPUART connection to the VCP interface

Table 10. USART1 connection

Solder bridge configuration(1)	Feature
SB32, SB34 ON **SB24 SB26 SB31 SB33 OFF**	**USART1 (PA9/PA10) connected to STLINK-V3E VCP**
SB31, SB33 ON SB25 SB27 SB32 SB34 OFF	USART1 (PA9/PA10) connected to Zio, ARDUINO® Uno V3 D0/D1

1. *The default configuration is in bold.*

Table 11. LPUART1 connection

Solder bridge configuration(1)	Feature
SB25, SB27 ON **SB24 SB26 SB31 SB33 OFF**	**LPUART1 (PG7/PG8) connected to Zio, ARDUINO® Uno V3 D0/D1**
SB24, SB26 ON SB25 SB27 SB32 SB34 OFF	LPUART1 (PG7/PG8) connected to STLINK-V3E VCP.

1. *The default configuration is in bold.*

By default:

- Serial communication between the target MCU and ST-LINK MCU is enabled on USART1 because this interface supports the bootloader mode.
- Serial communication between target MCU, ARDUINO® Uno V3, and ST morpho connectors is enabled on LPUART1, not to interfere with the VCP interface.

PG7 and PG8 are also connected to the ST morpho connector CN12 pins 66 (SB72) and 67 (SB73). The two solder bridges can be removed in case of conflict between ARDUINO® Uno V3 and ST morpho for PG7 or PG8.

6.10 Bootloader

The bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory via USART, I^2C, SPI, CAN FD, or USB FS in device mode through the device firmware upgrade (DFU). The bootloader is available on all devices. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

The Root Secure Services (RSS) are embedded in a flash area named secure information block, programmed during ST production. For example, it enables secure firmware installation (SFI), thanks to the RSS extension firmware (RSSe SFI). This feature allows customers to protect the confidentiality of the firmware to be provisioned into the STM32 when production is subcontracted to an untrusted third party. The RSS is available on all devices, after enabling the TrustZone® through the TZEN option bit.

The I/O PH3_BOOT0 gives external hardware access to the bootloader.

By default, this pin is set to level LOW by a pull-down resistor, to boot on the internal flash memory. It is possible to put this GPIO to level HIGH to boot on the system flash memory (bootloader), by connecting a 2.54-mm pitch jumper between the ST morpho connector (CN7) pin-7 and VDD pin 5.

As mentioned above, USART1 on PA9/PA10 is connected by default because this interface supports the bootloader mode.

6.11 USB Type-C® FS/HS

The STM32 Nucleo-144 board supports a USB interface. The USB connector (CN15) is a USB Type-C® connector.

This USB interface can be full speed (FS) or high speed (HS) depending on the embedded STM32U5 series microcontroller.

The NUCLEO-U575ZI-Q board embeds a USB full-speed (FS) interface and the NUCLEO-U5A5ZJ-Q board embeds a USB high-speed (HS) interface.

The STM32 Nucleo-144 board supports USB Type-C® sink power mode only.

The USB power green LED (LD7) lights up when V_{BUS} is powered by a USB host and the Nucleo-144 board works as a USB device.

6.11.1 USB FS/HS device

With a USB stack inside the STM32 and when a USB host connection to the USB Type-C® connector (CN15) of STM32 Nucleo-144 is detected, the STM32 Nucleo-144 board can be a USB device. Depending on the powering capability of the USB host, the board can be powered by the V_{BUS} terminal (CN15). In the board schematic diagrams, the corresponding power voltage line is called 5V_UCPD. The STM32 Nucleo-144 board supports a 5 V USB voltage from 4.75 to 5.5 V. MCU VDD_USB supports the 3V3 power source only. Section 6.4 provides information on how to use the powering options. The hardware configuration for the USB interface is shown in Table 12.

Table 12. Hardware configuration for the USB interface

I/O	Solder bridge	Setting	Configuration(1)
PA11	SB40	**OFF**	**PA11 is used as USB_FS_N diff pair interface. No more muxing.**
		ON	PA11 can be used as a USB data interface and is also available on the ST morpho connector. USB function can be used, but performances can be impacted due to the track length to the expansion connector causing impedance mismatch.
PA12	SB41	**OFF**	**PA12 is used as a USB_FS_P diff pair interface. No other muxing.**
		ON	PA12 can be used as a USB data interface and is also available on the ST morpho connector. USB function can be used, but performances can be impacted due to the track length to the expansion connector causing impedance mismatch.

1. *The default configuration is shown in bold.*

6.11.2 UCPD

The USB Type-C® introduces the USB Power Delivery feature. The STM32 Nucleo-144 implementation for the USB power delivery supports the dead battery and the sink mode with 5 V and 0.5 A (2.5 W).

In addition to the I/O DP/DM directly connected to the USB Type-C® connector, five I/Os are also used for UCPD configuration: configuration channel (CCx), VBUS-SENSE, UCPD dead battery (DBn), and UCPD_FAULT (FLT) feature.

To protect the STM32 Nucleo-144 from USB over-voltage, a Programmable Power Supply (PPS) compliant USB Type-C® port protection is used: TCPP01-M12 IEC6100-4-2 level 4-compliant IC.

- Configuration Channel I/O: UCPD_CCx: These signals are connected to the associated CCx line of the USB Type-C® connector through the STM USB port Protection TCPP01-M12. These lines are used for the configuration channel lines (CCx) to select the USB Type-C® current mode. The STM32 Nucleo-144 supports only sink current mode.
- Dead Battery I/O: UCPD_DBn: This signal is connected to the associated DBn line of the TCPP01-M12. The STM USB port protection TCPP01-M12 internally manages the dead battery resistors.

- V_{BUS} fault detection: UCPD_FLT: This signal is provided by the ST USB Type-C® port protection. It is used as fault reporting to MCU after a bad V_{BUS} level detection. By design, the STM32 Nucleo-144 V_{BUS} protection is set to 6 V maximum. (R41 is set to 2K7 to select 6 V maximum).

For more detail about UCPD with the TCPP01-M12 USB Type-C® port protection for sink application, refer to the application note *USB Type-C Power Delivery using STM32 MCUs and MPUs* (AN5225) related to USB Type-C® power delivery using STM32xx series.

Table 13 describes the hardware configuration for the UCPD feature.

Table 13. Hardware configuration for the UCPD feature

I/O	Solder bridge	Setting	Configuration(1)
PA15	SB42	OFF	PA15 Not connected to USB Type-C® port protection and used as T_JTDI (optional configuration with SB39)
		ON	**PA15 connected to USB Type-C® port protection and NOT used as T_JTDI**
	SB8	**OFF**	**PA15 connected to USB Type-C® port protection and used as UCPD_CC1**
		ON	PA15 directly connected to USB Type-C® connector. USB Type-C® port protection is bypassed.
PB15	SB9	**OFF**	**PB15 connected to USB Type-C® port protection and used as UCPD_CC2**
		ON	PB15 directly connected to USB Type-C® connector. USB Type-C® port protection is bypassed.
PC2	SB6	**ON**	**PC2 used as VBUS_SENSE**
		OFF	PC2 NOT used for UCPD. Can be used on the Zio connector (SB53)
PB5	SB46	**ON**	**IO UCPD_DBn connected to USB Type-C® port protection and used as a dead battery feature**
		OFF	PB5 not used for UCPD_DBn can be used as SAI or SPI on ZIO connector
	JP8	ON	UCPD_DBCC1 connected to GND (only for internal UCPD debug purpose)
		OFF	**UCPD_DBCC1 not connected to GND, can be used for Zio connector**
PB14	SB45	**ON**	**IO UCPD_FLT connected to USB Type-C® port protection and used as over-voltage fault reporting to MCU**
		OFF	PB14 not used for UCPD_FLT can be used on the ST morpho connector
	JP7	ON	UCPD_DBCC2 connected to GND (only for internal UCPD debug purpose)
		OFF	**UCPD_DBCC2 not connected to GND, can be used for the ST morpho connector**

1. *The default configuration is shown in bold*

6.11.3 USB Type-C® connector

Figure 14 shows the pinout of the USB Type-C® connector CN15.

Figure 14. USB Type-C® connector (CN15) pinout

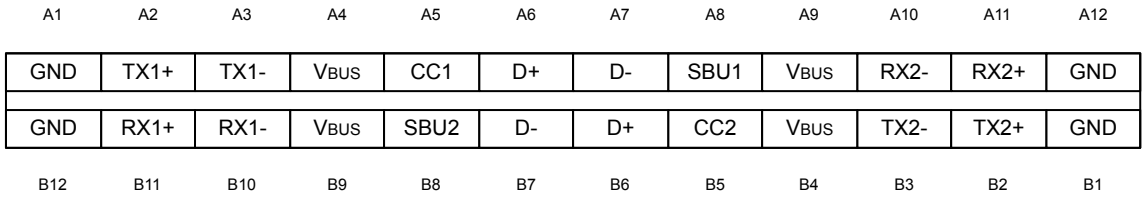


Table 14 describes the pinout of the USB Type-C® connector (CN15).

Table 14. USB Type-C® connector (CN15) pinout

STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin
-	GND	GND	A1	B12	GND	GND	-
-	-	TX1+	A2	B11	RX1+	-	-
-	-	TX1-	A3	B10	RX1-	-	-
-	VBUS_C/ 5V_USB_C	VBUS	A4	B9	VBUS	VBUS_C/ 5V_USB_C	-
PA15	UCPD_CC1	CC1	A5	B8	SBU2	-	-
PA12	USB_FS_P	D+	A6	B7	D-	USB_FS_N	PA11
PA11	USB_FS_N	D-	A7	B6	D+	USB_FS_P	PA12
-	-	SBU1	A8	B5	CC2	UCPD_CC2	PB15
-	VBUS_C/ 5V_USB_C	VBUS	A9	B4	VBUS	VBUS_C/ 5V_USB_C	-
-	-	RX2-	A10	B3	TX2-	-	-
-	-	RX2+	A11	B2	TX2+	-	-
-	GND	GND	A12	B1	GND	GND	-

7 Extension connectors

Six extension connectors are implemented on the STM32U5 Nucleo-144 board:

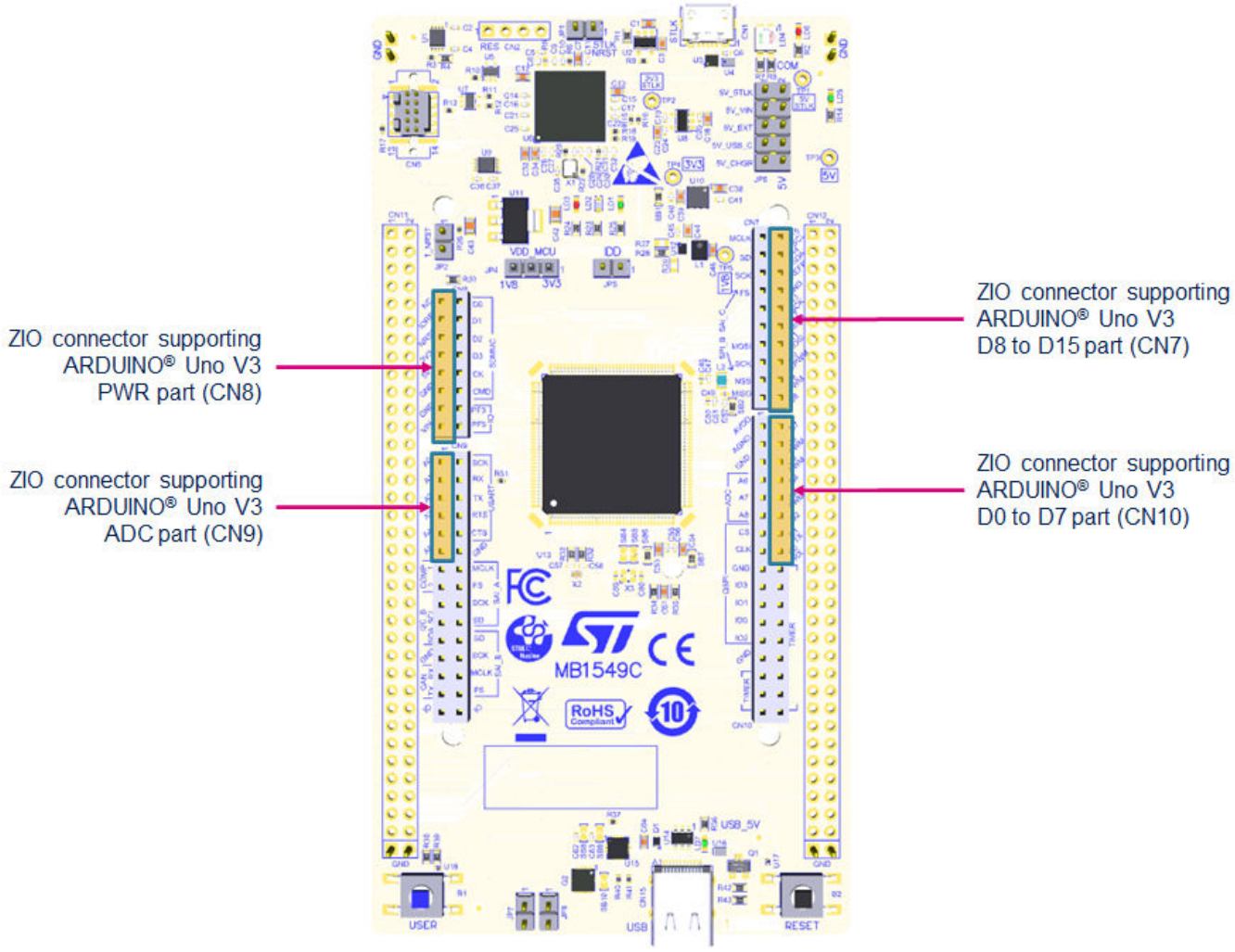
- Zio connectors (CN7, CN8, CN9, and CN10) supporting ARDUINO® Uno V3
- ST morpho connectors (CN11 and CN12)

7.1 Zio connectors supporting ARDUINO® Uno V3

The Zio connectors (CN7, CN8, CN9, and CN10) are female connectors supporting the ARDUINO® Uno V3 standard. Most shields designed for ARDUINO® can fit the Nucleo board.

Caution: Most of the STM32 microcontroller I/Os are 5 V-tolerant, but few of them are only 3V3-compatible, while ARDUINO® Uno V3 is 5 V-compatible. Refer to the STM32U5 series data brief and STM32U5xx product datasheets for their I/O structure.

Figure 15. Zio connectors supporting ARDUINO® Uno V3



The related pinout for the ARDUINO® connector is listed in Table 15, Table 16, Table 17, and Table 18.

Table 15. ARDUINO®-included Zio connector (CN7) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
SAI2_A	PC6	SAI_C_MCLK	D16	1	2	D15	I2C_A_SCL	PB8	I2C1
SAI2_A	PD11	SAI_C_SD	D17	3	4	D14	I2C_A_SDA	PB9	I2C1
SAI2_A	PB13	SAI_C_SCK	D18	5	6	VREFP	-	-	-
SAI2_A	PD12	SAI_C_FS	D19	7	8	GND	-	-	-
SAI1_B/ SPI3	PA4	SAI_D_FS	D20(7)	9	10	D13	SPI_A_SCK	PA5	SPI1
SAI1_B/ SPI3	PB4	SAI_D_MCLK	D21 (7)(8)	11	12	D12	SPI_A_MISO	PA6	SPI1
SAI1_B/ SPI3	PB5	SAI_D_SD/ SPI_B_MOSI	D22 (5)(7)(8)	13	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7	SPI1
SAI1_B/ SPI3	PB3	SAI_D_SCK/ SPI_B_SCK	D23(6) (7)(8)	15	16	D10	SPI_A_CS / TIM_B_PWM3(1)	PD14	SPI1/ TIM4_CH3
SAI1/SPI3	PA4	SPI_B_NSS	D24 (8)	17	18	D9	TIM_B_PWM2	PD15	TIM4_CH4
SAI1/SPI3	PB4	SPI_B_MISO	D25 (8)	19	20	D8	IO	PF12	-

1. *Due to muxing constraints, the SPI_NSS is not available as an alternate on this I/O, so this pin is affected by an I/O function to do the chip selection.*

A solder bridge (SB20) is used to disconnect the VREFP to the ARDUINO® connector CN7 pin 6.

- SB20 OFF: VREFP is not connected to the ARDUINO® connector CN7 pin 6 (Default configuration).
- SB20 ON: VREFP is connected to the ARDUINO® connector CN7 pin 6.

Table 16. ARDUINO®-included Zio connector (CN8) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
RES	-	NC	NC	1	2	D43	SDMMC_D0	PC8	SDMMC1
IO REF	-	IOREF	IOREF	3	4	D44	SDMMC_D1	PC9	SDMMC1
RESET	NRST	NRST	NRST	5	6	D45	SDMMC_D2	PC10	SDMMC1
3V3 I/O	-	3V3	3V3	7	8	D46	SDMMC_D3	PC11	SDMMC1
5V output	-	5V	5V	9	10	D47	SDMMC_CK	PC12	SDMMC1
GND	-	GND	GND	11	12	D48	SDMMC_CMD	PD2	SDMMC1
GND	-	GND	GND	13	14	D49	IO	PF3	-
VIN	-	VIN	VIN	15	16	D50	IO	PF5	-

Table 17. ARDUINO®-included Zio connector (CN9) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
ADC1_IN8	PA3	ADC	A0	1	2	D51	USART_B_SCLK	PD7	USART2
ADC1_IN7	PA2	ADC	A1(3)	3	4	D52	USART_B_RX	PD6	USART2
ADC1_IN4	PC3	ADC	A2	5	6	D53	USART_B_TX	PD5	USART2
ADC1_IN15	PB0	ADC	A3(3)	7	8	D54	USART_B_RTS	PD4	USART2
ADC1_IN2	PC1	ADC	A4	9	10	D55	USART_B_CTS	PD3	USART2
ADC1_IN1	PC0	ADC	A5	11	12	GND	-	-	-
COMP1	PB2	COMP1_INP	D72	13	14	D56	SAI_A_MCLK	PE2	SAI1_A
COMP2	PB6	COMP2_INP	D71	15	16	D57	SAI_A_FS	PE4	SAI1_A
I2C2	PF2	I2C_B_SMBA	D70	17	18	D58	SAI_A_SCK	PE5	SAI1_A
I2C2	PF1	I2C_B_SCL	D69	19	20	D59	SAI_A_SD	PE6	SAI1_A
I2C2	PF0	I2C_B_SDA	D68	21	22	D60 (7)	SAI_B_SD	PE3	SAI1_B
-	-	-	GND	23	24	D61 (7)	SAI_B_SCK	PF8	SAI1_B
CAN1	PD0	CAN_RX	D67	25	26	D62 (7)	SAI_B_MCLK	PF7	SAI1_B
CAN1	PD1	CAN_TX	D66	27	28	D63 (7)	SAI_B_FS	PF9	SAI1_B
-	PG0	IO	D65	29	30	D64	IO	PG1	-

Table 18. ARDUINO®-included Zio connector (CN10) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
AVDD	-	-	AVDD	1	2	D7	IO	PF13	IO
AGND	-	-	AGND	3	4	D6	TIM_A_PWM1	PE9	TIM1_CH1
GND	-	-	GND	5	6	D5	TIM_A_PWM2	PE11	TIM1_CH2
ADC1_IN16	PB1	ADC_A_IN	A6	7	8	D4	IO	PF14	IO
ADC1_IN3	PC2	ADC_B_IN	A7	9	10	D3	TIM_A_PWM3	PE13	TIM1_CH3
ADC1_IN6	PA1	ADC_C_IN	A8	11	12	D2	IO	PF15	IO
OCTOSPI1	PA2	OCTOSPI_CS	D26(3)	13	14	D1(1)	USART_A_TX	PG7(2)	LPUART1
OCTOSPI1	PB10	OCTOSPI_CLK	D27(4)	15	16	D0(1)	USART_A_RX	PG8(2)	LPUART1
-	-	-	GND	17	18	D42	TIM_A_PWM1N	PE8	TIM1_CH1N
OCTOSPI1	PE15	OCTOSPI_IO3	D28(4)	19	20	D41	TIM_A_ETR	PE7	TIM1_ETR
OCTOSPI1	PB0	OCTOSPI_IO1	D29(3)	21	22	GND	-	-	-
OCTOSPI1	PE12	OCTOSPI_IO0	D30(4)	23	24	D40	TIM_A_PWM2N	PE10	TIM1_CH2N
OCTOSPI1	PE14	OCTOSPI_IO2	D31(4)	25	26	D39(4)	TIM_A_PWM3N	PE12	TIM1_CH3N
-	-	-	GND	27	28	D38(4)	TIM_A_BKIN2	PE14	TIM1_BKIN2
TIM2_CH1	PA0	TIM_C_PWM1	D32	29	30	D37(4)	TIM_A_BKIN1	PE15	TIM1_BKIN
TIM1_CH1	PA8	TIM_D_PWM1	D33	31	32	D36(4)	TIM_C_PWM2	PB10	TIM2_CH3
TIM4_ETR	PE0	TIM_B_ETR	D34	33	34	D35	TIM_C_PWM3	PB11	TIM2_CH4

1. *The default configuration for the D0/D1 signal is LPUART1 on PG7 and PG8, USART1 on PA9 and PA10 is connected by default on STLINK-V3E.*

2. *PG2 to PG15 can have a different I/O level from other I/Os because supplied by VDDIO.*
3. *I/O shared between ADC and OCTOSPI (exclusive)*
4. *I/O shared between OCTOSPI and motor control (exclusive)*
5. *I/O shared between SAI_D, SPI_B, and UCPD function (exclusive)*
6. *I/Os are shared between SAI and JTAG SWO (exclusive)*
7. *SAI_D and SAI_B groups are on the same SAI instance (exclusive).*
8. *SAI_D group is shared with the SPI_B group, (exclusive).*

Note: The OCTOSPI interface is used in quad-mode communication without DQS to support Quad-SPI memories.

7.2 ST morpho headers (CN11 and CN12)

The ST morpho consists of CN11 and CN12 male pin header footprints (not soldered by default). They can be used to connect the STM32 Nucleo-144 board to an extension board or a prototype/wrapping board placed on top of the STM32 Nucleo-144 board. All signals and power pins of the STM32 are available on the ST morpho connector. An oscilloscope, a logic analyzer, or a voltmeter can also probe this connector.

Figure 16. ST morpho connector

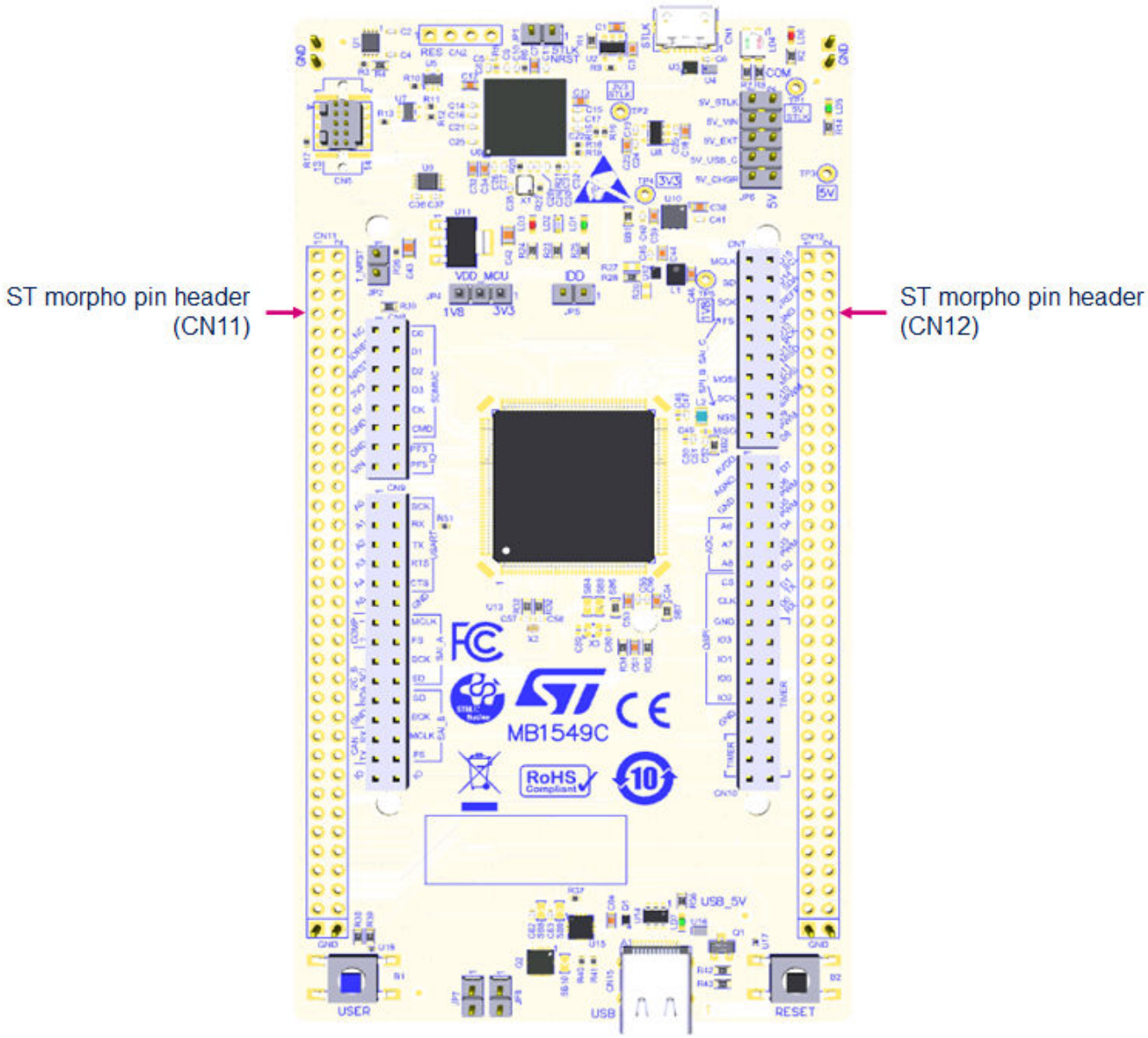


Table 19 shows the pin assignments for the STM32 on the ST morpho connector.

Table 19. ST morpho connector pin assignment

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	PC10	2	PC11	1	PC9	2	PC8
3	PC12	4	PD2	3	PB8	4	PC6
5	VDD	6	5V_EXT	5	PB9	6	NC
7	PH3_BOOT0(1)	8	GND	7	VREFP(2)	8	5V_STLK(3)
9	PF6	10	NC	9	GND	10	PD8
11	PF7	12	IOREF	11	PA5	12	PA12
13	PA13(4)	14	NRST	13	PA6	14	PA11
15	PA14(4)	16	3V3	15	PA7	16	NC
17	PA15	18	5V	17	PB6	18	PB11
19	GND	20	GND	19	PC7	20	GND
21	PB7	22	GND	21	PA9	22	PB2
23	PC13	24	VIN	23	PA8	24	PB1
25	PC14	26	NC	25	PB10	26	PB15
27	PC15	28	PA0	27	PB4	28	PB14
29	PH0	30	PA1	29	PB5	30	PB13
31	PH1	32	PA4	31	PB3	32	AGND
33	VBAT	34	PB0	33	PA10	34	NC
35	PC2	36	PC1	35	PA2	36	PF5
37	PC3	38	PC0	37	PA3	38	PF4
39	PD4	40	PD3	39	GND	40	PE8
41	PD5	42	PG2(5)	41	PD13	42	PF10
43	PD6	44	PG3(5)	43	PD12	44	PE7
45	PD7	46	PE2	45	PD11	46	PD14
47	PE3	48	PE4	47	PE10	48	PD15
49	GND	50	PE5	49	PE12	50	PF14
51	PF1	52	PF2	51	PE14	52	PE9
53	PF0	54	PF8	53	PE15	54	GND
55	PD1	56	PF9	55	PE13	56	PE11
57	PD0	58	PG1	57	PF13	58	PF3
59	PG0	60	GND	59	PF12	60	PF15
61	PE1	62	PE6	61	PG14(5)	62	PF11
63	PG9(5)	64	PG15(5)	63	GND	64	PE0
65	PG12(5)	66	PG10(5)	65	PD10	66	PG8(5)
67	NC	68	PG13(5)	67	PG7(5)	68	PG5(5)
69	PD9	70	NC	69	PG4(5)	70	PG6(5)

1. *The default state of BOOT0 is 0. It can be set to 1 when a jumper is plugged into pins 5-7 of CN11.*
2. *V_{REFP} is not connected to CN12 by default (SB20 OFF).*
3. *5V_STLK is the 5V power signal, coming from the STLINK-V3E USB connector. It rises before the 5V signal of the board.*
4. *PA13 and PA14 are shared with SWD signals connected to STLINK-V3E.*
5. *PG2 to PG15 can be set to different I/O levels, thanks to the SB selecting the source for VDDIO2.*

7.3 Solder bridge configuration for the expansion connector

Table 20 details the solder bridges of the STM32U5 Nucleo-144 board for the expansion connector.

Table 20. Solder bridge configuration

Definition	Bridge	Setting(1)	Comment
IOREF selection	SB16	**OFF**	**IOREF is not connected to the 1V8 power supply.**
		ON	IOREF is connected to the 1V8 power supply.
	SB17	OFF	IOREF is not connected to the VDD power supply.
		ON	**IOREF is connected to the VDD power supply.**
	SB18	**OFF**	**IOREF is not connected to the 3V3 power supply.**
		ON	IOREF is connected to the 3V3 power supply.
SDMMC IO PC8/PC9	SB19	OFF	PC8 is not connected to ST morpho CN12 pin 2 to avoid stub on Zio CN8 SDMMC_D0.
		ON	**PC8 is connected to ST morpho CN12 pin 2 and Zio CN8 pin 2: SDMMC_D0 signal quality can be impacted.**
	SB22	OFF	PC9 is not connected to ST morpho CN12 pin 1 to avoid stub on Zio CN8 SDMMC_D1.
		ON	**PC9 is connected to ST morpho CN12 pin 1 and Zio CN8 pin 4. SDMMC_D1 signal quality can be impacted.**
ADC-A3 / OCTOSPI_IO1 PB0	SB63	OFF	PB0 is not used as OCTOSPI_IO1.
		ON	**PB0 is used as OCTOSPI_IO1.**
	SB64	OFF	PB0 is not connected to ARDUINO® A3
		ON	**PB0 is connected to ARDUINO® A3.**
	SB65	OFF	PB0 is not connected to ST morpho pin 34.
		ON	**PB0 is connected to ST morpho pin 34.**
ADC_A1 / OCTOSPI_CS PA2	SB56	OFF	PA2 is not connected to Zio OCTOSPI_CS.
		ON	**PA2 is connected to Zio OCTOSPI_CS.**
	SB57	OFF	PA2 is not connected to ARDUINO® A1.
		ON	**PA2 is connected to ARDUINO® A1.**
ADC-A7 / VBUS_SENSE PC2	SB53	OFF	PC2 is not connected to ADC_A7 on the Zio connector and is used as USB Type-C® VBUS_SENSE (SB6).
		ON	**PC2 is connected to ADC_A7 on the Zio connector.**
Zio SAI_D / SPI_B interface	SB35	OFF	PA4 is not connected to Zio CN7 pin 9 for the SAI_D interface.
		ON	**PA4 is connected to Zio CN7 pin 9 for the SAI_D interface.**
	SB38	OFF	PA4 is not connected to Zio CN7 pin 17 for the SPI_B interface.
		ON	**PA4 is connected to Zio CN7 pin 17 for the SPI_B interface.**
	SB36	OFF	PB4 is not connected to Zio (CN7) for the SAI_D interface.
		ON	**PB4 is connected to Zio (CN7) for the SAI_D interface.**
	SB43	OFF	PB4 is not connected to Zio (CN7) for the SPI_B interface.
		ON	**PB4 is connected to Zio (CN7) for the SPI_B interface.**
	SB37	OFF	PB5 is not connected to Zio (CN7) for the SPI_B interface: Reserved for UCPD_DBCC1.
		ON	**PB5 is connected to Zio (CN7) for the SPI_B interface, shared with UCPD_DBn and UCPB_DBCC1.**

Definition	Bridge	Setting(1)	Comment
OCTOSPI_CLK / TIMER_C_PWM2 PB10	SB61	OFF	PB10 is not used as OCTOSPI_CLK.
		ON	**PB10 is used as OCTOSPI_CLK.**
	SB62	OFF	PB10 is not used as a TIMER for motor control.
		ON	**PB10 is used as a TIMER for motor control.**
TIMER_C_PWM1 / User-Button PA0	SB60	OFF	PA0 is not used as a TIMER for motor control, reserved for the user button.
		ON	**PA0 can be used as a TIMER for motor control, but cannot be used as a user button.**
OCTOSPI_IO3 / TIMER_A_BKIN1 PE15	SB66	OFF	PE15 is not used as OCTOSPI_IO3.
		ON	**PE15 is used as OCTOSPI_IO3.**
	SB67	OFF	PE15 is not used as a TIMER for motor control.
		ON	**PE15 is used as a TIMER for motor control.**
OCTOSPI_IO0 / TIMER_A_PWM3N PE12	SB68	OFF	PE12 is not used as OCTOSPI_IO0.
		ON	**PE12 is used as OCTOSPI_IO0.**
	SB69	OFF	PE12 is not used as a TIMER for motor control.
		ON	**PE12 is used as a TIMER for motor control.**
OCTOSPI_IO2 / TIMER_A_BKIN2 PE14	SB70	OFF	PE14 is not used as OCTOSPI_IO2.
		ON	**PE14 is used as OCTOSPI_IO2.**
	SB71	OFF	PE14 is not used as a TIMER for motor control.
		ON	**PE14 is used as a TIMER for motor control.**

1. *The default configuration is in bold.*

Note: The OCTOSPI interface is used in quad-mode communication without DQS to support Quad-SPI memories.

8 STM32U5 Nucleo-144 board (MB1549) product information

8.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

- First sticker: product order code and product identification, generally placed on the main board featuring the target device.
  Example:

Product order code Product identification

- Second sticker: board reference with revision and serial number, available on each PCB.
  Example:

MBxxxx-Variant-yzz syywwxxxxx	

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: *"MBxxxx-Variant-yzz"*, where *"MBxxxx"* is the board reference, *"Variant"* (optional) identifies the mounting variant when several exist, *"y"* is the PCB revision, and *"zz"* is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as *"ES"* or *"E"* are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"ES" or *"E"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

8.2 STM32U5 Nucleo-144 board (MB1549) product history

Table 21. Product history

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-U575ZI-Q	NUU575ZIQ$AT1	MCU: STM32U575ZIT6Q silicon revision "X" MCU errata sheet: *STM32U575xx and STM32585xx device errata* (ES0499) Board: MB1549-C02	Initial revision for Nucleo-144 embedded STM32U575ZIT6Q MCU with a USB full-speed interface	Bootloader communication interfaces are not available if TZEN=1. When TrustZone® is enabled and boot from system memory is selected (BOOT0 = 1) to use the bootloader, the ST embedded bootloader is blocked, thus making all the bootloader interfaces no more usable (USB-DFU, USART, SPI, I²C, and CAN FD). As a consequence, the SFI (secure firmware install) using bootloader communication interfaces does not work, and the option bytes cannot be changed using the bootloader interface. SFI and option bytes change using JTAG/SWD interface remains functional. There is no workaround to this limitation solved in the NUU575ZIQ$AT2 product identification.
	NUU575ZIQ$AT2	MCU: STM32U575ZIT6Q silicon revision "X" MCU errata sheet: *STM32U575xx and STM32585xx device errata* (ES0499) Board: MB1549-C03	The bootloader revision embedded on this STM32U575ZIT6Q integrates the correction for the bootloader communication interfaces when TZEN=1.	No limitation
NUCLEO-U5A5ZJ-Q	NUU5A5ZJQ$AT1	MCU: STM32U5A5ZJT6Q silicon revision "C" MCU errata sheet: *STM32U575xx and STM32585xx device errata* (ES0499) Board: MB1549-C04	Initial revision for Nucleo-144 embeds the STM32U5A5ZJT6Q MCU with USB high-speed interface.	The STM32U5A5ZJT6Q silicon revision “C” embedded on the NUCLEO-U5A5ZJ-Q with the NUU5A5ZJQ$AT1 product identification does not support the SFI. This limitation is solved on the NUU5A5ZJQ$AT2 product identification.
	NUU5A5ZJQ$AT2	MCU: STM32U5A5ZJT6Q silicon revision "X" MCU errata sheet: *STM32U575xx and STM32585xx device errata* (ES0499) Board: MB1549-C04	The STM32U5A5ZJT6Q silicon revision “X” embedded on NUCLEO-U5A5ZJ-Q with the NUU5A5ZJQ$AT2 product identification supports the SFI.	No limitation

8.3 Board revision history

Table 22. **Board revision history**

Board reference	Board variant and revision	Board change description	Board limitations
MB1549	C02	Initial revision	SWDIO: Because of the level shifter to support 1V8 MCU debugging, it is recommended to set the SWDIO frequency to 8 MHz.
	C03	BOM improvement: • Update C57 and C58 capacitors from 4.7 to 1.8 pF for 32 KHz CLOAD adaptation • Include STM32U575ZIT6Q with new embedded RSS	SWDIO: Because of the level shifter to support 1V8 MCU debugging, it is recommended to set the SWDIO frequency to 8 MHz.
	C04	BOM improvement: • Update C57 and C58 capacitors from 1.8 to 6.8 pF 32 KHz CLOAD link to STM32 32 KHz update • Update the user button management with debounce SW (removed C84, R38) and update R39 to 0 Ω	SWDIO: Because of the level shifter to support 1V8 MCU debugging, it is recommended to set the SWDIO frequency to 8 MHz.

9 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

9.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible party (in the USA)

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9.2 ISED Compliance Statement

ISED Canada ICES-003 Compliance Label: *CAN ICES-3 (B) / NMB-3 (B)*.

Étiquette de conformité à la NMB-003 d'ISDE Canada: *CAN ICES-3 (B) / NMB-3 (B)*.

Revision history

Table 23. **Document revision history**

Date	Version	Changes
24-Jun-2021	1	Initial release.
13-Sep-2021	2	Added *Product limitation* to the *NUU575ZIQ$AT1 product identification* and *NUU575ZIQ$AT2 product identification* solving this limitation.
13-Apr-2022	3	Added *Board MB1549-C03*. Updated *Table 18* and *Table 20* for the OCTOSPI interface.
27-Jan-2023	4	Added *NUCLEO-U5A5ZJ-Q* new product. Updated *Hardware block diagram*, *Embedded STLINK-V3E* with former *Figure 7* removed, *Power supply and power selection*, and *STM32U5 Nucleo-144 board (MB1549) product information* with new *Table 21* and *Table 22*.
23-Feb-2023	5	Updated *Table 16* titles. Removed *CE conformity*.
29-Mar-2023	6	Updated crystal characteristics in OSC clock sources.

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