DATA ITEM DESCRIPTION

Title: TIMING CONSTRAINT VALIDATION (TCV)

The Timing Constraint Validation (TCV) provides a method to verify timing constraints have been properly derived and applied. Visualizations are provided to convey certain aspects of timing to improve understanding for the reader.

Requirements:

1. Content

1. Scope. This section shall be divided into the following paragraphs.

1.1 Identification. This paragraph shall identify the system for which the timing analysis is performed.

1.2 Document Overview. This paragraph shall summarize the purpose and contents of this document.

2. Reference Documents. This section shall include a list of all datasheets referenced in this document with title, revision and date. The name, location and hash of all timing reports shall be listed. The name, location and hash of all board timing reports shall be listed. A part number for the released device shall be listed.

3. Timing Constraint Analysis. This section shall include the following subsections. This is the main analysis section of the DID.

3.1 External Interface Identification. This paragraph shall include a list of all interfaces which are analyzed in this document.

3.x Interface Analysis. This section shall include the following subparagraphs

3.x.1 Overview. This paragraph shall include a description of the interface. It shall identify the type of interface (source synchronous, double data rate, etc…) This section shall include a diagram showing the devices and pins included in the analysis. The devices shall be labeled. External traces shall be named.

3.x.2 Timing Parameters. This paragraph shall include the following items:

a. External setup and hold constraints. Use the same names that are in the data sheet.
b. Trace length min and max delays.

3.x.3 Clock and Edge identification. This section shall include the following items:

a. Clock identification (include the name, frequency and diagram showing both launching and capture clocks).

b. Edge identification (The launching clock edge shall be numbered. The capturing clock edge shall be lettered. The edges involved in setup checks shall be identified. The edges involved in hold checks shall be identified. Double Data rate edges shall be identified.).

3.x.2.1 General Equations. This section shall include the following items:

a. Diagram showing all elements in the data and clock paths inside both devices and between the devices. (clock elements, pads and flip flops.) This is a representational diagram which will be used as a reference for constraint generation. This diagram can be the same in section 3.x.1.

b. Derive setup equations for all paths using elements referenced from the diagram.

c. Derive hold equations for all paths using elements referenced from the diagram.

3.x.2.2 Output Delay Calculation. This section shall include the following items:

a. Derive output delay max equations for all paths from setup equation in previous section.

b. Derive output delay min equations for all paths from hold equation in previous section.

3.x.2.3 Input Delay Calculation. This section shall include the following items:

a. Derive input delay max equations for all paths from setup equation in previous section.

b. Derive input delay min equation for all paths from hold equation in previous section.

3.x.3 Validation. This section shall include the following subsections:

3.x.3.1 Timing Report Checks. This section shall include the following items:

a. Data and clock path have the same source

b. Clock Recovery Pessimism Removal analysis (Does the clock portion of the data path match the part of the clock path.)

c. Clock Path Validation (Can the output clock be traced to an external pin)

d. Data Path Validation (Can the data be traced to an external pin)

e. Input/Output delay validation (Are the output and input delays calculated in the previous section found in the timing reports.)

f. Clock edge validation (Are the correct timing edges being used.)

g. Clock paths are the same for hold and setup

h. Check process corners

3.x.3.2 Timing Path Visualizations. This section shall include the following items. This section will provide visualizations to assist the reader in gaining understanding aspects of the timing paths.

a. Diagram showing relationship between clock and datapath

b. Datapath fanout distribution

c. Datapath latency distribution

d. CRPR point as % of clock path.

3.x.4 Results. This section shall include the following items:

a. Diagram showing an eye pattern for all timing paths over PVT. Busses shall be combined into a single

b. Indicate timing margins.