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74VHC4066
Quad Analog Switch

General Description

These devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the 4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The 4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

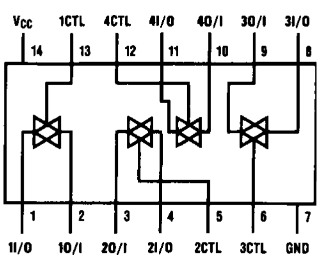
- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μA maximum (74VHC)
- Matched switch characteristics
- Individual switch controls
- Pin and function compatible with the 74HC4066

Ordering Code:

Order Number	Package Number	Package Description
74VHC4066M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74VHC4066MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC4066N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

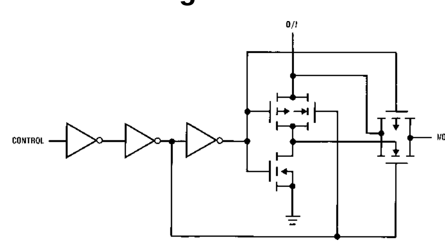
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Top View

Schematic Diagram



Truth Table

Input	Switch
CTL	**I/O–O/I**
L	"OFF"
H	"ON"

Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	–0.5 to +15V
DC Control Input Voltage (V_{IN})	–1.5 to V_{CC} + 1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE} – 0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	–40	+85	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 9.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	T_A=–40 to 85°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			9.0V		6.3	5.3	V
			12.0V		8.4	8.4	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			9.0V		2.7	2.7	V
			12.0V		3.6	3.6	V
R_{ON}	Maximum "ON" Resistance See (Note 5)	$V_{CTL} = V_{IH}$, I_S = 2.0 mA	4.5V	100	170	200	Ω
		$V_{IS} = V_{CC}$ to GND	9.0V	50	85	105	Ω
		(*Figure 1*)	12.0V	30	70	85	Ω
			2.0V	120	180	215	Ω
		$V_{CTL} = V_{IH}$, I_S = 2.0 mA	4.5V	50	80	100	Ω
		$V_{IS} = V_{CC}$ or GND	9.0V	35	60	75	Ω
		(*Figure 1*)	12.0V	20	40	60	Ω
R_{ON}	Maximum "ON" Resistance Matching	$V_{CTL} = V_{IH}$	4.5V	10	15	20	Ω
		$V_{IS} = V_{CC}$ to GND	9.0V	5	10	15	Ω
			12.0V	5	10	15	Ω
I_{IN}	Maximum Control Input Current	$V_{IN} = V_{CC}$ or GND; V_{CC} = 2 – 6V			±0.05	±0.5	µA
I_{IZ}	Maximum Switch "OFF" Leakage Current	$V_{OS} = V_{CC}$ or GND	6.0V	10	±60	±600	nA
		V_{IS} = GND or V_{CC}	9.0V	15	±80	±800	nA
		$V_{CTL} = V_{IL}$ (*Figure 2*)	12.0V	20	±100	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	$V_{IS} = V_{CC}$ to GND	6.0V	10	±40	±150	nA
		$V_{CTL} = V_{IH}$	9.0V	15	±50	±200	nA
		V_{OS} = OPEN (*Figure 3*)	12.0V	20	±60	±300	nA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	6.0V		1.0	10	µA
		I_{OUT} = 0 µA	9.0V		2.0	20	µA
			12.0V		4.0	40	µA

Note 4: For a power supply of 5V ± 10% the worst case on resistance (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC} – GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–12V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		T_A=–40 to 85°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		3.3V	25	30	20	ns
			4.5V	5	10	13	ns
			9.0V	4	8	10	ns
			12.0V	3	7	11	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	3.3V	30	58	73	ns
			4.5V	12	20	25	ns
			9.0V	6	12	15	ns
			12.0V	5	10	13	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	3.3V	60	100	125	ns
			4.5V	25	36	45	ns
			9.0V	20	32	40	ns
			12.0V	15	30	38	
	Minimum Frequency Response (*Figure 7*) 20 log(V_O/V_I) = –3 dB	R_L = 600Ω	4.5V	40			MHz
		V_{IS} = 2 V_{PP} at (V_{CC}/2) (Note 6)(Note 7)	9.0V	100			MHz
	Crosstalk Between any Two Switches (*Figure 8*)	R_L = 600Ω, F = 1 MHz (Note 7)(Note 8)	4.5V	–52			dB
			9.0V	–50			dB
	Peak Control to Switch Feedthrough Noise (*Figure 9*)	R_L = 600Ω, F = 1 MHz	4.5V	100			mV
		C_L = 50 pF	9.0V	250			mV
	Switch OFF Signal Feedthrough Isolation (*Figure 10*)	R_L = 600Ω, F = 1 MHz $V_{(CT)}$ V_{IL} (Note 7)(Note 8)	4.5V	–42			dB
			9.0V	–44			dB
THD	Total Harmonic Distortion (*Figure 11*)	R_L = 10 kΩ, C_L = 50 pF, F = 1 kHz V_{IS} = 4 V_{PP}	4.5V	.013			%
		V_{IS} = 8 V_{PP}	9.0V	.008			%
C_{IN}	Maximum Control Input Capacitance			5	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			20			pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		0.5			pF
C_{PD}	Power Dissipation Capacitance			15			pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation).

Note 7: V_{IS} is centered at V_{CC}/2.

Note 8: Adjust input for 0 dBm.

AC Test Circuits and Switching Time Waveforms

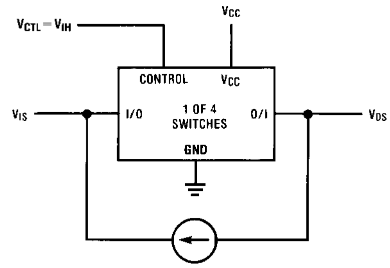


FIGURE 1. "ON" Resistance

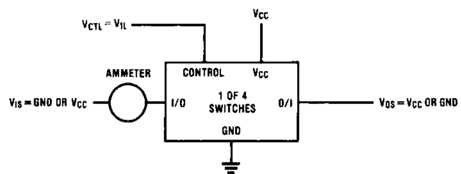


FIGURE 2. "OFF" Channel Leakage Current

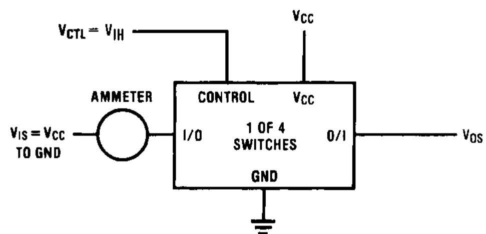


FIGURE 3. "ON" Channel Leakage Current

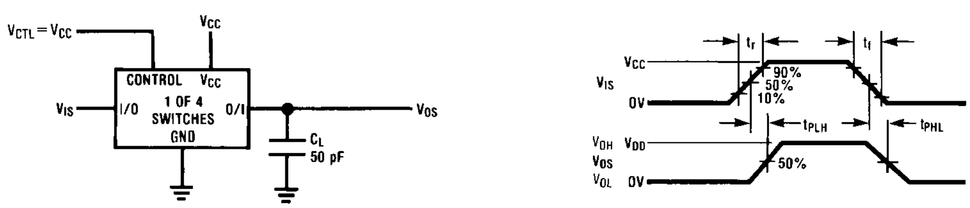


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

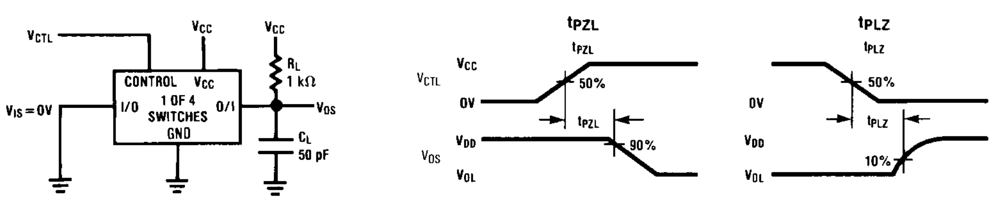


FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

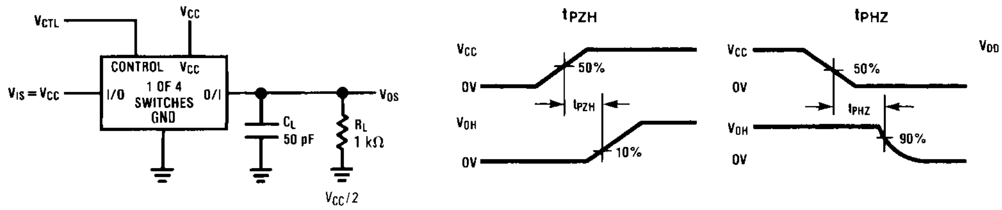


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

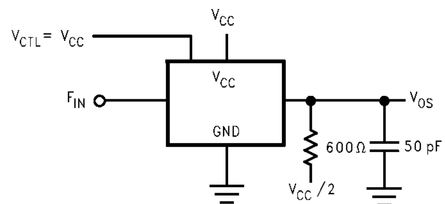


FIGURE 7. Frequency Response

Crosstalk and Distortion Test Circuits

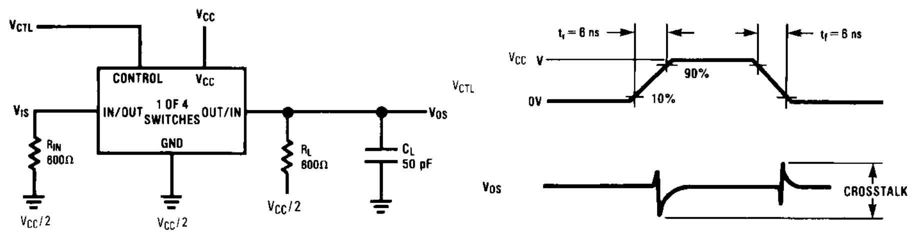


FIGURE 8. Crosstalk: Control Input to Signal Output

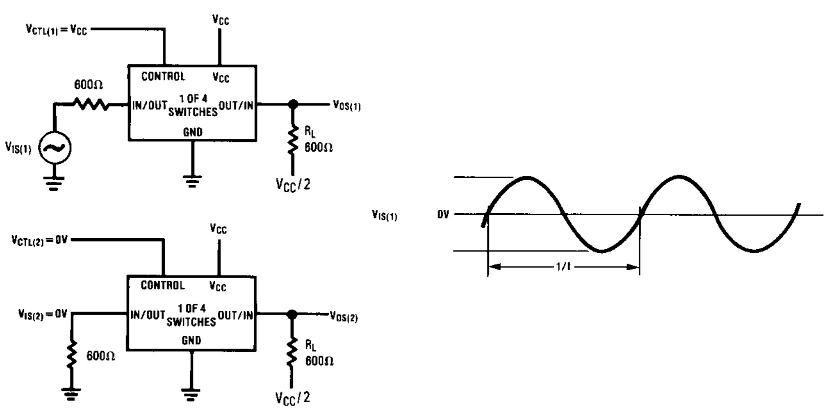


FIGURE 9. Crosstalk Between Any Two Switches

Crosstalk and Distortion Test Circuits (Continued)

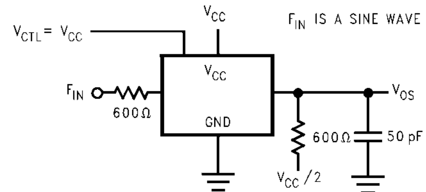


FIGURE 10. Switch OFF Signal Feedthrough Isolation

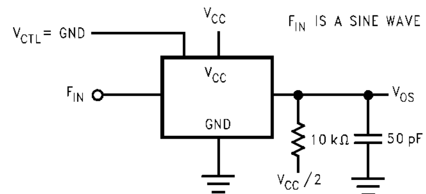
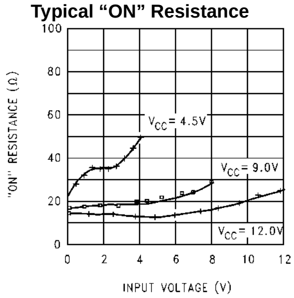


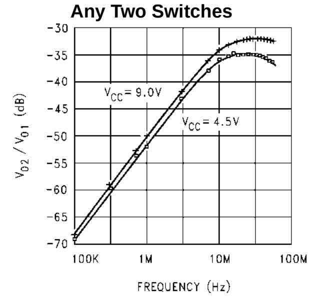
FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

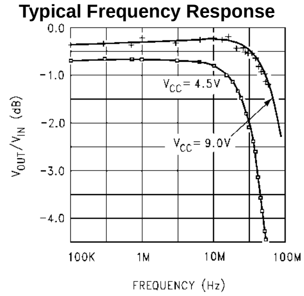
Typical "ON" Resistance



Typical Crosstalk Between Any Two Switches



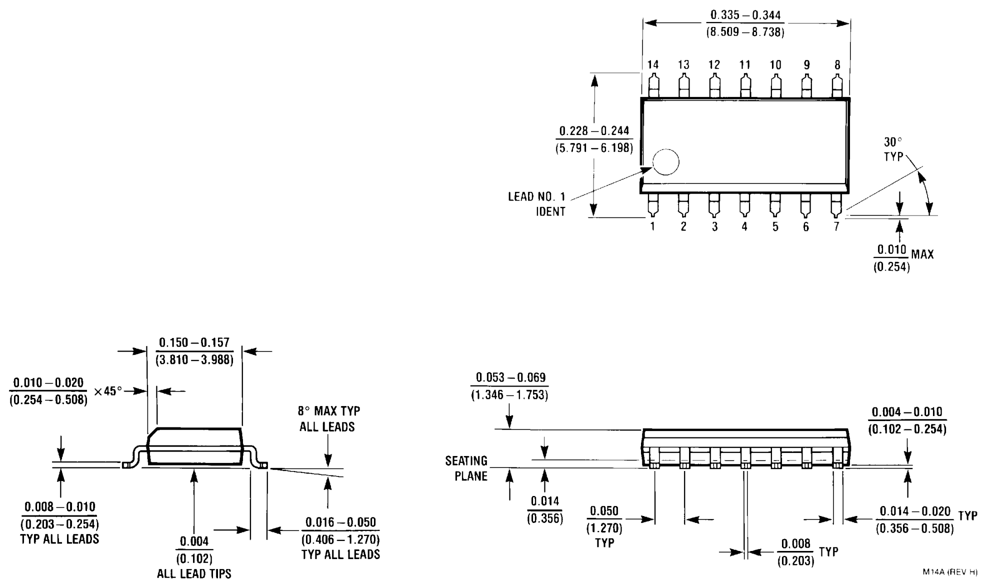
Typical Frequency Response



Special Considerations

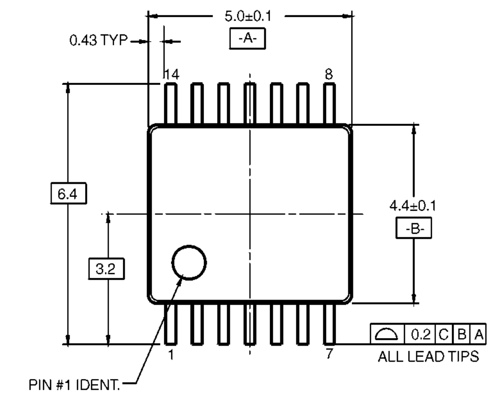
In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

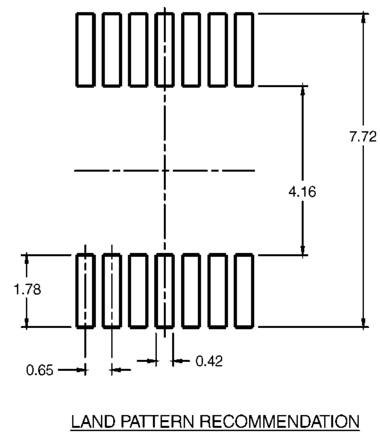
Physical Dimensions inches (millimeters) unless otherwise noted

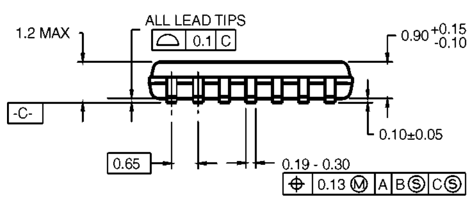


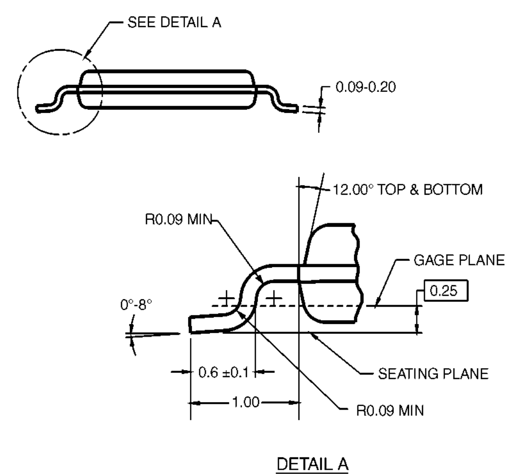
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)









NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

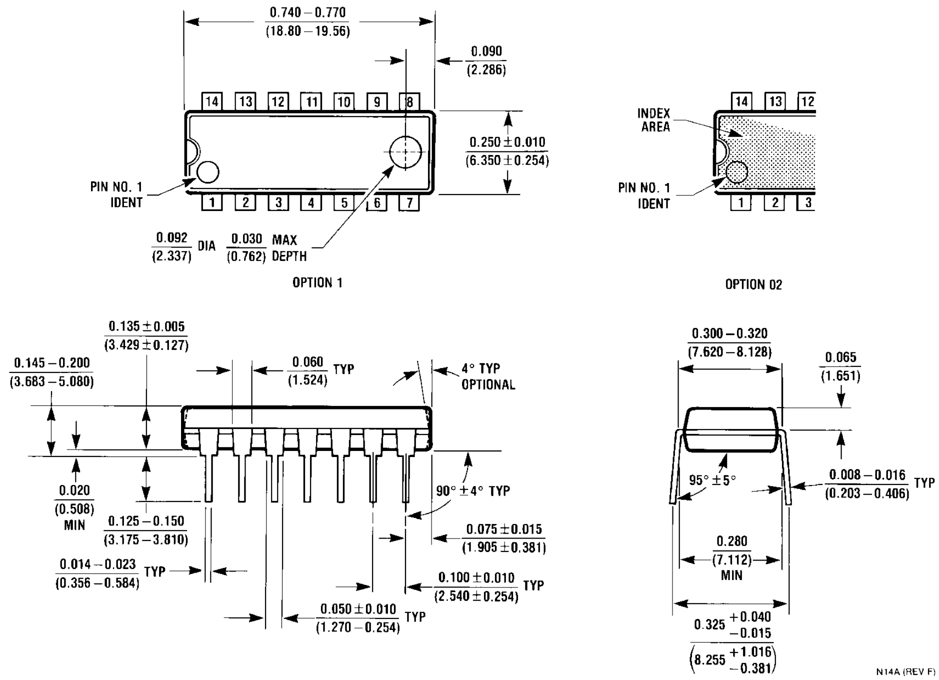
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A