A Fully Reconfigurable Low-Noise Biopotential Sensing Amplifier With 1.96 Noise Efficiency Factor

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***Abstract*—A fully reconfigurable biopotential sensing amplifier utilizing floating-gate transistors is presented in this paper. By using the complementary differential pairs along with the current reuse technique, the theoretical limit for the noise efficiency factor of the proposed amplifier is below 1.5. Without consuming any extra power, floating-gate transistors are employed to program the low-frequency cutoff corner of the amplifier and to implement the common-mode feedback. A concept proving prototype chip was designed and fabricated in a 0.35 μm CMOS process occupying 0.17 mm^2 silicon area. With a supply voltage of 2.5 V, the measured midband gain is 40.7 dB and the measured input-referred noise is 2.8μV_{rms}. The chip was tested under several configurations with the amplifier bandwidth being programmed to 100 Hz, 1 kHz, and 10 kHz. The measured noise efficiency factors in these bandwidth settings are 1.96, 2.01, and 2.25, respectively, which are among the best numbers reported to date. The measured common-mode rejection and the supply rejection are above 70 dB. When the bandwidth is configured to be 10 kHz, the dynamic range measured at 1 kHz is 60 dB with total harmonic distortion less than 0.1%. The proposed amplifier is also demonstrated by recording electromyography (EMG), electrocardiography (ECG), electrooculography (EOG), and electroencephalography (EEG) signals from human bodies.**

***Index Terms*—Biopotential sensing amplifier, common-mode feedback, floating-gate circuit, low-noise amplifier, low-power amplifier, noise efficiency factor, reconfigurable circuit.**

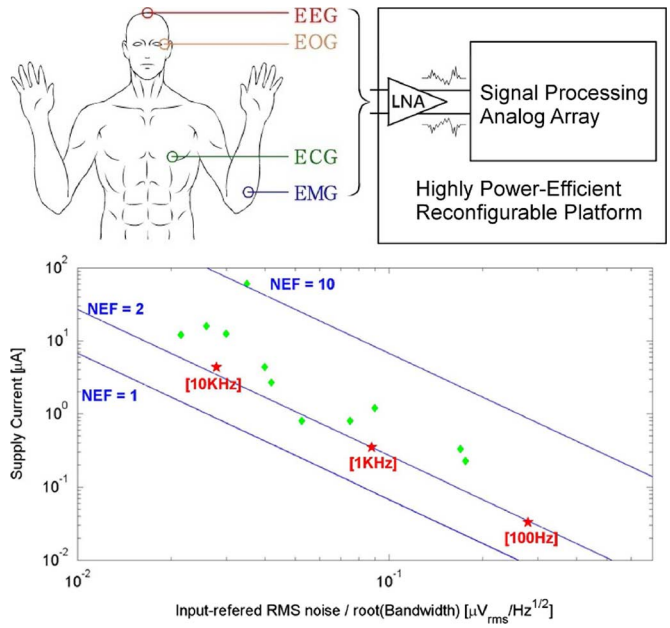

Fig. 1. The proposed amplifier can be followed by a signal processing analog array and integrated into a highly power-efficient reconfigurable computation platform. The noise efficiency factor (NEF) of the proposed amplifier was evaluated with the bandwidth being configured to 10 kHz, 1 kHz, and 100 Hz. The bottom plot shows the efficiency comparison between this work (marked by asterisks) and other recent works (marked by diamonds) in NEF contours.

I. Introduction

REMARKABLE advances in wearable and implantable devices that record physiological signals have brought about revolutionary improvements in a variety of biomedical applications, such as health monitoring [1], disease detection [2], neural prostheses [3], [4], and brain stimulation therapies [5], [6]. It is critical for these sensing devices to have a small form factor and low power consumption while enabling unobtrusive and chronic monitoring. Particularly for implanted devices, the power dissipation from these electronics must be low enough to avoid excess heat flux tissue damage. Because the sensing amplifiers usually dominate the power and the noise performance of the recording frontend, significant research activity has been focused on designing this crucial circuit block [2], [7]–[15].

Under stringent area and power constraints, neural recording amplifiers have the most challenging specifications [16]. It is necessary to provide a high amplification gain with low electronic noise to extract weak extracellular neural signals, which have amplitudes around tens of micro-volts. Since the circuit input-referred noise can be depressed by consuming more current, the noise efficiency factor (NEF) [17] has been widely utilized as the figure-of-merit to quantify this tradeoff. A small NEF value is preferred in designing neural sensing amplifiers. To prevent the amplifier outputs from being saturated, it is necessary to reject the drifting DC offset stemming from the binding and unbinding reactions on the electrode surface. Additionally, a large dynamic range with high linearity is required to avoid the aliasing and mixing between the rapid action potentials (200 Hz–10 kHz) and the low-frequency local field potentials (0.1 Hz–200 Hz) [13]. Furthermore, the sensing

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amplifier needs a high common-mode rejection ratio (CMRR) to suppress the 50/60 Hz power line interference, and a high power-supply rejection ratio (PSRR) to minimize the effects of the noise and disturbance from the power source.

Besides the neural signals, there are many other kinds of biopotential signals for medical diagnosis or for activity monitoring that can be sensed through electrodes attached to the skin, such as the electroencephalography (EEG), the electromyogram (EMG), the electrocardiogram (ECG), and the electrooculography (EOG). Depending on their physiological nature, different biopotential signals have distinct amplitude and frequency characteristics. The distribution of these commonly recorded biopotential signals span more than four decades both in amplitude, from 1 μV to 10 mV, and in frequency, from 1 Hz to 10 kHz [12], [18]. It is more economical to develop a programmable or reconfigurable sensing interface rather than to customize the design for each individual application. Moreover, under the area and power constraints, programmability and reconfigurability in general are beneficial in dealing with the process variation and mismatch issues in analog integrated circuits. Therefore, programmable sensing interface circuits have recently been adopted in many biomedical recording systems [4], [6], [13], [18]–[20].

Because of the ability to be programmed in continuum, floating-gate transistors have been exploited to make up universal sensor interface [21], and to perform versatile computation in large scale reconfigurable analog systems with superb area and power efficiency [22]–[24]. Nowadays, floating-gate based reconfigurable analog arrays have been used to model and to implement a variety of nonlinear neural dynamics [25], [26] with great complexity and flexibility. These highly power-efficient computation analog arrays can be located after the sensing frontend and can perform diverse signal processing to reduce the required information bandwidth for transmission. A floating-gate based biopotential sensing amplifier can be easily integrated into such reconfigurable platforms to facilitate the development of extremely power-efficient systems that can interface with living beings, as shown in Fig. 1.

In this paper, we present a floating-gate based reconfigurable biopotential sensing amplifier that meets the stringent requirements in neural recording applications, such as the rejection to offset drifting, large dynamic range, high linearity, high CMRR and PSRR, and low NEF. The amplifier uses complimentary differential pairs and the current reuse strategy to double the amplifier transconductance under the same current consumption. A fully differential topology is employed to ensure high CMRR and PSRR. The circuit bandwidth as well as the power consumption can be fully programmed in continuum by using floating-gate transistors. The common mode feedback is realized by a single floating-gate transistor without consuming any extra power. The measured NEF of 1.96 is among the lowest numbers that have been reported.

This paper is organized as follows. A literature survey on existing biopotential and neural sensing amplifiers is summarized in Section II. The design principles of the proposed amplifier and a brief introduction to floating-gate transistors, including long-term reliability information, are presented in Section III. The design tradeoff and comparison, detailed analysis on output swing range, input common-mode range, noise, and NEF are also derived in Section III. Both benchtop and biological measurement results are shown in Section IV. Finally, the conclusion along with the comparison table is drawn in Section V.

II. Biopotential Amplifiers

Instrumentation amplifiers have been broadly used in biopotential recording applications because of the high input impedance and the easy gain and offset adjustments through resistors [17]. However, the power consumption and the input-referred noise in this traditional approach are too high for implant applications. The capacitive feedback amplifier proposed in [7] can be integrated with microelectrode arrays achieving input-referred noise less than 3 $\mu\mathrm{V_{rms}}$ with low power consumption. The theoretical limit for the NEF with that employed operational transconductance amplifier (OTA) is about 2.9. The proposed MOS-BJT pseudo-resistors, which occupy small area but render resistance larger than 10^{12} Ω, provide the DC path and set the low-frequency cutoff corner down to tens of milli-Hz range in a 1.5 μm CMOS process. This capacitive feedback approach that uses capacitors to set the gain and to reject the DC offset has become the most popular topology in neural sensing applications.

The pseudo-resistors proposed in [7] cause nonlinearity. Besides, the resistance value as well as the low-frequency cutoff corner is set by the process and cannot be tuned. To program the low-frequency cutoff corner, digital-to-analog converters are applied at the gates of two back-to-back connected transistors [18] with the cost of extra current consumption. There is also a tradeoff between area and number of available options.

The limit for the NEF of the OTA used in the capacitive feedback amplifier has been improved by using current scaling and source degeneration techniques in a folded cascode topology [8]. Currents that do not contribute to amplifier transconductance are severely scaled down to save power. Source degeneration resistors are placed to reduce noise from transistors in current source branches. Current splitting technique further improves the NEF by increasing the effective transconductance [2]. The theoretical limit for NEF is reduced to 2.02 and the measured input-referred noise in both [2], [8] is around 3.06 $\mu\mathrm{V_{rms}}$. A partial operational transconductance amplifier sharing architecture is proposed in [10] to reduce the area and the NEF when multiple OTAs are integrated in an electrode array.

Complementary differential pairs are adopted in fully differential topologies to further improve both the common-mode rejection and the NEF [9], [11], [12], [20]. Self-biased schemes are applied to the OTAs in [9], [11] to save the extra power consumption and silicon area for common-mode feedback (CMFB). However, the output common-mode voltage is sensitive to the current level. Therefore, the current cannot be adjusted even when the required bandwidth is reduced. One of the amplifiers proposed in [12] employs a two-stage topology with CMFB circuit and achieves NEF of 2.9, which is still close to the numbers obtained from previous designs. Another complementary inverter with open-loop configuration proposed in [12] achieves NEF of 1.9. However, this amplifier cannot be practically used in biopotential sensing applications because of the poor supply rejection and high sensitivity to process variation.

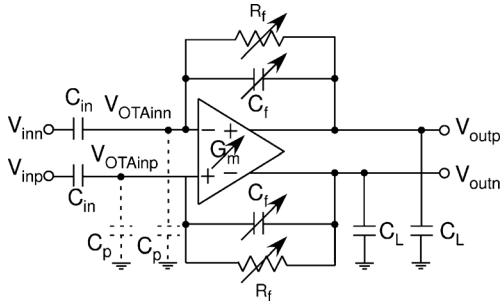

Fig. 2. A fully differential capacitive feedback topology is adopted for the proposed reconfigurable biopotential amplifier.

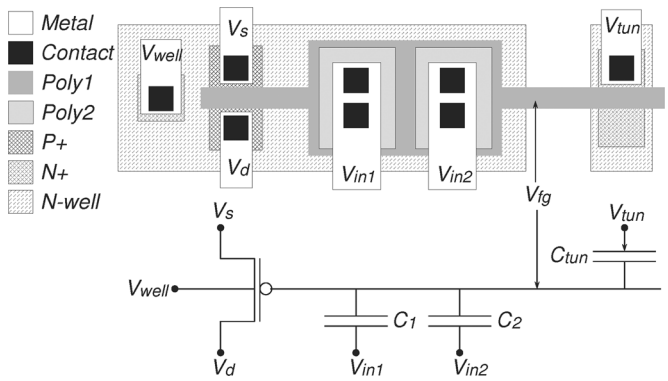

Fig. 3. The circuit schematic and layout of a pMOS floating-gate transistor with two input capacitances.

Besides the capacitive feedback amplifier approach, chopper techniques have been used to reduce the flicker noise and offset with the cost of reduced input impedance, increment of required amplifier bandwidth, and the extra dynamic power for driving switches. The modulated instrumentation amplifiers can achieve the input-referred noise less than 1 $\mu\mathrm{V_{rms}}$ with the NEF around 4.6 [1], [13], [14], [27].

In this paper, we present a floating-gate based reconfigurable biopotential sensing amplifier. The amplifier bandwidth range can be programmed in continuum. If the flicker noise is negligible, the theoretical limit for the NEF in our proposed design is below 1.45.

III. Reconfigurable Low-Noise Amplifier Design

Although instrumentation amplifiers with chopping techniques can achieve the input-referred noise below 1 $\mu\mathrm{V_{rms}}$, the power consumption is relatively high. An analog frontend with the input-referred noise of 3 $\mu\mathrm{V_{rms}}$ is usually sufficient for most biopotential recording applications. Therefore, the capacitive feedback topology is adopted in our design because of its low circuit complexity and high power efficiency. Considering the advantages of common-mode noise suppression, dynamic range, CMRR, PSRR, and NEF, our proposed sensing amplifier uses a fully differential architecture and the block diagram is shown in Fig. 2.

Assuming that the OTA is a first-order system and that the gain is much larger than the feedback ratio, i.e., $\mathrm{G_mR_o} \gg \mathrm{C_{in}} + \mathrm{C_f} + \mathrm{C_p}/\mathrm{C_f}$, the capacitive feedback amplifier has two poles located at $1/R_\mathrm{f}C_\mathrm{f}$ and $\mathrm{G_m}/\mathrm{C_{eff}}$, where $\mathrm{G_m}$ is the OTA transconductance, R_o is the OTA output impedance, C_p is the parasitic capacitance at the high impedance nodes, $C_\mathrm{eff} = C_\mathrm{o}C_\mathrm{T} - {C_\mathrm{f}}^2/C_\mathrm{f}, C_\mathrm{T} = C_\mathrm{in} + C_\mathrm{f} + C_\mathrm{p}$, and $C_\mathrm{o} = C_\mathrm{L} + C_\mathrm{f}$. There is a zero located at $\mathrm{G_m}/C_\mathrm{f}$ that is usually far away from the frequency range of interest. The midband gain is set by the capacitance ratio, $C_\mathrm{in}/C_\mathrm{f}$, and can be changed by switching different amount of feedback capacitance into the circuit. The low-frequency and the high-frequency cutoff corners can be adjusted independently by programming the values of R_f and $\mathrm{G_m}$, respectively.

In our proposed reconfigurable amplifier, floating-gate transistors are used for bias generation, common-mode feedback, and programmable feedback resistances. A brief introduction to floating-gate transistors and the relevant reliability information will be presented in the beginning of this section. Then we will shed light on the fact that the floating-gate approach not only facilitates the reconfigurability efficiently but also improves the theoretical NEF limit below 1.5. The power consumption of our proposed topology is also lower than that in the traditional approach.

A. Floating-Gate Transistor and Reliability

A floating-gate transistor is a normal transistor with the gate surrounded by high-quality silicon-oxide. Under normal operating conditions, the charge stored on the floating gate cannot escape. As such, floating-gate transistors have been used as nonvolatile memories for decades. One or multiple external voltages can be capacitively coupled into the floating gate. The layout and the circuit schematic of a pMOS floating-gate transistor with two input capacitances are shown in Fig. 3. If the parasitic and the tunneling capacitances are negligible, the floating-gate voltage can be expressed as

$$V_\mathrm{fg} = \frac{C_1 V_\mathrm{in1} + C_2 V_\mathrm{in2} + Q}{C_1 + C_2} \tag{1}$$

where Q is the charge on the floating-gate, which can be programmed precisely using hot-electron injection (CEI) and Fowler-Nordheim (FN) tunneling [21]. The same mechanisms are adopted in program/erase operations in digital flash memories [28].

The hot carrier reliability evaluation and degradation models of floating-gate devices after long-term program/erase cycles have been broadly studied through experimental techniques [28]–[33]. The detrimental effects are mainly attributed to two fundamental mechanisms: 1) charging of oxide traps and 2) generation of new oxide interface traps [29]. The distributions of oxide trap charge and the interface state concentrate on regions under high electrical stress, such as the region close to the drain when devices are under hot-electron stress and the region close to the source when the devices are under source-side FN erase-bias stress [30]. To avoid the oxide degradation causing adverse effects on amplifier performance, such as noise and bandwidth degradation, the indirect programming scheme [34] is adopted in our amplifier realization. The floating-gate transistors used in the operation mode do not experience high electrical stress, and are therefore not affected by increased oxide charges and interface states.

A floating-gate retention model in a 0.5 μm digital CMOS process is presented in [32]. For a floating-gate transistor with a capacitance of 100 fF, the voltage drift over 10 years at 55°C is extrapolated to be 0.5 μV. Thorough reliability testing results and retention models of pMOS EEPROM with 70Å tunneling oxide manufactured in generic logic CMOS processes have been presented in [31]. Assuming an end of life criterion of 70% loss in transistor current, a charge storage life time well exceeding 100 years at 125°C was extracted from the measurement results and reported in [31]. A 400μV voltage drift over a period of 10 years at 25°C is reported in a floating-gate voltage reference that is fabricated in a 0.35 μm CMOS process [33]. From these experimental results and the conclusions drawn from literature, the floating-gate charge retention time in a 0.35 μm logic CMOS process with a 70Å thick oxide is sufficiently long for biomedical applications.

Although the long-term oxide degradation due to CEI and FN tunneling reduces the programming efficiency as well as the retention time, these unfavorable effects on analog floating-gate circuits are less significant than those on digital flash memories. Digital memory cells must perform reliably for more than tens of thousands of open-loop programming/erase cycles. In modern flash memory cells, the floating-gate capacitance is approximately 1 fF. By contrast, the floating-gate capacitance in analog circuits can easily be larger than 100 fF or even larger than 1 pF. Charge perturbation stemming from finite retention time only causes unobservable voltage drift in such analog circuits. Moreover, the floating-gate analog circuits are usually designed to be programmed for just dozens or hundreds of times in a closed-loop fashion. The overall device stress period is significantly shorter than that in digital memories. Therefore, the charge perturbation effect is less apparent in analog floating-gate circuits. If the high voltage used for floating-gate programming is generated internally using on-chip charge pumps, the floating-gate transistors are not connected to the chip pads directly. All of the electrostatic discharge (ESD) events and supply glitches are handled by ESD protection circuits located close to the pads. Thus the floating-gate transistors as well as other circuits on the chip will not be damaged by environmental disturbances.

B. Floating-Gate Operational Transconductance Amplifier

To improve the amplifier power efficiency, the amount of current flowing through transistors that do not contribute to transconductance, for example transistors in current mirrors, should be minimized. These transistors generate noise and may consume extra current resulting in a high value of NEF. However current mirrors are inevitable if the differential input signals are to be converted to a single-ended output. To minimize the NEF, the topology of the OTA should be fully differential including no current mirrors. To further push the NEF below the theoretical limit reported in [8], complementary differential pairs along with the current reuse technique are exploited to double the transconductance under the same current consumption. The resultant NEF can, therefore, improve by a factor of $\sqrt{2}$.

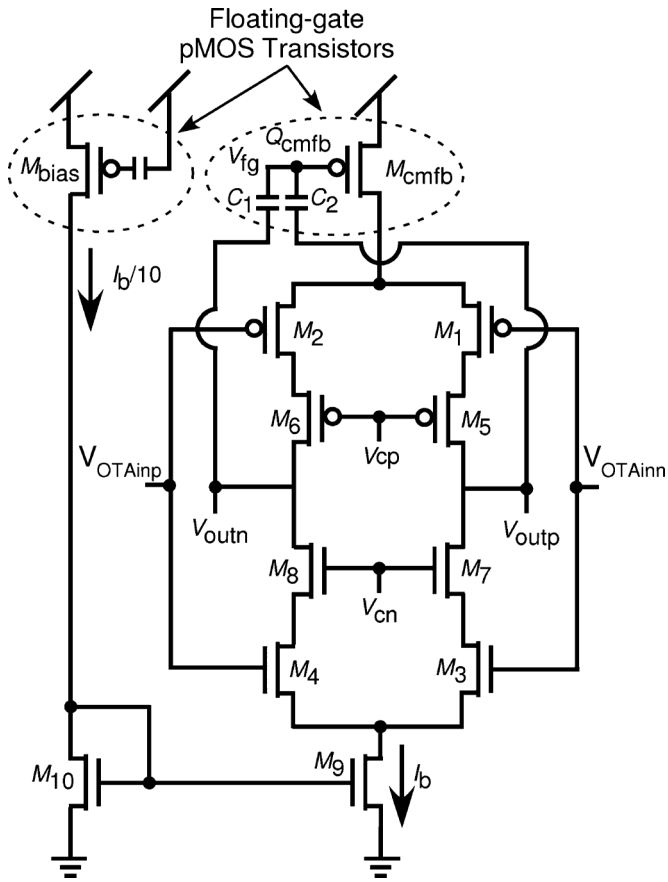

Fig. 4. The schematic of proposed floating-gate OTA employed in the reconfigurable biopotential amplifier. Switches used for floating-gate programming are not shown for simplicity.

The schematic of our proposed OTA is illustrated in Fig. 4, where switches and transistors used for floating-gate programming are not shown for simplicity. Complementary differential pairs are composed of M_{1-4}. The amount of $\mathrm{G_m}$, as well as the bandwidth, is set by the tail current, I_{b}, which comes from a pMOS floating-gate transistor, M_{bias}. This current can be programmed precisely. Cascode transistors, M_{5-8}, are employed to increase OTA gain with negligible noise contribution. The cascode bias voltages can be generated from a central bias generator block, which contains programmable floating-gate current sources and diode-connected transistors. The generated bias voltages then can be distributed across a large sensing amplifier array to minimize the extra power consumption per amplifier cell. Alternatively, the bias voltages can be generated locally by making cascode transistors floating-gate transistors. The floating-gate voltages can be programmed to the desired levels without consuming any extra power.

A pMOS floating-gate transistor, M_{cmfb}, is utilized for common-mode feedback. If the parasitic capacitance associated with the floating gate is negligible when compared with C_1 and C_2, the charge, Q_{cmfb}, on the floating-gate of M_{cmfb} can be programmed to adjust V_{fg} as shown in (1). If two input coupling capacitors, C_1 and C_2, are equally sized and matched, the output common-mode voltage can be extracted without introducing any noise and without consuming extra power.

When all transistors are biased in the saturation region, the common-mode feedback loop adjusts $V_{\rm fg}$ to some fixed level so that the current flowing through $M_{\rm cmfb}$ is equal to $I_{\rm b}$, which is constant. Depending on the amount of invariant floating-gate charge, $Q_{\rm cmfb}$, the output common-mode voltage remains at a constant level as desired.

The common-mode feedback capacitors, C_1 and C_2, are fractions of the load capacitance, which is usually large to achieve low input-referred noise. Hence these two capacitors can be sized large enough to guarantee matching without decreasing the circuit bandwidth. The incremental transconduction gain from the floating-gate charge, $Q_{\rm cmfb}$, to the output common-mode voltage, $V_{\rm out,cm}$, can be derived as

$$\frac{\Delta V_{\rm out,cm}}{\Delta Q_{\rm cmfb}} = \frac{1}{C_1 + C_2}. \tag{2}$$

This is equivalent to adjusting the voltage across a capacitor of size equal to $C_1 + C_2$ by programming the charge on it. It has been shown that the voltage can be programmed from rail to rail with 13-bit resolution with a 100 fF capacitor [35]. Therefore, for any current level of $I_{\rm b}$, the output common-mode voltage of the proposed OTA can be easily adjusted to the middle of supply rails. From (2), any charge disturbance from unknown environmental events, although unlikely, that cause tens-of-millivolt change on the floating gates will not break the circuit entirely but will only cause the output common-mode voltage to drift by tens of millivolts because of the negative feedback in the circuit.

Compared with traditional common-mode feedback approaches, the proposed floating-gate CMFB topology is simpler, occupies less silicon area, and consumes no extra power. Unlike self-biasing common-mode feedback schemes, this floating-gate approach can be applied to any current levels.

C. Reconfigurable Feedback Pseudo-Resistor

In some applications, it is preferable to suppress low-frequency interference without using additional filters to save power and area. Therefore, floating-gate based reconfigurable pseudo-resistors are adopted in our proposed amplifier to adjust the low-frequency cutoff corner in a very broad and continuous range. The equivalent circuit and the schematic are shown in Fig. 5. Two pMOS floating-gate transistors, M_1 and M_2, are connected in series with programming switches, M_{1s} and M_{2s}, which disconnect M_1 and M_2 from the circuit in the programming mode. MOS capacitors, $M_{1\rm tun}$ and $M_{2\rm tun}$, serve as tunneling junctions for Fowler-Nordheim tunneling. Hot carrier injection for charge trimming is performed on two injection transistors, $M_{1\rm p}$ and $M_{2\rm p}$, which share floating gates with M_1 and M_2 respectively. Switch transistors, M_{3-6}, connect the control gate voltages to $V_{\rm g\_prog}$ in the programming mode and to $V_{\rm DD}$ in the operation mode. The reset transistor, $M_{\rm rst}$, is for fast DC settling during the circuit start-up phase. Since the floating-gate voltage can be programmed in continuum, and the voltage can be programmed higher than $V_{\rm DD}$ and lower than ground, the resultant low-frequency cutoff corner of the sensing amplifier can be tuned in a very wide range without consuming any extra power.

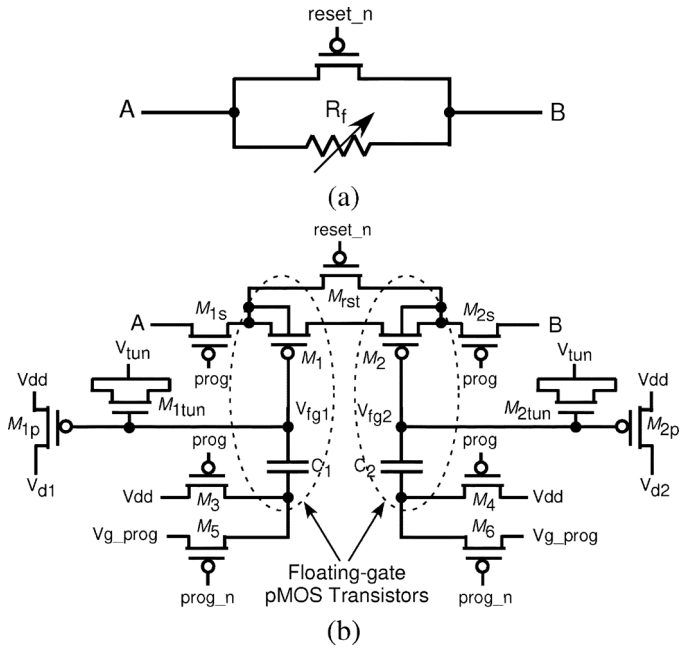

Fig. 5. Reconfigurable pseudo-resistor. (a) The equivalent circuit of the reconfigurable pseudo-resistor. A reset switch is for fast settling. (b) The schematic of the reconfigurable pseudo-resistor. Indirect programming technique is employed to reconfigure the resistance.

D. Input and Output Voltage Swing Analysis

Cascoding nMOS and pMOS differential pairs on top of each other reduces the output and input common-mode swing ranges. To simplify the analysis, the pMOS and nMOS transistors in the OTA are assumed to be designed and to be biased in a symmetric fashion (i.e., in Fig. 4, $V_{\rm SD,cmfb} = V_{\rm DS,9}$, $V_{\rm SD,2} = V_{\rm DS,4}$, $V_{\rm SD,6} = V_{\rm DS,8}$, $V_{\rm SG,2} = V_{\rm GS,4}$, and $V_{\rm SG,6} = V_{\rm GS,8}$). Under this symmetry assumption, the output and input common-mode ranges can be analyzed by just looking at transistors $M_{8,4,9}$ in Fig. 4. Because of the high voltage gain, the voltage swing at the OTA input nodes, $V_{\rm OTAinp}$ and $V_{\rm OTAinn}$, is tiny and $V_{\rm OTAinp} \approx V_{\rm OTAinn} \approx V_{\rm DD}/2$. To keep all transistors biased in the saturation region, it is required to have

$$V_{\rm GS,4} < \frac{V_{\rm DD}}{2} - V_{\rm DSsat} \tag{3}$$

$$V_{\rm cn} > \frac{V_{\rm DD}}{2} + V_{\rm GS,8} - V_{\rm GS,4} + V_{\rm DSsat} \tag{4}$$

$$\frac{V_{\rm DD}}{2} - \frac{V_{\rm swing}}{2} > V_{\rm cn} - V_{\rm GS,8} + V_{\rm DSsat}. \tag{5}$$

If all transistors are biased in the subthreshold region, $V_{\rm DSsat} \approx 5U_{\rm T} \approx 125$ mV, where $U_{\rm T}$ is the thermal voltage. The input differential pairs can be sized in such a way that

$$V_{\rm GS,4} = \frac{V_{\rm DD}}{2} - V_{\rm DSsat} - \Delta V_9 \tag{6}$$

and the cascode voltage can be biased as

$$V_{\rm cn} = \frac{V_{\rm DD}}{2} + V_{\rm GS,8} - V_{\rm GS,4} + V_{\rm DSsat} + \Delta V_4 \tag{7}$$

where $\Delta V_{4(9)}$ is the positive marginal voltages to keep $M_{4(9)}$ above V_{DSsat}(i.e., $\Delta V_{4(9)} = V_{\mathrm{DS},4(9)} - V_{\mathrm{DSsat}} > 0$). The output voltage swing range can be derived as

$$V_{\mathrm{swing}} = V_{\mathrm{DD}} - 6V_{\mathrm{DSsat}} - 2(\Delta V_4 + \Delta V_9) \tag{8}$$

under the assumption that pMOS and nMOS transistors are symmetrically biased.

To analyze the input common-mode swing range, the saturation constraints can be written as

$$V_{\mathrm{OTAinp}} - V_{\mathrm{GS},4} > V_{\mathrm{DSsat}} \tag{9}$$

$$V_{\mathrm{cn}} - V_{\mathrm{GS},8} - (V_{\mathrm{OTAinp}} - V_{\mathrm{GS},4}) > V_{\mathrm{DSsat}}. \tag{10}$$

If $V_{\mathrm{GS},4}$ and V_{cn} are designed as (6) and (7), the input swing range of the OTA can be derived as

$$\frac{V_{\mathrm{DD}}}{2} - \Delta V_9 \le V_{\mathrm{OTAinp}} \le \frac{V_{\mathrm{DD}}}{2} + \Delta V_4. \tag{11}$$

Therefore, under the symmetrical biasing conditions, the input common-mode swing range depends on the marginal voltages of ΔV_4 and ΔV_9 designed in (6) and (7). If the pMOS and nMOS transistors are not biased in the symmetric manner, the input common-mode voltage swing range will reduce to

$$V_{\mathrm{OTAinp}} \ge \frac{V_{\mathrm{DD}}}{2} - \min(\Delta V_9, \Delta V_2) \tag{12}$$

$$V_{\mathrm{OTAinp}} \le \frac{V_{\mathrm{DD}}}{2} + \min(\Delta V_4, \Delta V_{cmfb}). \tag{13}$$

In this case, the minimum supply voltage for the proposed OTA can be expressed as

$$V_{\mathrm{DD,min}} = V_{\mathrm{swing}} + 6V_{\mathrm{DSsat}} + \Delta V_4 + \Delta V_9 + \Delta V_2 + \Delta V_{cmfb}. \tag{14}$$

It is obvious from (14) that the supply voltage should accommodate six saturation voltages as well as the required output and input common-mode signal swing ranges.

E. Noise Analysis

If all transistors in the OTA are properly biased in the saturation region, the noise contribution from cascode transistors, M_{5-8}, is attenuated by a factor of $1/(1 + g_s r_o)$, where g_s is the incremental source transconductance and r_o is the output resistance of a transistor. Hence it is negligible compared to the noise from transistors in the differential pairs. Besides, the tail current transistor, M_9, as well as the common-mode feedback transistor, M_{cmfb}, does not contribute to differential noise. Therefore, the output-referred current noise of the proposed floating-gate OTA can be simply expressed as

$$\tilde{i}_o^2 = 4 \cdot 4kT\gamma g_m \quad (A^2/\mathrm{Hz}) \tag{15}$$

where k is Boltzmanns constant, T is the absolute temperature, g_m is the transconductance of the transistor, and $\gamma = 2/3$ for strong-inversion operation, $\gamma = 1/(2\kappa)$ for subthreshold operation, and κ is the subthreshold slope coefficient of a MOSFET transistor. Since the differential pair transistors should be sized large enough to suppress the flicker noise, they usually operate in the subthreshold region, where $g_m = \kappa I_b/(2U_T)$.

The noise analysis of a capacitive feedback amplifier has been detailed in [36]. The total output-referred voltage noise is independent of the current consumption and is given as

$$\hat{V}_{\mathrm{no,rms}}^2 = \frac{qU_T}{\kappa} \cdot \frac{C_T}{C_f C_o}. \tag{16}$$

Since the gain of the amplifier is C_{in}/C_f, the input-referred voltage noise can be expressed as

$$\hat{V}_{\mathrm{ni,rms}} = \sqrt{\frac{qU_T}{\kappa} \cdot \frac{C_T C_f}{{C_{in}}^2 C_o}}. \tag{17}$$

The noise efficiency factor (NEF) [17] is commonly used to evaluate the efficiency in the noise-power tradeoff. It is defined as

$$\mathrm{NEF} = \hat{V}_{\mathrm{ni,rms}} \sqrt{\frac{2I_{\mathrm{total}}}{\pi \cdot U_T \cdot 4kT \cdot \mathrm{BW}}} \tag{18}$$

where BW is the high-frequency cutoff corner in Hz.

The theoretical NEF for a single BJT amplifier with a perfect load and without 1/f noise is 1 by definition. For a single MOS common-source amplifier biased in the subthreshold region, since the g_m, as well as BW, is proportional to $\kappa I_{\mathrm{total}}$, the theoretical NEF becomes $1/\kappa$ under the same assumptions of perfect loading and 1/f noise exclusion.

With the same bias current, if the amplifier employs complementary MOS transistors to double the g_m, and hence the bandwidth, the theoretical NEF can be improved by $\sqrt{2}$. However, the CMRR and the PSRR of such amplifier is usually low and unworkable in biomedical sensing applications [12]. Differential pairs are necessary to be adopted in the amplifier architecture to achieve practical CMRR and PSRR, with the cost of halving the transconductance efficiency, which results in NEF degradation by a factor of $\sqrt{2}$. Therefore, under the same assumptions of perfect loading and 1/f noise exclusion, the theoretical NEF for an amplifier using complementary differential pairs in a push-pull topology is $1/\kappa$, which is in line with the theoretical NEF of our proposed reconfigurable sensing amplifier. The detail analysis is given briefly as follows.

Assuming that the differential pair transistors are biased in the subthreshold region, the bandwidth can be expressed as

$$\mathrm{BW} = \frac{G_m}{2\pi C_{\mathrm{eff}}} \approx \frac{\kappa I_b}{2\pi U_T} \cdot \frac{C_f}{C_T C_o}. \tag{19}$$

From (18) and (19), if the bias current through $M_{\rm bias}$ in Fig. 4 is negligible, the NEF of the proposed sensing amplifier is

$$\mathrm{NEF} = \frac{C_{\rm T}}{\kappa C_{\rm in}} \approx \frac{1}{\kappa} \approx 1.43. \tag{20}$$

In (20), it is assumed a typical value of $\kappa = 0.7$ with negligible $C_{\rm p}$ and $C_{\rm f}$ when compared with $C_{\rm in}$. This expression is equivalent to the NEF value of a single MOSFET transistor operating in the subthreshold region.

Compared with the theoretical limit for the NEF in a folded-cascode OTA using the current scaling technique in [8]

$$\mathrm{NEF}_{\rm fc} = \frac{\sqrt{2}}{\kappa} \approx 2.02 \tag{21}$$

the limit of our proposed topology is improved by a factor of $\sqrt{2}$. The theoretical limit of the partial OTA sharing architecture proposed in [10] is

$$\mathrm{NEF}_{\rm ps} = \frac{\sqrt{2}}{\kappa}\sqrt{\frac{n+1}{2n}} \tag{22}$$

where n is the array size. This limit approaches to (20) when the number of the sharing amplifiers approaches infinity.

F. Design Tradeoff and Comparison

There is a fundamental tradeoff between noise, swing ranges, supply voltage, and power consumption. In our proposed OTA, from the aforementioned analysis, the supply voltage is raised up to minimize the value of NEF and to accommodate the output and input common-mode swing ranges. Although the value of NEF is minimized, it does not completely represent the total power efficiency because the term of supply voltage is absent in the NEF definition. Therefore, meticulous attention should be paid when the power consumption is compared with traditional approaches.

Under the assumption that transistors are biased in the subthreshold region, if only one, say nMOS, differential pair is adopted in the OTA, the bias current needs to be doubled to achieve the same $\mathrm{G_m}$. Without consuming extra current, cascode transistors cannot be spared to obtain the gain of the same order of $(g_{\rm m}r_{\rm o})^2$. Therefore, there will be a pair of cascoded pMOS current sources on top of the cascoded nMOS differential pair as the active load. It can be shown that the minimum supply voltage is

$$\begin{aligned} V_{\rm DD,min,trad} &= V_{\rm swing} + 5V_{\rm DSsat} + \Delta V_4 + \Delta V_9 \\ &\approx \frac{V_{\rm DD,min}}{2} + \frac{V_{\rm swing}}{2} + 2V_{\rm DSsat}. \end{aligned} \tag{23}$$

If a folded-cascode topology is employed as in [2], [8], the minimum supply voltage can be reduced to

$$\begin{aligned} V_{\rm DD,min,folded} &= V_{\rm swing} + 4V_{\rm DSsat} \\ &\approx \frac{V_{\rm DD,min}}{2} + \frac{V_{\rm swing}}{2} + V_{\rm DSsat} - \frac{\Delta V_{\rm in,cm}}{2} \end{aligned} \tag{24}$$

where $\Delta V_{\rm in,cm}$ is the input common-mode swing range. With typical values of $V_{\rm DSsat} = 125$ mV and $\mathrm{V_{swing}} = 400$ mV, only when $\Delta V_{\rm in,cm} \geq 650$ mV, the minimum supply voltage can be lower than the half of that in our proposed approach. However, because of the dramatic current scaling at the output biasing branches, the differential pair transistors are also cascoded and the current sources are implemented by source degenerated transistors in [2], [8]. Therefore, another term of *IR* drop will be added in (24). Usually the degeneration resistance should be large enough to minimize the noise contribution and the resulting supply voltage is even higher than the expression of (23). Since the required supply voltages in these cases are more than half of $V_{\rm DD,min}$ expressed in (14), our proposed amplifier consumes less power than the traditional approaches. Moreover, in our proposed topology, there are no active load transistors, which only contribute to noise without enhancing $\mathrm{G_m}$. Thus the input referred noise is lower than the traditional approach. In summary, with the cost of higher supply voltage, our proposed amplifier achieves lower noise, less power consumption, better reconfigurability, and simpler topology compared with the traditional approaches.

IV. Measurement Results

A concept proving prototype of the reconfigurable biopotential sensing amplifier was fabricated in a 0.35 μm CMOS process with two-poly-four-metal(2P4M) layers. The chip contains two versions of amplifiers. Both amplifiers are designed to have the maximum midband gain of 110 (or 40.8 dB) with the input capacitance of 22 pF. One version of the amplifier has fixed feedback capacitors of 200 fF. The other version includes feedback capacitor arrays with 5-bit control signals to adjust the gain. In each amplifier, six pMOS floating-gate transistors are used to set the bias current, the common-mode output voltage, and the feedback resistance. Without optimizing the layout area, each amplifier occupies a 0.17 mm^2. Two buffers following each amplifier are designed to drive testing instruments. The photograph of this prototype chip is shown in Fig. 6. In this prototype chip, the cascode biasing voltages, $V_{\rm cp}$ and $V_{\rm cn}$, are applied externally but they will be implemented by floating-gate transistors in the next version.

A. Test Bench Results

The major circuit characterization was performed on the amplifier with fixed feedback capacitors. The amplifier bandwidth was first configured to 10 kHz and the total current consumption, including the biasing branch, 4.3 μA. The measured maximum gain is 40.7 dB and is close to the designed value. The charge on the feedback floating-gate transistors can be programmed to set the low-frequency cutoff corner. In Fig. 7, we show the measured frequency responses when the low-frequency cutoff corner was configured from 5 mHz up to 200 Hz. The floating-gate programming approach does not pose limits on the range of the low-frequency cutoff corner. Actually the lower limit is set by the reverse biased junction current at the feedback transistor between its n-well and the p-substrate. If the feedback resistance is too large for the feedback current to compensate for the leakage current, the amplifier input nodes will be pulled down to ground gradually. In this chip, this limit is at about 10 mHz.

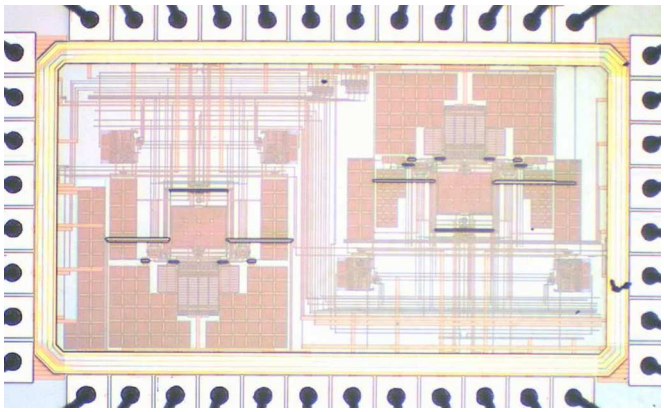

Fig. 6. The photograph of a prototype chip including two reconfigurable biopotential sensing amplifiers.

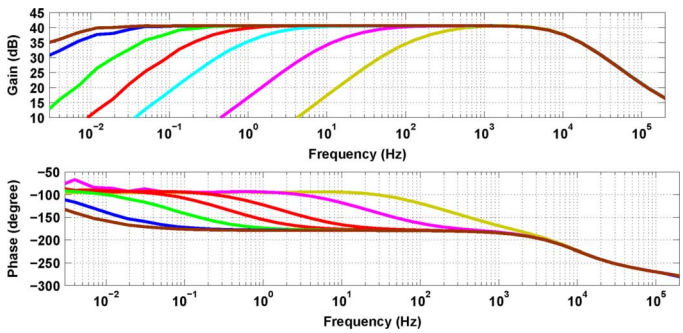

Fig. 7. Measured frequency responses of the amplifier of which low-frequency cutoff corner was configured several different values.

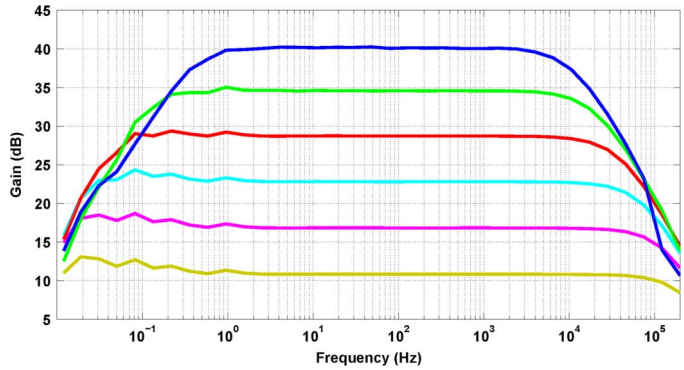

Fig. 8. Measured frequency responses of the programmable gain amplifier. The gain can be programmed from 40 dB down to 10 dB. The ripples at low frequencies are the measurement artifacts due to insufficient time constant setup in the lock-in amplifier.

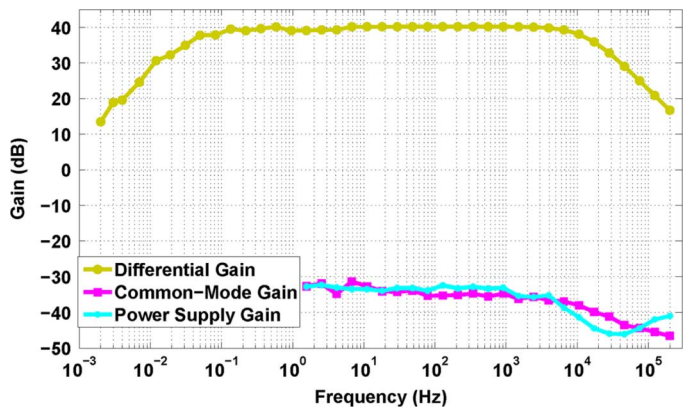

Fig. 9. Measured Common-mode and power supply rejection ratios. Both CMRR and PSRR exceed 70 dB over the range of 1 Hz to 10 kHz.

Without low-frequency interferences, the practical upper limit for the low-frequency cutoff corner should be determined by the noise contribution of the feedback resistance. When the resistance is too small, the thermal noise of the feedback transistors is no longer negligible and the noise performance degrades [16]. In the noise measurement, the low-frequency cutoff corner is kept below 1 Hz.

The gain of the second amplifier can be programmed by switching different amount of feedback capacitance from the binary capacitor arrays into the circuit. The measured frequency responses are shown in Fig. 8. The measured maximum gain is 40.3 dB, which is slightly lower than the designed value due to the increment of parasitic capacitance. The gain can be programmed from 40 dB down to 10 dB using 5-bit control signals.

Measured common-mode rejection and supply rejection responses are shown in Fig. 9. The CMRR and the PSRR are dependent on the matching between two branches. Several chips are measured and the CMRR and the PSRR exceed 70 dB over the range of 1 Hz to 10 kHz. At low frequencies, the rejection ratios are dominated by the mismatch between the low-frequency cutoff corners of two branches, which can be adjusted by trimming the charge on the feedback floating-gate transistors.

A 60 Hz common-mode waveform is combined with a 200 Hz 4 $\mathrm{mV_{pp}}$ differential signal feeding into the amplifier to test the input common-mode range. With the peak-to-peak amplitude of 565.7 mV, the measured differential gain is degraded by 1 dB because some transistor is no longer in the saturation region.

To characterize the noise performance, the amplifier bandwidth was programmed to several values: 10 kHz, 1 kHz, and 100 Hz. The total current consumptions in these three configurations are 4.3 μA, 348 nA, and 33 nA, respectively. The measured frequency responses are shown in Fig. 10. The noise spectrums are shown in Fig. 11. The total noise power are integrated from 50 mHz to 200 kHz and the measured input-referred noise voltages in these bandwidth settings are all 2.8 $\mu\mathrm{V_{rms}}$. In the case of 1 kHz bandwidth, the output noise waveform is divided by the gain to generate the input-referred noise waveform, which is shown in Fig. 12. Its standard deviation is 2.76 $\mu\mathrm{V_{rms}}$, which agrees with the value extracted from the noise spectrum. The measured noise efficiency factors in these three settings are 2.25, 2.01, and 1.96 respectively, which are among the lowest values published to date. The measured characteristics of the reconfigurable biopotential sensing amplifier are summarized in Table I. When the bandwidth is set to 10 kHz, the differential pairs operate closer to the threshold region. Therefore, the transconductance efficiency as well as the NEF degrades. The NEF can be improved in the next version by making the differential pair transistors larger.

The total harmonic distortion (THD) is dominated by the nonlinearity of the OTA at high frequencies and is dominated by that of the feedback floating-gate transistors at low frequencies. The THD measurement results when the bandwidth is configured to

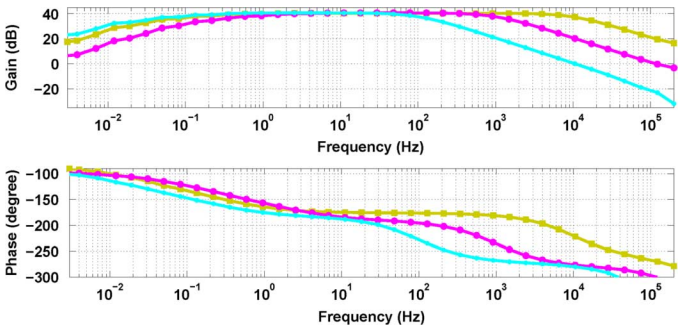

Fig. 10. The amplifier was configured to have the bandwidth of 10 kHz, 1 kHz, and 100 Hz.

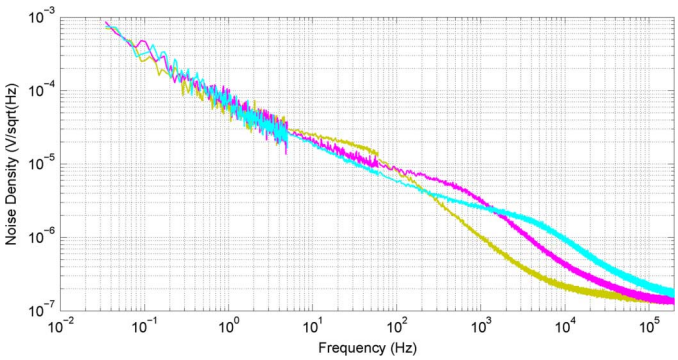

Fig. 11. Measured amplifier noise spectrums with the bandwidth being programmed to 10 kHz, 1 kHz, and 100 Hz, respectively.

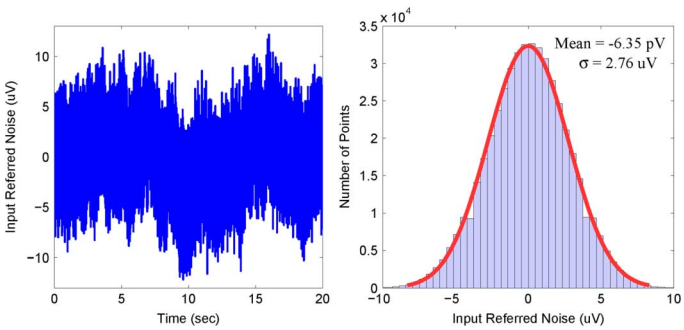

Fig. 12. Measured amplifier input-referred noise waveform and its histogram from the configuration with the bandwidth equal to 1 kHz. The standard deviation is 2.76 $\mu\mathrm{V_{rms}}$ which agrees with the noise spectrum measurement.

10 kHz are shown in Figs. 13 and 14. The output magnitude is adjusted to 300 $\mathrm{mV_{rms}}$ (or -10.4 dBV). The measured 3rd harmonic is 60 dB down with the primary frequency at 1 kHz. The THD is degraded to 40 dB when the primary frequency is set at 10 Hz. The dynamic range of the reconfigurable biopotential amplifier is 60 dB. The THD measurement results with bandwidths of 1 kHz and 100 Hz are also summarized in Table I.

B. Biological Measurement Results

We also verified our proposed reconfigurable biopotential sensing amplifier in a real recording environment and took several different kinds of electrophysiological signals from human bodies using commercial Ag/AgCl skin electrodes. The measured input-referred recorded waveforms are shown in Fig. 15. The amplifier bandwidth was first programmed to

TABLE I
MEASURED CHARACTERISTICS OF THE AMPLIFIER

Parameter	Measured Value
Supply Voltage	2.5 V
Max. Gain	40.74 dB
CMRR (1Hz – 10 kHz)	$>$ 70 dB
PSRR (1Hz – 10 kHz)	$>$ 70 dB
Input Common-mode Range (-1 dB Gain Degradation)	565.7 mV
Area (in 0.35 μm CMOS Process)	0.17mm^2
Bandwidth (0.1Hz – 10 kHz)	
Total Current	4.3 μA
Input Referred Noise (50 mHz – 200 kHz)	2.8 $\mu\mathrm{V_{rms}}$
NEF	2.25
THD @ 1 kHz with 300 $\mathrm{mV_{rms}}$ output	0.1%
THD @ 10Hz with 300 $\mathrm{mV_{rms}}$ output	1%
Dynamic Range (10Hz – 1 kHz)	60 dB
Bandwidth (0.5Hz – 1 kHz)	
Total Current	348 nA
Input Referred Noise (50 mHz – 200 kHz)	2.8 $\mu\mathrm{V_{rms}}$
NEF	2.01
THD @ 100Hz with 250 $\mathrm{mV_{rms}}$ output	1%
Dynamic Range (10Hz – 100Hz)	55.36 dB
Bandwidth (0.05Hz – 100Hz)	
Total Current	33 nA
Input Referred Noise (50 mHz – 200 kHz)	2.8 $\mu\mathrm{V_{rms}}$
NEF	1.96
THD @ 10Hz with 200 $\mathrm{mV_{rms}}$ output	1%
Dynamic Range (10Hz – 100Hz)	53.43 dB

10 kHz to record the flexed and relaxed muscle EMG signals from the right forearm. Since the ECG bandwidth is within 1 kHz, the amplifier bandwidth was reconfigured to 1 kHz to record the ECG. The recorded PQRST waves are clearly shown in the second plot in Fig. 15. To observe the EOG signals during the eye movement, the amplifier bandwidth was reconfigured to 100 Hz. The recorded waveform is shown in the third plot. Finally, we recorded the α-wave from the visual cortex during the periods of eyes closed and opened. The waveform variation before and after a wink is obviously shown in the forth plot in Fig. 15.

V. CONCLUSION

A fully reconfigurable biopotential sensing amplifier with measured input-referred noise of 2.8 $\mu\mathrm{V_{rms}}$ is presented in this paper. Thanks to the employment of the complementary differential pairs and the floating-gate common-mode feedback architecture, the proposed amplifier can achieve the best efficiency in the tradeoff between noise and power. The measured noise efficiency factor in the configuration of 100 Hz bandwidth is 1.96 consuming 82.5 nW of power. The NEF can be further reduced to 1.87 in the next version where the common-mode feedback will be performed on an nMOS floating-gate transistor to spare the current consumption in the biasing branch. The theoretical limit for the NEF of the proposed amplifier is $1/\kappa \approx 1.43$, which originates from the nature of the capacitive coupling of a MOSFET transistor. This number is equivalent to the NEF value of a single MOSFET transistor operating in the subthreshold region. The performance comparisons with recent

TABLE II
SUMMARY OF PERFORMANCE COMPARISON

Parameter	[7] 2003	[8] 2007	[10] 2011	[11] 2012	[12]BPA2 2012	[12]BPA3 2012	[13] 2012	[14] 2012	This work		
Technology (μm)	1.5	0.5	0.18	0.18	0.5	0.13	0.35	0.18	0.35		
Supply voltage (V)	$\pm$2.5	2.8	1.8	1	1	1	3.3	0.6	2.5		
Supply current (A)	16μ	2.7μ	4.4μ	0.8μ	0.8μ	12.1μ	22.4μ	1μ	4.3μ	348n	33n
Gain (dB)	39.5	40.9	39.4	40	36	40	46.7	40	40.7		
Bandwidth (kHz)	7.2	5.3	7.2	5.8	4.7	10.5	N/A	1.8	10	1	0.1
Low-frequency cutoff (Hz)	0.025	45	10	0.2	0.3	0.05	N/A	0.5	0.1	0.5	0.05
Input-referred noise (μV_{rms})	2.2	3.06	3.5	5.71	3.6	2.2	3.3	5.41	2.8		
Noise efficiency factor (NEF)	4.0	2.67	3.35	2.59	1.9	2.9	4.5	4.7	2.25	2.01	1.96
THD with	1%	1%	1%	N/A	7.1%	1%	0.1%	N/A	0.1%	1%	1%
Input voltage (mV)	16.7	7.3	5.7	N/A	1	1	20	N/A	3	2.5	2
Dynamic Range (dB) (@ 1%THD)	69	58	58.4	N/A	N/A	N/A	66.4	63	>60	55.36	53.43
CMRR (dB)	≥ 83	66	70.1	>60	N/A	80	>110	>120	>70		
PSRR (dB)	≥ 85	75	63.8	>70	5.5	≥ 80	>110	>120	>70		
Area (mm^2)	0.16	0.16	0.06	N/A	0.07	0.07	0.16	0.28	0.17		

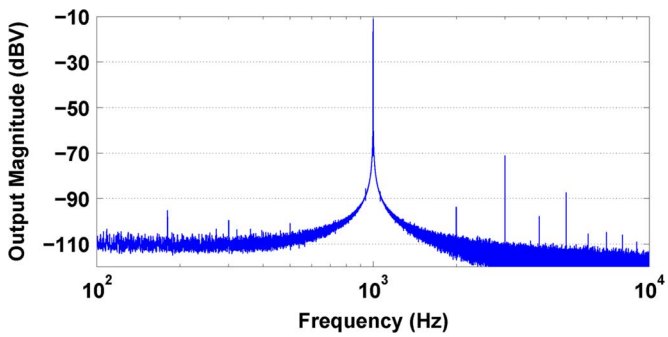

Fig. 13. Measured THD result with an 1 kHz, 3 mV_{rms} sinusoidal input signal. The 3rd harmonic is 60 dB below the main tone.

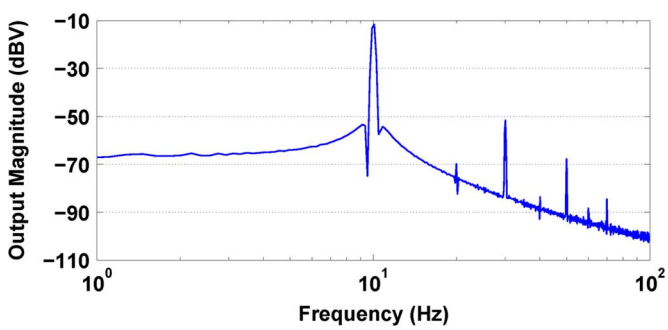

Fig. 14. Measured THD result with an 10 Hz, 3 mV_{rms} sinusoidal input signal. The 3rd harmonic is 40 dB below the main tone.

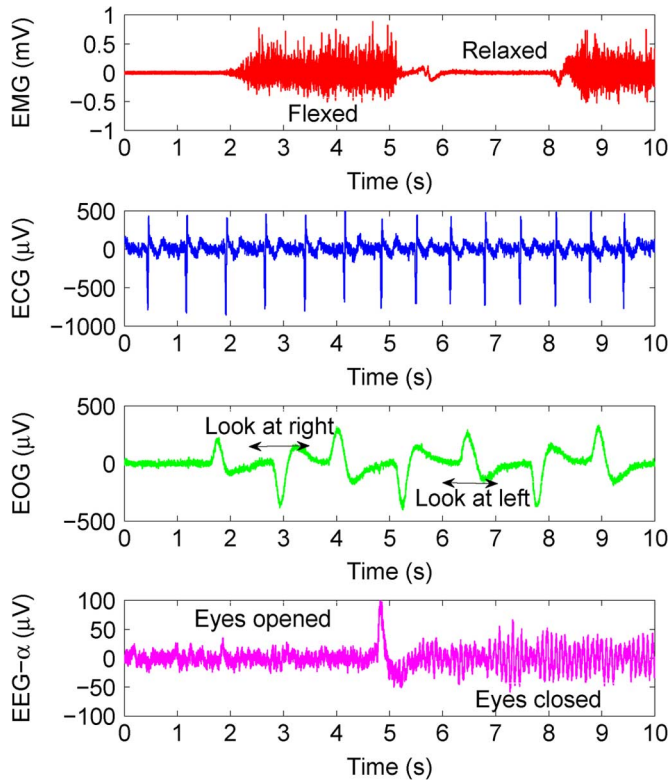

Fig. 15. Measured input-referred electrophysiological signals: Electromyography (EMG), electrocardiography (ECG), electrooculography (EOG), and electroencephalography (EEG) α wave. The amplifier bandwidths are configured to 10 kHz, 1 kHz, 100 Hz and 100 Hz respectively in these recordings.

prior works are listed in Table II. This work is the only one of which the high-frequency and the low-frequency corners can be programmed in continuum without using off-chip components. Besides the benchtop measurements, different kinds of electrophysiological signals was recorded using the proposed amplifier with several bandwidth configurations. In summary, the amplifier presented in this paper achieves excellent circuit performance as well as exceptional reconfigurability.

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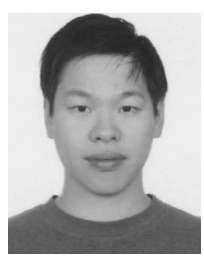

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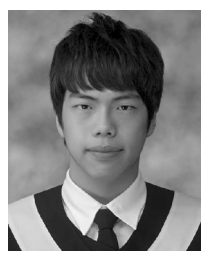

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