Group 20 VHDL Testing Document

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# Console Output

**WHEN** '0' => ch := ' ';

**WHEN** '1' => ch := 'B';

**WHEN** 'U' => ch := 'U';

**WHEN** **OTHERS** => ch := 'X';

# Test 1: Default Sample Commands

## Output

*#*

*#*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB BB BB B BB*

*# BB BBBBBBB*

*# BBBBBB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

*# BBBBBB*

*# BBBBBBB BB*

*# BB B BB BB BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B BB*

*# BB B B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*# B B B B B*

*#*

*# BBBBBBBBB*

*# B BBBBBBB B*

*# BB BBBBB BB*

*# BBB BBB BBB*

*# BBBB B BBBB*

*# BBBBBBBBBBB*

*# BBBB B BBBB*

*# BBB BBB BBB*

*# BB BBBBB BB*

*# B BBBBBBB B*

*# BBBBBBBBB*

*# \*\* Note: Commands from: Test1.txt, VDP PASSED.*

## Justifications for Test

This test was used as a method to test whether the main logic flow of our code was working or not. Since this test does not provide a wide range of input commands, this test was only used at the start of our verification process.

## Code Coverage

Test 1 has a basic hardware coverage. It only draws black lines, and clears a small block with the start point already in the bottom left. However, it does test xbias as the star has lines which don’t have an angle of 45 degrees.

### Overall

*Coverage Report Totals BY FILES: Number of Files 8*

*Total coverage (Code Coverage Only, filtered view): 70.9%*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *388* *321* *67* *82.7*

*Branches* *252* *183* *69* *72.6*

*UDP Condition Rows* *0* *0* *0* *100.0*

*FEC Condition Terms* *30* *15* *15* *50.0*

*UDP Expression Rows* *0* *0* *0* *100.0*

*FEC Expression Terms* *14* *10* *4* *71.4*

*States* *22* *20* *2* *90.9*

*Transitions* *60* *39* *21* *65.0*

### By File

*Coverage Report Summary Data by file*

*Total Coverage By File (code coverage only, filtered view): 74.0%*

*File: draw\_any\_octant.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *8* *8* *0* *100.0*

*Branches* *2* *2* *0* *100.0*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *2* *2* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *38* *34* *4* *89.4*

*File: draw\_octant.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *25* *25* *0* *100.0*

*Branches* *10* *10* *0* *100.0*

*FEC Condition Terms* *7* *6* *1* *85.7*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *162* *140* *22* *86.4*

*File: hdb.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *166* *133* *33* *80.1*

*Branches* *98* *64* *34* *65.3*

*FEC Condition Terms* *12* *2* *10* *16.6*

*FEC Expression Terms* *8* *7* *1* *87.5*

*States* *12* *10* *2* *83.3*

*Transitions* *32* *16* *16* *50.0*

*Toggle Bins* *366* *329* *37* *89.8*

*File: pix\_cache\_pak.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *12* *0* *12* *0.0*

*Branches* *10* *0* *10* *0.0*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *0* *0* *0* *100.0*

*File: pix\_word\_cache.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *36* *29* *7* *80.5*

*Branches* *29* *21* *8* *72.4*

*FEC Condition Terms* *2* *0* *2* *0.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *34* *33* *1* *97.0*

*File: pix\_write\_cache.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *33* *31* *2* *93.9*

*Branches* *16* *14* *2* *87.5*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *4* *4* *0* *100.0*

*Transitions* *8* *5* *3* *62.5*

*Toggle Bins* *124* *122* *2* *98.3*

*File: project\_pack.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *13* *7* *6* *53.8*

*Branches* *16* *11* *5* *68.7*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *0* *0* *0* *100.0*

*File: rcb.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *95* *88* *7* *92.6*

*Branches* *71* *61* *10* *85.9*

*FEC Condition Terms* *9* *7* *2* *77.7*

*FEC Expression Terms* *4* *1* *3* *25.0*

*States* *6* *6* *0* *100.0*

*Transitions* *20* *18* *2* *90.0*

*Toggle Bins* *316* *274* *42* *86.7*

*NEVER FAILED: 83.3%* *ASSERTIONS: 6*

# Test 2: Drawing Different Shapes

## Output

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB B*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB BB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB BBB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB BBBB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB BBBBB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB BBBBBB*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB BBBBBBB*

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*# B BB*

*#*

*# BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

*# BBBBBBBBBBBBBBBBBBBB B BBBBBBBBBBBBBBBBBBBBBBBB*

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*# \*\* Note: Commands from: Test2.txt, VDP PASSED.*

## Justifications for Test

This test builds on test 1, and draws/moves/clears lines/blocks in different octants. It also attempts to draw straight lines/blocks to test the octant truth table. Also tested are dots, filling up the whole screen with clear, and multi-block tests. Multicolour move/draw/clear is tested. Long lines using draw/clear are tested.

## Code Coverage

Test 2 should have a larger coverage than test 1. It tests clears in each direction, and hence executes the compare/swap function used to move the start point to the bottom left. It also tests moving with colours, as well as drawing lines in each octant using clear commands

### Overall

*Coverage Report Totals BY FILES: Number of Files 8*

*Total coverage (Code Coverage Only, filtered view): 85.9%*

*Enabled Coverage Active Hits Misses % Covered*

*---------------- ------ ---- ------ ---------*

*Stmts 388 350 38 90.2*

*Branches 252 216 36 85.7*

*UDP Condition Rows 0 0 0 100.0*

*FEC Condition Terms 30 29 1 96.6*

*UDP Expression Rows 0 0 0 100.0*

*FEC Expression Terms 14 10 4 71.4*

*States 22 22 0 100.0*

*Transitions 60 43 17 71.6*

### By File

Coverage Report Summary Data by file

Total Coverage By File (code coverage only, filtered view): 87.9%

File: draw\_any\_octant.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 8 8 0 100.0

Branches 2 2 0 100.0

FEC Condition Terms 0 0 0 100.0

FEC Expression Terms 2 2 0 100.0

States 0 0 0 100.0

Transitions 0 0 0 100.0

Toggle Bins 38 38 0 100.0

File: draw\_octant.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 25 25 0 100.0

Branches 10 10 0 100.0

FEC Condition Terms 7 6 1 85.7

FEC Expression Terms 0 0 0 100.0

States 0 0 0 100.0

Transitions 0 0 0 100.0

Toggle Bins 162 160 2 98.7

File: hdb.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 166 153 13 92.1

Branches 98 85 13 86.7

FEC Condition Terms 12 12 0 100.0

FEC Expression Terms 8 7 1 87.5

States 12 12 0 100.0

Transitions 32 20 12 62.5

Toggle Bins 366 365 1 99.7

File: pix\_cache\_pak.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 12 0 12 0.0

Branches 10 0 10 0.0

FEC Condition Terms 0 0 0 100.0

FEC Expression Terms 0 0 0 100.0

States 0 0 0 100.0

Transitions 0 0 0 100.0

Toggle Bins 0 0 0 100.0

File: pix\_word\_cache.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 36 31 5 86.1

Branches 29 23 6 79.3

FEC Condition Terms 2 2 0 100.0

FEC Expression Terms 0 0 0 100.0

States 0 0 0 100.0

Transitions 0 0 0 100.0

Toggle Bins 34 33 1 97.0

File: pix\_write\_cache.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 33 31 2 93.9

Branches 16 14 2 87.5

FEC Condition Terms 0 0 0 100.0

FEC Expression Terms 0 0 0 100.0

States 4 4 0 100.0

Transitions 8 5 3 62.5

Toggle Bins 124 122 2 98.3

File: project\_pack.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 13 10 3 76.9

Branches 16 14 2 87.5

FEC Condition Terms 0 0 0 100.0

FEC Expression Terms 0 0 0 100.0

States 0 0 0 100.0

Transitions 0 0 0 100.0

Toggle Bins 0 0 0 100.0

File: rcb.vhd

Enabled Coverage Active Hits Misses % Covered

---------------- ------ ---- ------ ---------

Stmts 95 92 3 96.8

Branches 71 68 3 95.7

FEC Condition Terms 9 9 0 100.0

FEC Expression Terms 4 1 3 25.0

States 6 6 0 100.0

Transitions 20 18 2 90.0

Toggle Bins 316 302 14 95.5

NEVER FAILED: 83.3% ASSERTIONS: 6

# Test 3: Random Command Testing

## Output

*# BBBB B BBBBB BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

*# BB B BB BBBBB BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

*# BB BB BBB BBBBBB BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

*# BBBBB BBBB BBBBBB BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*

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*# \*\* Note: Commands from: Test3.txt, VDP PASSED.*

## Justifications for Test

This test attempts to generate as many commands as possible to get the maximum code coverage. It uses a C++ testbench (<http://ideone.com/euh1Cg>) to generate the random commands. Colours are varied. More emphasis is placed on the draw command by weighting the command array.

## Code Coverage

This test should test most of the possible commands as it runs 100,000 randomly generated commands. It should cover all the previous corner cases and hence should have a larger code coverage.

### Overall

*Coverage Report Totals BY FILES: Number of Files 8*

*Total coverage (Code Coverage Only, filtered view): 85.9%*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *388* *350* *38* *90.2*

*Branches* *252* *216* *36* *85.7*

*UDP Condition Rows* *0* *0* *0* *100.0*

*FEC Condition Terms* *30* *29* *1* *96.6*

*UDP Expression Rows* *0* *0* *0* *100.0*

*FEC Expression Terms* *14* *10* *4* *71.4*

*States* *22* *22* *0* *100.0*

*Transitions* *60* *43* *17* *71.6*

### By File

*Coverage Report Summary Data by file*

*Total Coverage By File (code coverage only, filtered view): 88.0%*

*File: draw\_any\_octant.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *8* *8* *0* *100.0*

*Branches* *2* *2* *0* *100.0*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *2* *2* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *38* *38* *0* *100.0*

*File: draw\_octant.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *25* *25* *0* *100.0*

*Branches* *10* *10* *0* *100.0*

*FEC Condition Terms* *7* *6* *1* *85.7*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *162* *162* *0* *100.0*

*File: hdb.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *166* *153* *13* *92.1*

*Branches* *98* *85* *13* *86.7*

*FEC Condition Terms* *12* *12* *0* *100.0*

*FEC Expression Terms* *8* *7* *1* *87.5*

*States* *12* *12* *0* *100.0*

*Transitions* *32* *20* *12* *62.5*

*Toggle Bins* *366* *365* *1* *99.7*

*File: pix\_cache\_pak.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *12* *0* *12* *0.0*

*Branches* *10* *0* *10* *0.0*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *0* *0* *0* *100.0*

*File: pix\_word\_cache.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *36* *31* *5* *86.1*

*Branches* *29* *23* *6* *79.3*

*FEC Condition Terms* *2* *2* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *34* *33* *1* *97.0*

*File: pix\_write\_cache.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *33* *31* *2* *93.9*

*Branches* *16* *14* *2* *87.5*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *4* *4* *0* *100.0*

*Transitions* *8* *5* *3* *62.5*

*Toggle Bins* *124* *122* *2* *98.3*

*File: project\_pack.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *13* *10* *3* *76.9*

*Branches* *16* *14* *2* *87.5*

*FEC Condition Terms* *0* *0* *0* *100.0*

*FEC Expression Terms* *0* *0* *0* *100.0*

*States* *0* *0* *0* *100.0*

*Transitions* *0* *0* *0* *100.0*

*Toggle Bins* *0* *0* *0* *100.0*

*File: rcb.vhd*

*Enabled Coverage* *Active* *Hits* *Misses % Covered*

*----------------* *------* *----* *------ ---------*

*Stmts* *95* *92* *3* *96.8*

*Branches* *71* *68* *3* *95.7*

*FEC Condition Terms* *9* *9* *0* *100.0*

*FEC Expression Terms* *4* *1* *3* *25.0*

*States* *6* *6* *0* *100.0*

*Transitions* *20* *18* *2* *90.0*

*Toggle Bins* *316* *307* *9* *97.1*

*NEVER FAILED: 83.3%* *ASSERTIONS: 6*