Lab 2 – Design, Simulation and Experimental Verification of Sequential Logic Circuits

CEG 2136 – Computer Architecture I

Fall 2022

University of Ottawa

Lab TAs: Reza & Yang

Jaiden Clee 300174453

Jasmin Cartier 300160723

Experiment Dates: 09/29/2022 & 10/06/2022

Table of Contents

Introduction

The purpose of this lab is to understand how to implement and test sequential logic circuits on an Altera DE2-115 board using Quartus II software. More specifically, this lab demonstrated how to create synchronous counter circuits and how to test them using various methods. Testing by manual control and automatic free running testing were the methods introduced in this lab. These methods allowed the outputs of the synchronous counters to be visualized on the Altera board and on an oscilloscope. The concepts used throughout the lab helped deepen the understanding of sequential circuits and their expected outputs.

Before completing the lab, state diagrams, excitation tables, and minimized excitation equations were derived for a 3-bit synchronous modulo 6 counter and for a 4-bit synchronous BCD counter. The function of the modulo 6 counter was to count from zero to five before repeating its sequence. Similarly, the function of the synchronous BCD counter was to count from zero to nine before repeating its sequence. Both counters had one control input ‘count’ which allowed the counters to move forward in their sequence if it was active high. They also had one output, RO and BRO respectively, which was only activated during the state before returning to zero. These counters were both implemented using JK flip-flops, with active-low asynchronous reset inputs, and were all connected to one clock input.

After the circuits for these counters were implemented and tested using Quartus, they were cascaded to create a modulo 60 counter. This counter was manually tested and its outputs were visualized using the Altera board.

Design

The state diagrams of the two Moore machine counters we derived in the prelab and are shown in Figure 1 and Figure 14. At each clock pulse, they advance to the next state only when the ‘count’ input is one. The modulo 6 counter counts from zero to five before the output RO is set to one and it starts from the beginning again with RO equal to zero. The BCD counter counts from zero to nine before the BRO output is set to one and it repeats its sequence. After deriving the excitation table for the modulo 6 and BCD counters, as seen in Table 1 and Table 2 respectively, K-maps were derived to find the minimized excitation equations for each flip-flop input and the circuit output. The K-maps for the modulo 6 counter are shown in Figures 2-8 and the K-maps for the BCD counter are shown in Figures 15-23. The circuit diagrams for the counter were implemented and this is shown in Figures 9 and 24. The circuits were derived using the output of the flip-flops, the input, and some AND and NOT gates in order to produce the correct function for each flip-flop and circuit outputs.

A ‘BCD-7 segment’ symbol provided by Quartus, was used to test each circuit by manual control. The implementations shown in Figure 12 and 27 produce circuit outputs using the LED lights on the Altera board. This testing method was helpful when the counter wasn’t working properly because it was easier to localize the circuit error. For the manual testing of the modulo 6 counter, a ‘switch’ input was added to the ‘BCD-7 segment’ symbol on the most significant input bit. The modulo 6 counter has only three outputs so the added ‘switch’ input was set to zero to produce the correct circuit output. Without the ‘switch’, the missing input is set to one by default producing the wrong outputs. During manual testing of both circuits, the clock was connected to a button on the Altera board to manually control the pace of the counter.

To create the modulo 60 counter, the modulo 6 and BCD counters were cascaded by connecting the ‘BRO’ output of the BCD counter to the ‘count’ input of the modulo 6 counter. Each counter was connected to a ‘BCD-7 segment’ symbol in order to display the outputs of the modulo 60 counter on the Altera board. The two counters were set on the same clock and each time the BCD reaches 9 it allows the modulo 6 counter to advance one state in its sequence. The implementation of the modulo 60 counter is shown in Figure 31.

Simulation and Verification of Implemented Design

The correct compilation and testing of the modulo 6 counter is shown in Figure 9 and 10. On the waveform, the counter begins by staying at zero which is expected since the ‘count’ value is forced to zero. Once the ‘count’ is forced high, at every clock pulse the counter advances one state until reaching the number five. The ‘RO’ output is only equal to one when the counter displays five before repeating its sequence. The same logic is used for the BCD counter. The compilation and waveform for the BCD counter is shown in Figure 25 and 26. The BCD counter also only advances in its sequence when the ‘count’ input is high, and the ‘BRO’ output is only equal to one when the counter displays nine before repeating its sequence.

The visualization of the BCD counter outputs on an oscilloscope are shown in Figure 30. This was achieved using the automatic free running testing method. The top part of the screen shows the waveform and at the bottom you can see the count sequence from zero to nine. Connecting the oscilloscope to the Altera board and managing the ground inputs caused some minor difficulties. In addition, the oscilloscope provided at the workstation wasn’t working so the circuit was reconnected to a second oscilloscope. Although this was time consuming, it provided more practice with the oscilloscope.

Discussion

In this lab, Quartus was used to implement a 3-bit modulo 6 counter, a 4-bit BCD counter, and a modulo 60 counter. To complete this task, skills learnt in the previous lab were used and new skills were learnt during the visualization of circuit outputs on an oscilloscope.

First, the 3-bit synchronous modulo 6 counter was designed and implemented using the Quartus II software. This circuit was then compiled, and simulated using a waveform editor. The outputs displayed on the waveform were compared to the excitation table given in the lab preparation documents to check the accuracy of the implemented circuit. Once this was completed, the mod 6 counter circuit was turned into a project symbol so that the counter could be used later on. The mod 6 counter was then tested using the manual control method, allowing the outputs to be displayed on the Altera board. To test the circuit using this method, the mod 6 counter was connected to a ‘BCD-7 segment’ symbol provided by Quartus. There were initial difficulties connecting the two symbols since the mod 6 counter had three outputs but the ‘BCD-7 segment’ symbol had four inputs. Initially, the connection of these two symbols only provided three inputs to the ‘BCD-7 segment’ symbol, which caused the outputs to be displayed incorrectly on the Altera board. To solve this problem, a fourth ‘switch’ input was connected to the ‘BCD-7 segment’ symbol, to set this input to zero. This solution fixed the outputs displayed on the Altera board, and the implementation of this fourth input can be seen in Figure 12.

Secondly, the 4-bit synchronous BCD counter was designed and implemented. Similarly to the modulo 6 counter, the circuit was compiled, simulated using a waveform editor, checked for accuracy, and turned into a project symbol for later use. Then, the BCD counter was tested using the manual control method by connecting it to a 'BCD-7 segment' symbol provided by Quartus. There were no difficulties encountered when connecting these two symbols. The correct outputs were then displayed on the Altera board, and compared to the derived excitation table of the counter. Unlike the modulo 6 counter, the BCD counter was then tested using the automatic free running method. This allowed the outputs to be displayed and analyzed on an oscilloscope. To test the counter using this method, the circuit design included a symbol of the BCD counter, four ground inputs, and an added clock output. This circuit can be found in Figure 29. This circuit was compiled and then visualized on the oscilloscope. This was similar to visualizing the circuit outputs on a waveform, but on the oscilloscope the outputs were dynamic. Unfortunately, the oscilloscope at the assigned work station did not work, but the project files were saved and moved to another device which had no issues. The outputs displayed on the oscilloscope were then compared to the waveform simulation of the BCD circuit to ensure accuracy.

Lastly, the symbols created earlier of the 3-bit modulo 6 counter and the 4-bit BCD counter were cascaded to create a modulo 60 counter. Each counter symbol was connected to a 'BCD-7 segment' Quartus symbol allowing the manual testing of the modulo 60 counter. No difficulties were encountered during this part of the lab, and the correct outputs were visualized on the Altera board. The circuit design for this counter can be seen in Figure 31.

In conclusion, there were minor difficulties throughout the lab but all counters were successfully compiled and tested. This lab provided a deeper understanding of sequential circuits, specifically counters, and the different testing methods that can be used.

Appendix

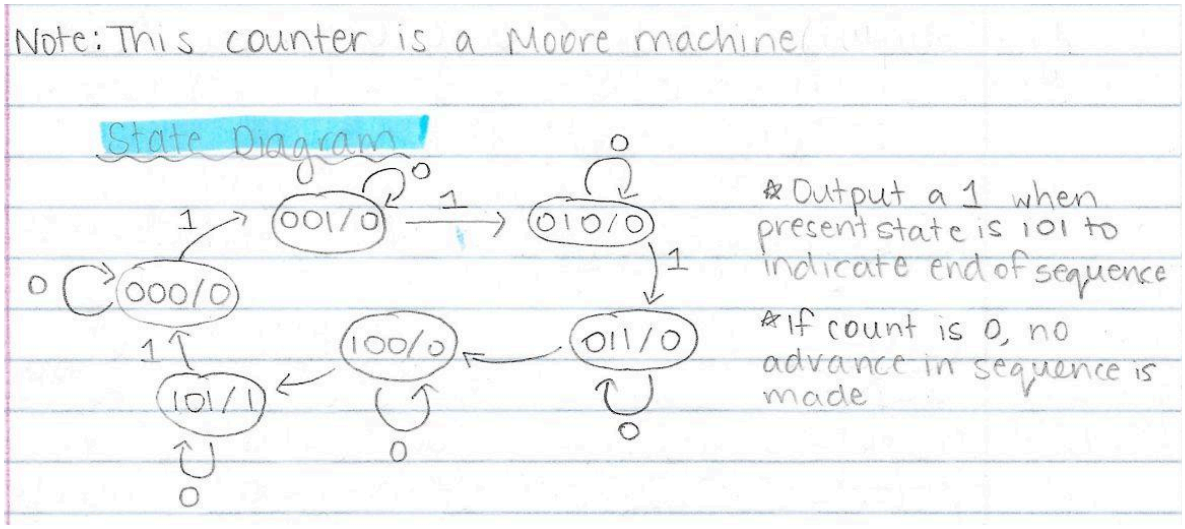

Figure 1: State diagram of the synchronous 3-bit modulo 6 counter derived during lab preparation

Table 1: Excitation table for the synchronous 3-bit modulo 6 counter

Input	Present State msb lsb			Next State msb lsb			Output	Synchronous Inputs					
count	Q2	Q1	Q0	Q2+	Q1+	Q0+	RO	J2	K2	J1	K1	J0	K0
0	X	X	X	Q2	Q1	Q0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	0	X	0	X	1	X
1	0	0	1	0	1	0	1	0	X	1	X	X	1
1	0	1	0	0	1	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	1	X	X	1	X	1
1	1	0	0	1	0	1	1	X	0	0	X	1	X
1	1	0	1	0	0	0	1	X	1	0	X	X	1
1	1	1	0	X	X	X	1	X	X	X	X	X	X
1	1	1	1	X	X	X	1	X	X	X	X	X	X

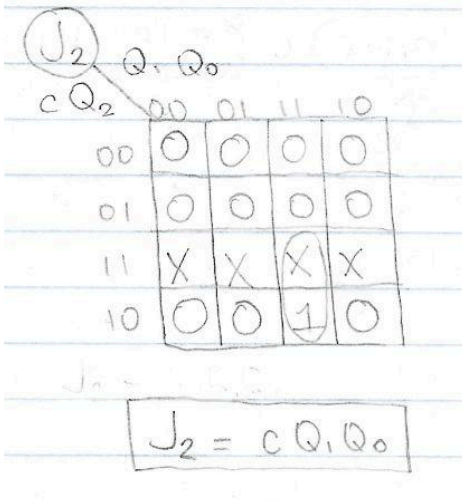

Figure 2: Karnaugh map for J2 derived from Table 1

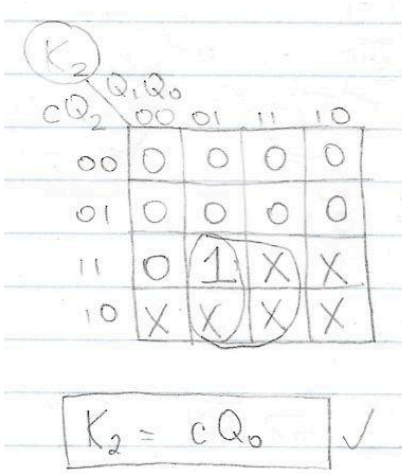

Figure 3: Karnaugh map for K2 derived from Table 1

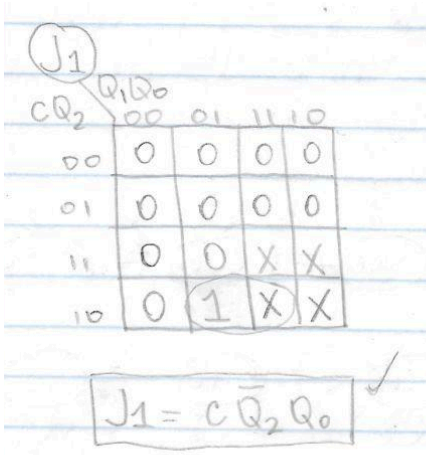

Figure 4: Karnaugh map for J1 derived from Table 1

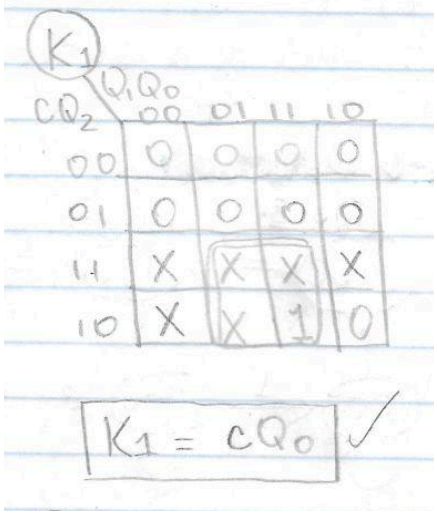

Figure 5: Karnaugh map for K1 derived from Table 1

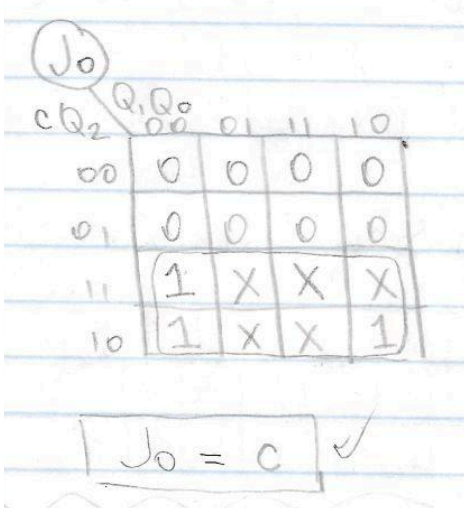

Figure 6: Karnaugh map for J0 derived from Table 1

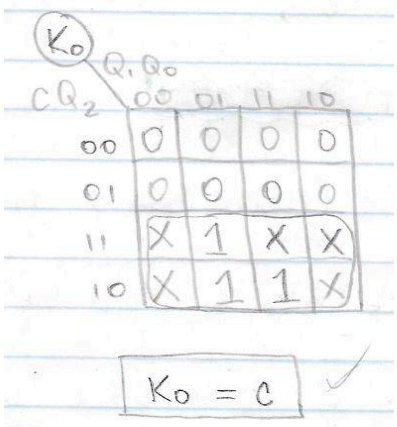

Figure 7: Karnaugh map for K0 derived from Table 1

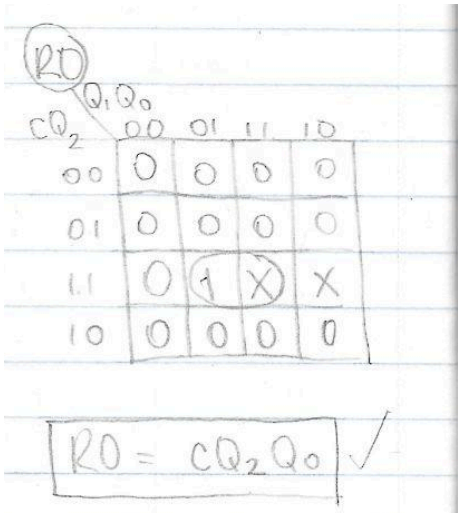

Figure 8: Karnaugh map for output RO derived from Table 1

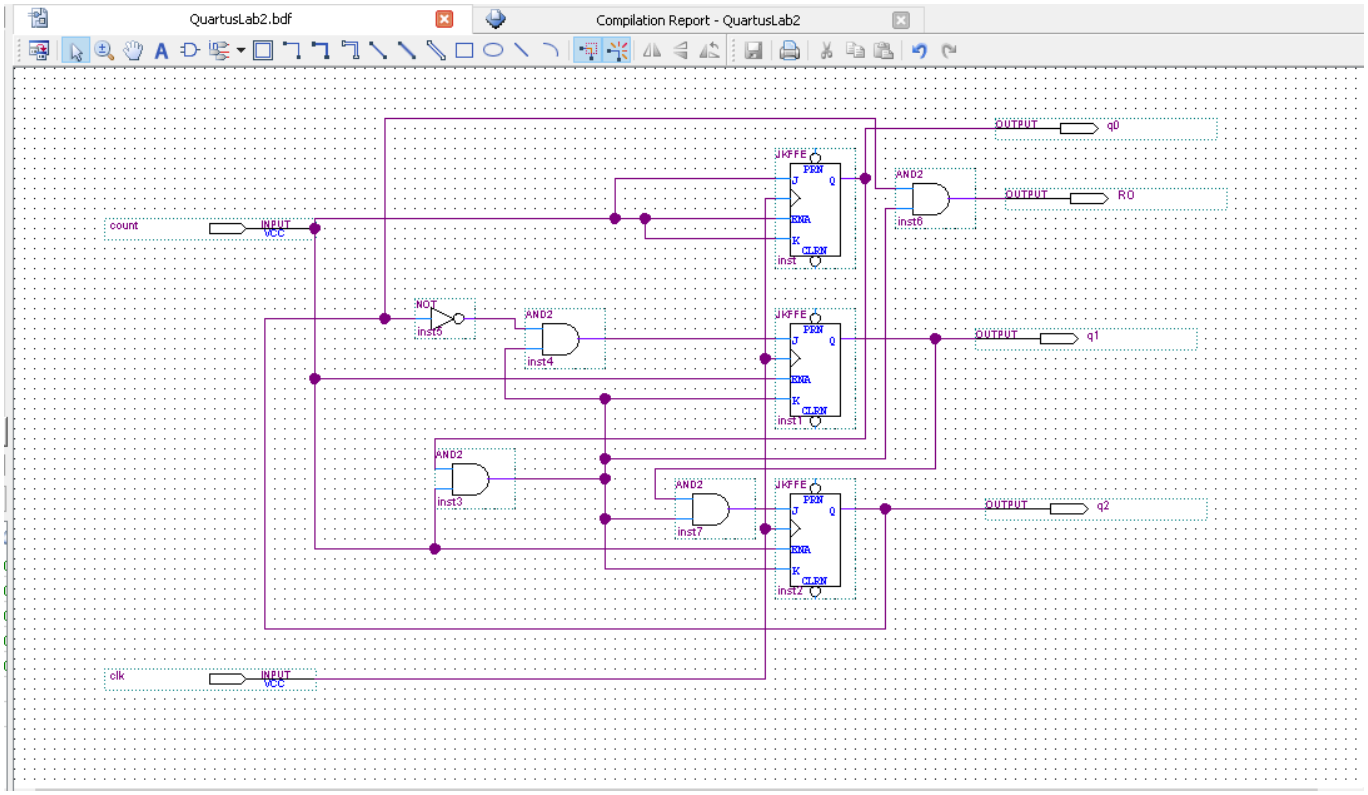

Figure 9: Circuit diagram representing a synchronous 3-bit mod 6 counter

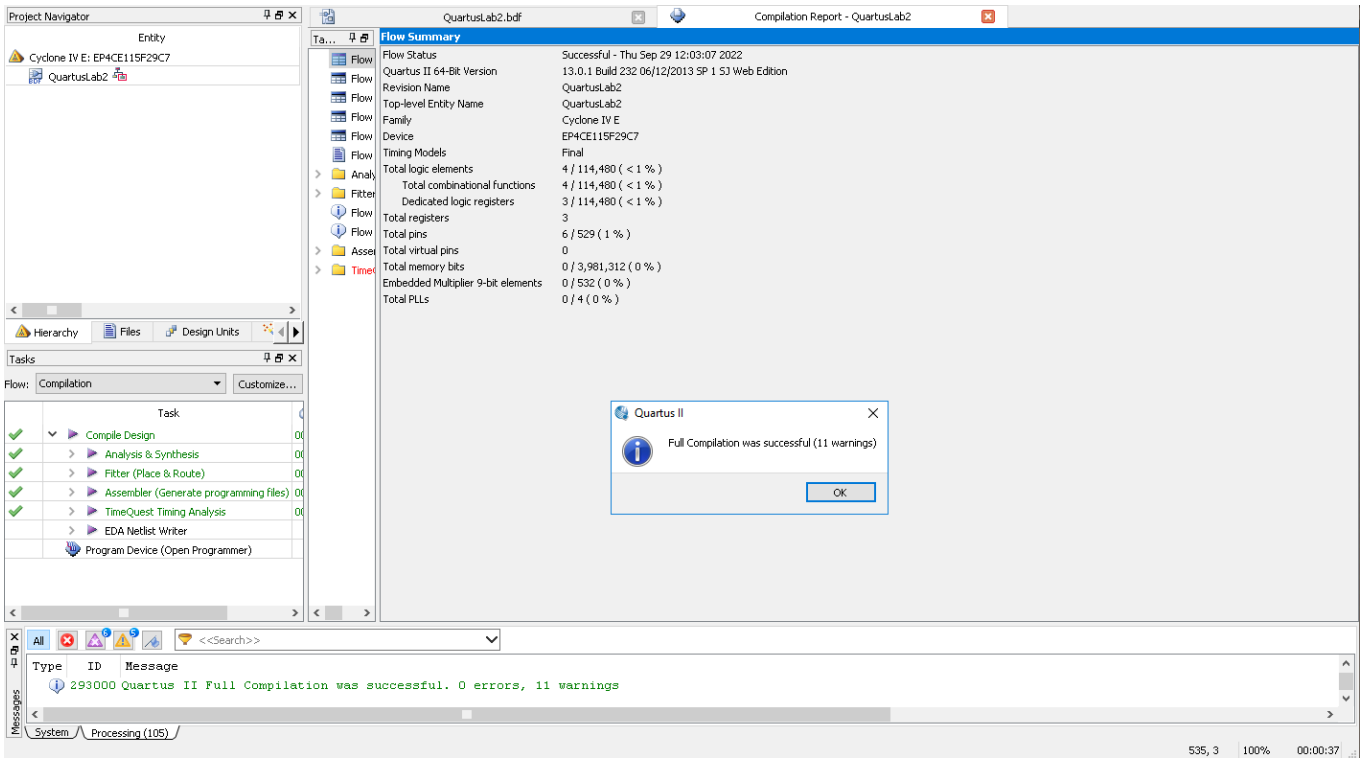

Figure 10: Compilation result of the circuit shown in Figure 9

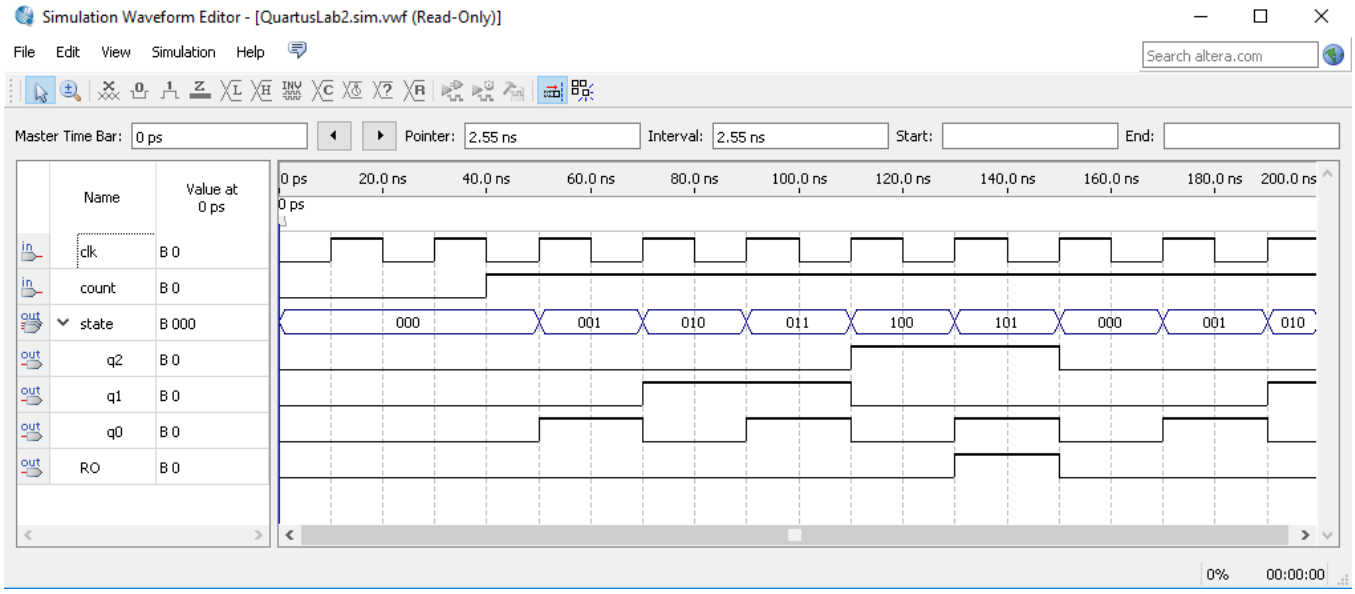

Figure 11: Simulation results of the waveform representing the circuit in Figure 9

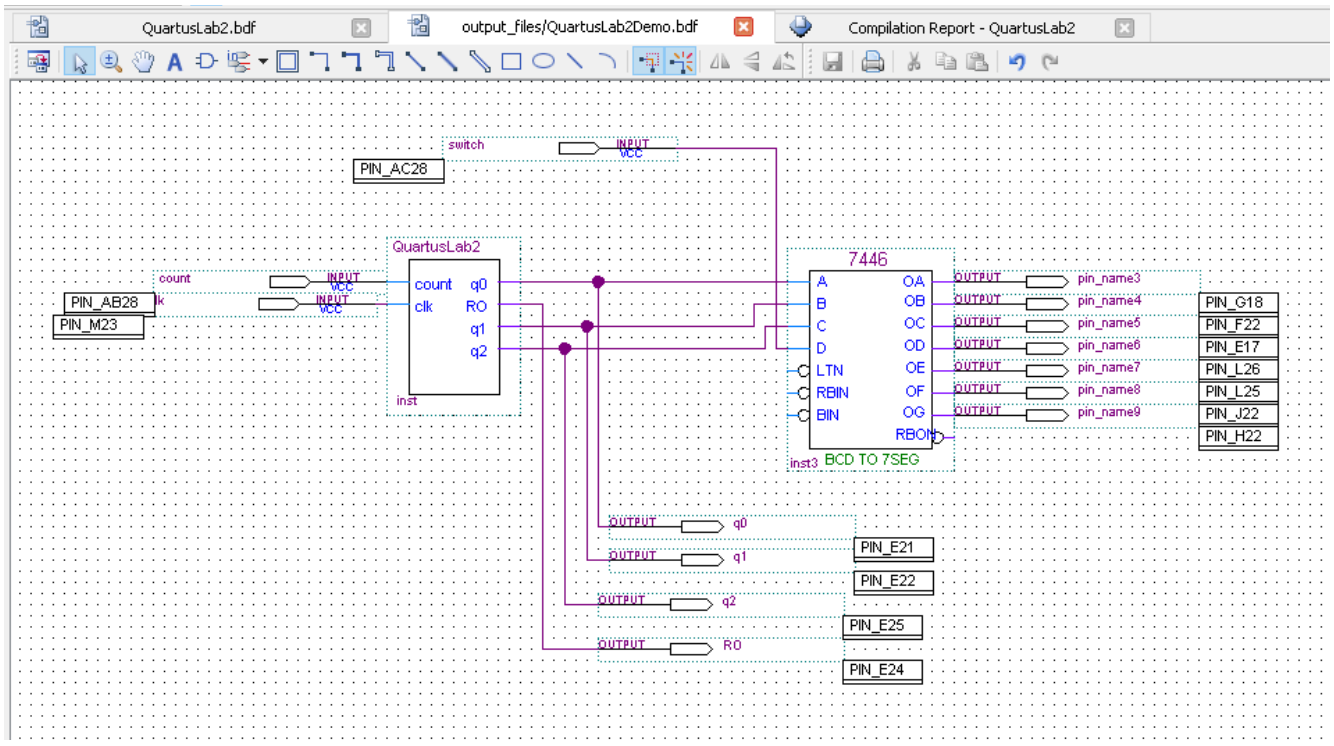

Figure 12: Circuit diagram used for the manual testing of a modulo 6 counter

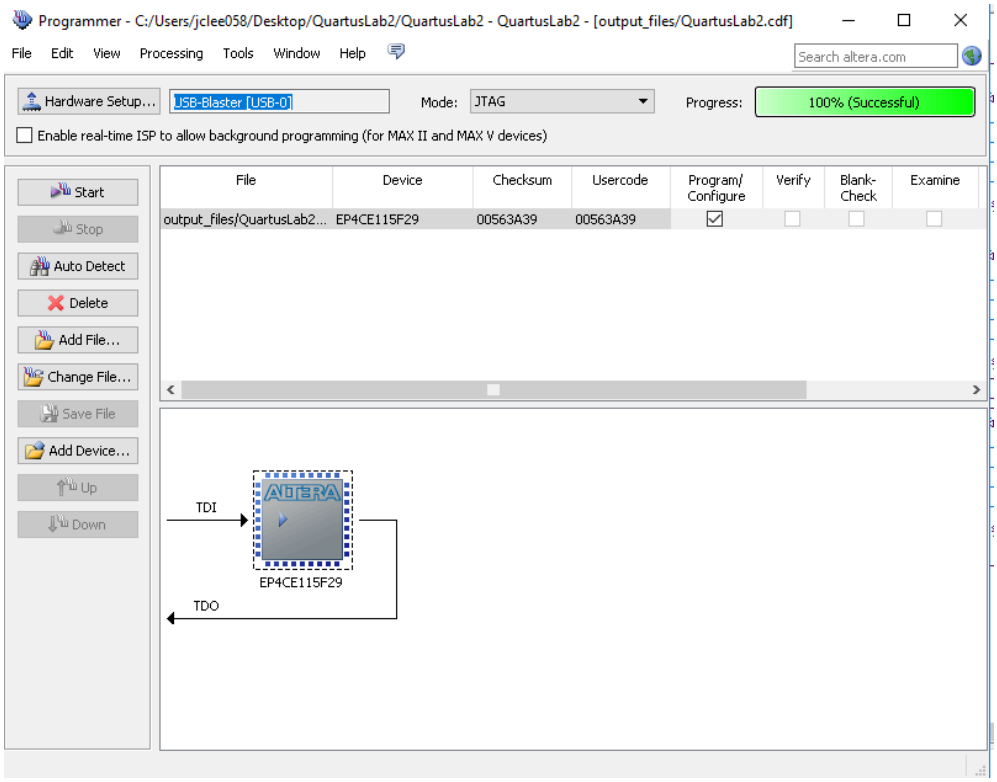

Figure 13: Programming compilation result of the circuit shown in Figure 12

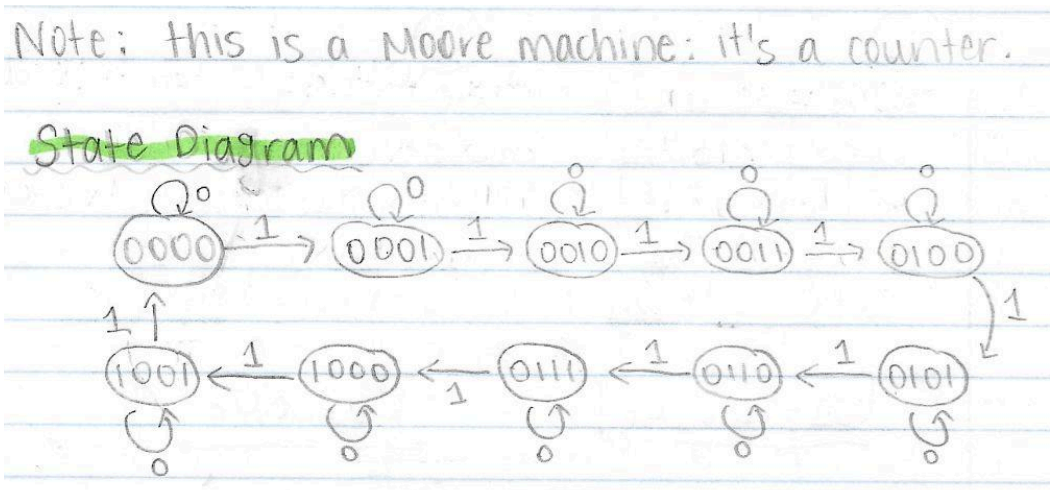

Figure 14: State diagram of the synchronous 4-bit BCD counter derived during lab preparation

Table 2: Excitation table for the synchronous 4-bit BCD 6 counter derived during lab preparation

Input	Present States msb lsb				Next States msb lsb				Output	Synchronous Inputs							
count	BQ3	BQ2	BQ1	BQ0	BQ3 +	BQ2 +	BQ1 +	BQ0 +	BRO	J3	K3	J2	K2	J1	K1	J0	K0
0	X	X	X	X	BQ3	BQ2	BQ1	BQ0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	X	0	X	0	X	1	X
1	0	0	0	1	0	0	1	0	0	0	X	0	X	1	X	X	1
1	0	0	1	0	0	0	1	1	0	0	X	0	X	X	0	1	X
1	0	0	1	1	0	1	0	0	0	0	X	1	X	X	1	X	1
1	0	1	0	0	0	1	0	1	0	0	X	X	0	0	X	1	X
1	0	1	0	1	0	1	1	0	0	0	X	X	0	1	X	X	1
1	0	1	1	0	0	1	1	1	0	0	X	X	0	X	0	1	X
1	0	1	1	1	1	0	0	0	0	1	X	X	1	X	1	X	1
1	1	0	0	0	1	0	0	1	0	X	0	0	X	0	X	1	X
1	1	0	0	1	0	0	0	0	1	X	1	0	X	0	X	X	1
1	…	…	…	…	X	X	X	X	0	X	X	X	X	X	X	X	X

Note: The bottom 6 rows have been condensed into the last row since these states are not used in the sequence of this counter.

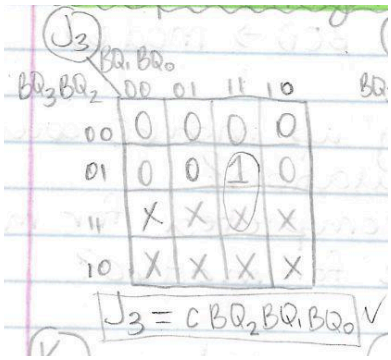

Figure 15: Karnaugh map for J3 derived from Table 2

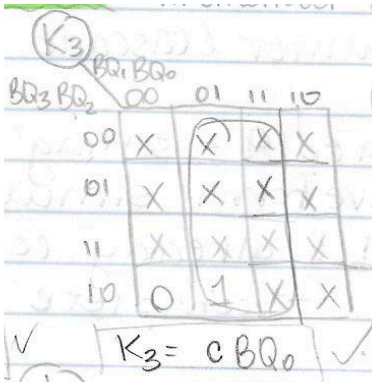

Figure 16: Karnaugh map for K3 derived from Table 2

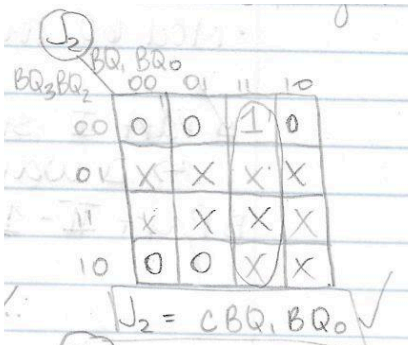

Figure 17: Karnaugh map for J2 derived from Table 2

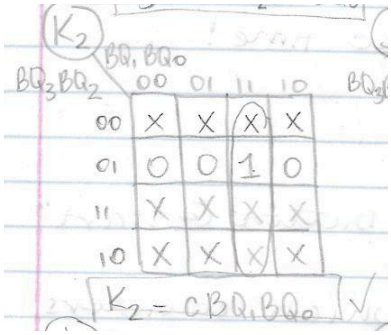

Figure 18: Karnaugh map for K2 derived from Table 2

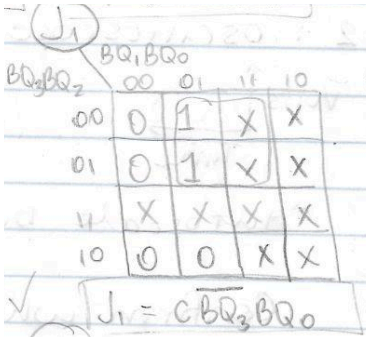

Figure 19: Karnaugh map for J1 derived from Table 2

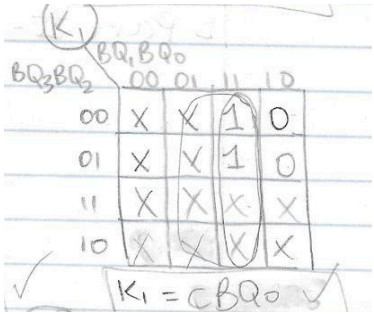

Figure 20: Karnaugh map for K1 derived from Table 2

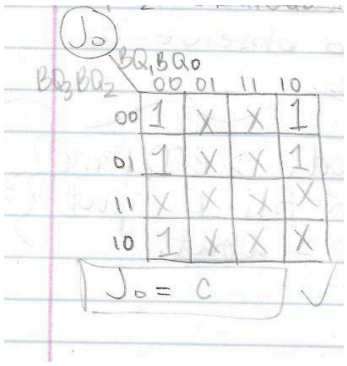

Figure 21: Karnaugh map for J0 derived from Table 2

Figure 22: Karnaugh map for K0 derived from Table 2

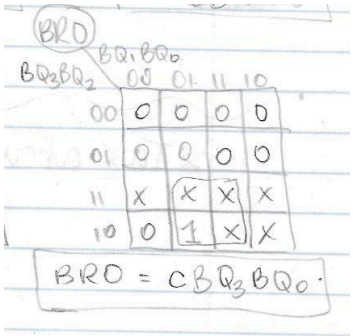

Figure 23: Karnaugh map for output BRO derived from Table 2

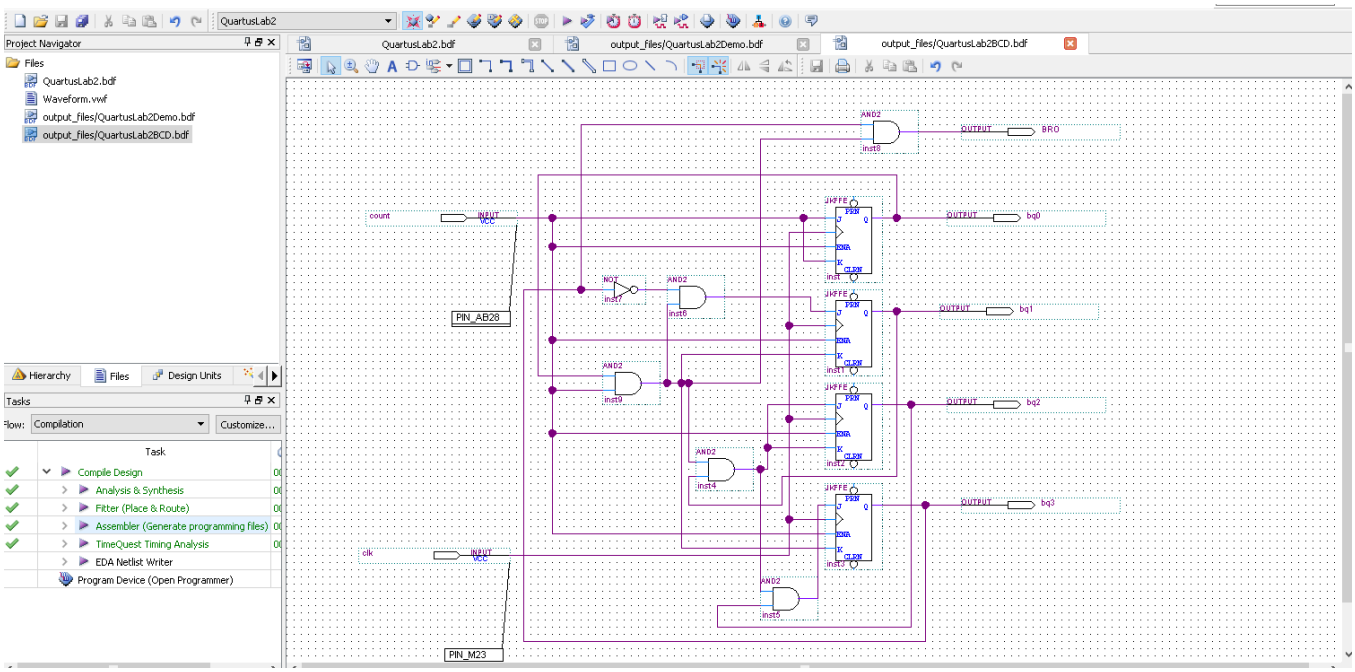

Figure 24: Circuit diagram representing a synchronous 4-bit BCD counter

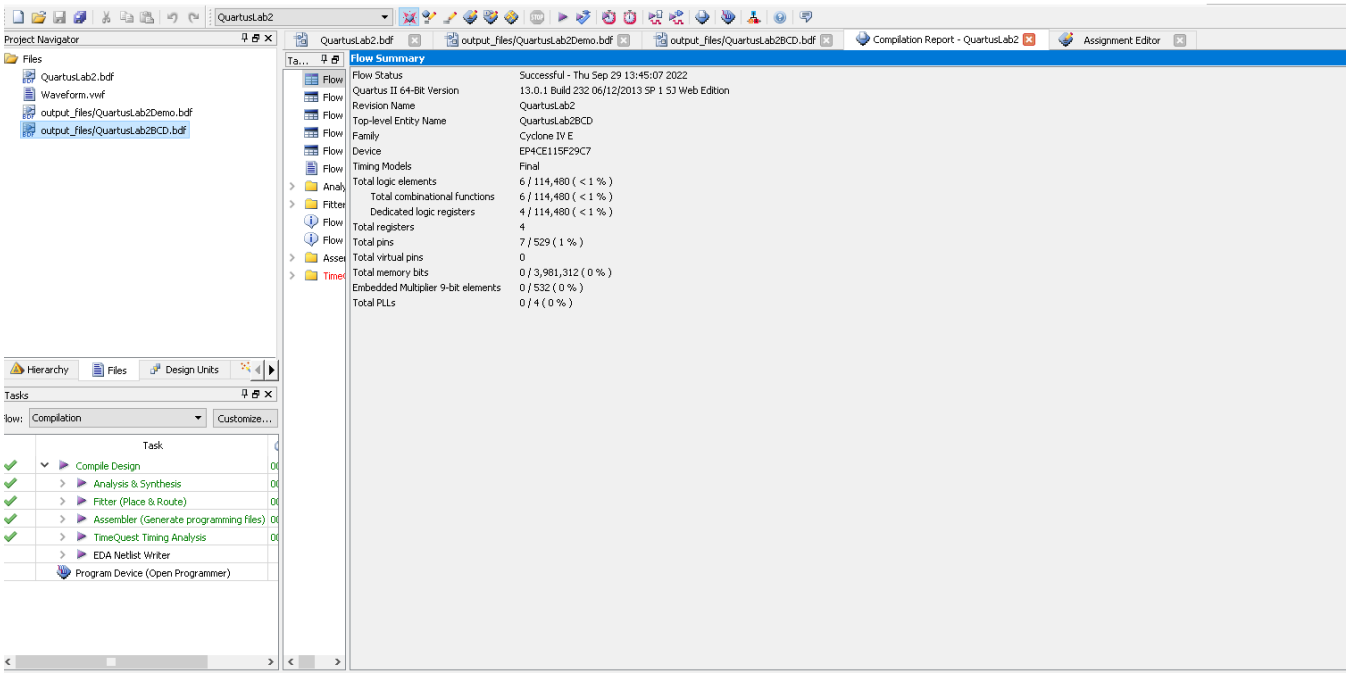

Figure 25: Compilation result of the circuit shown in Figure 24

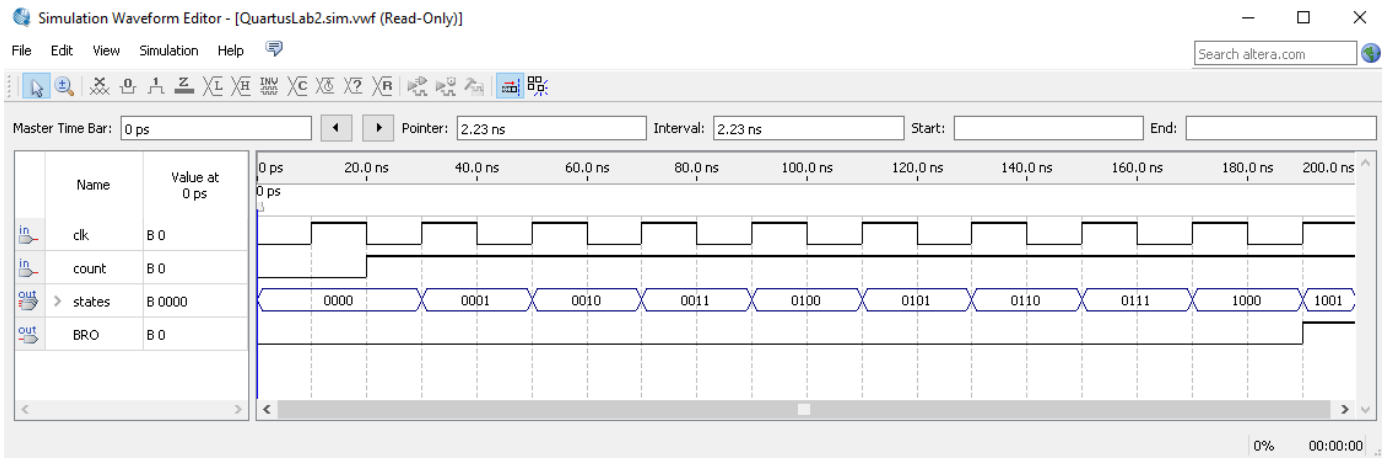

Figure 26: Simulation results of the waveform representing the circuit in Figure 24

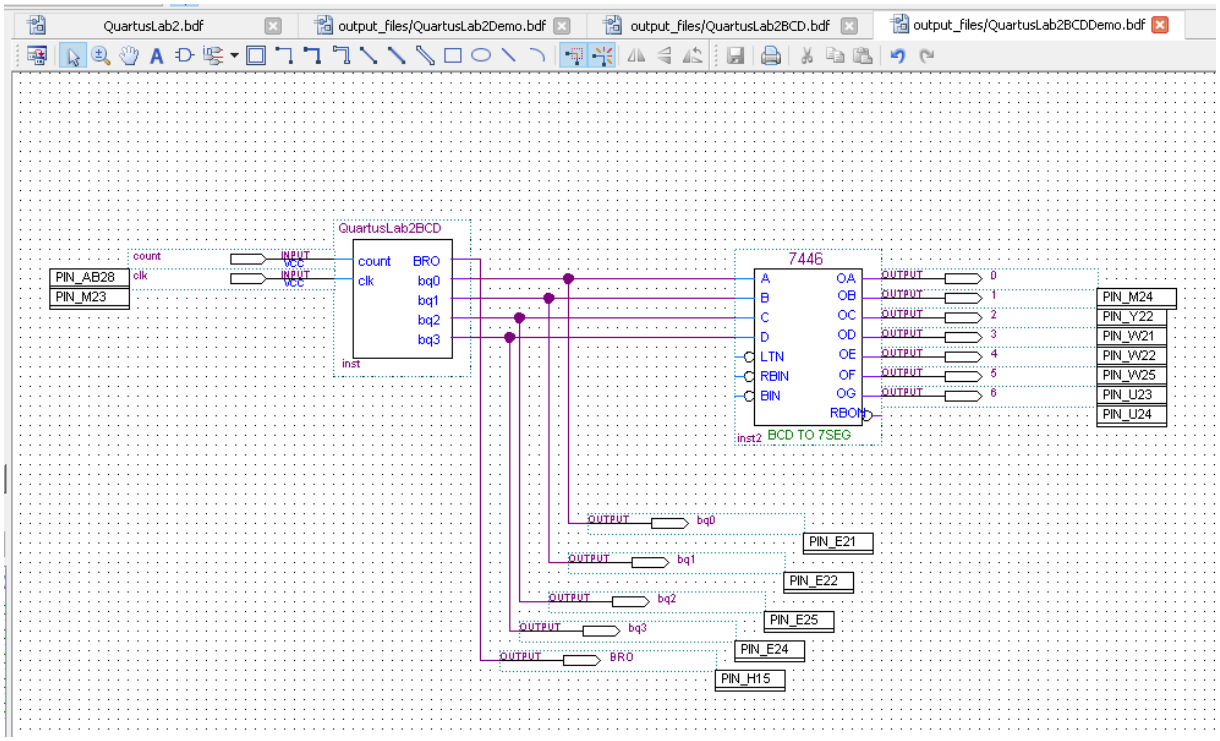

Figure 27: Circuit diagram used for the manual testing of a 4-bit BCD counter

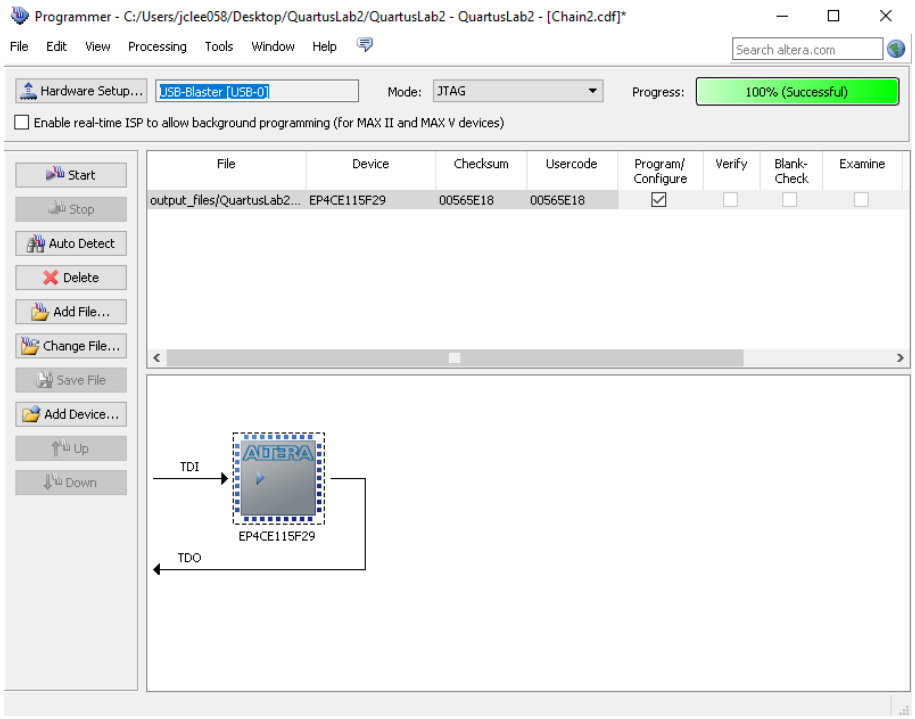

Figure 28: Programming compilation result of the circuit shown in Figure 27

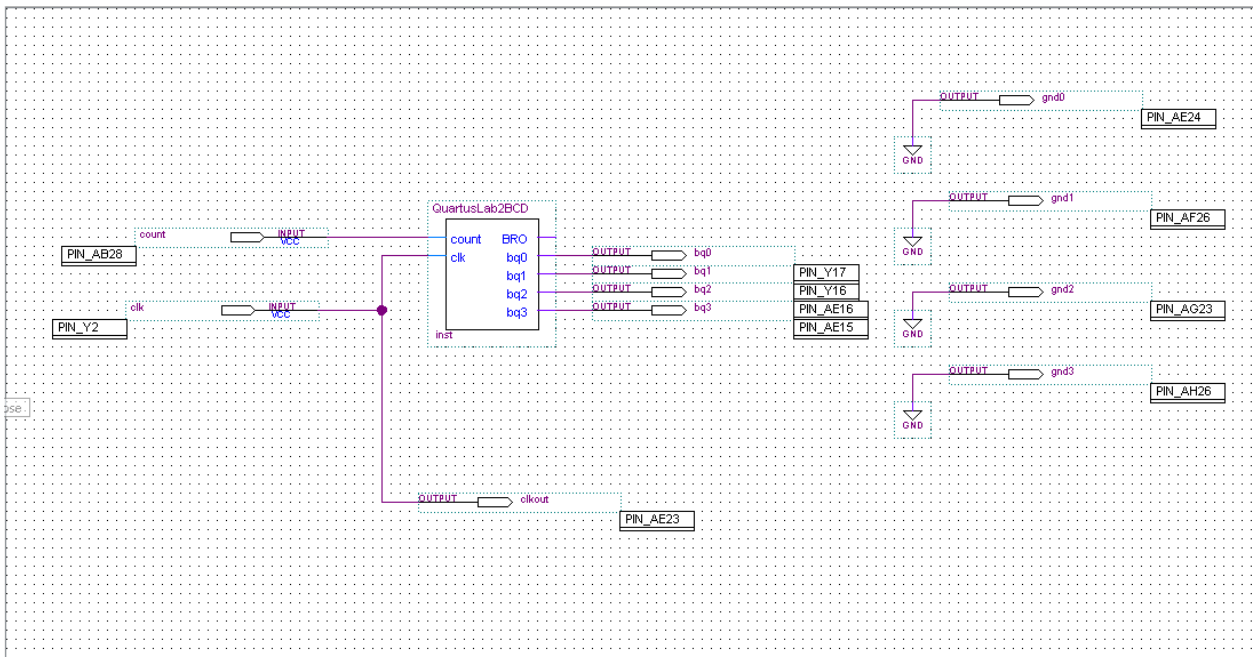

Figure 29: Circuit diagram used for the automatic free running testing of a 4-bit BCD counter

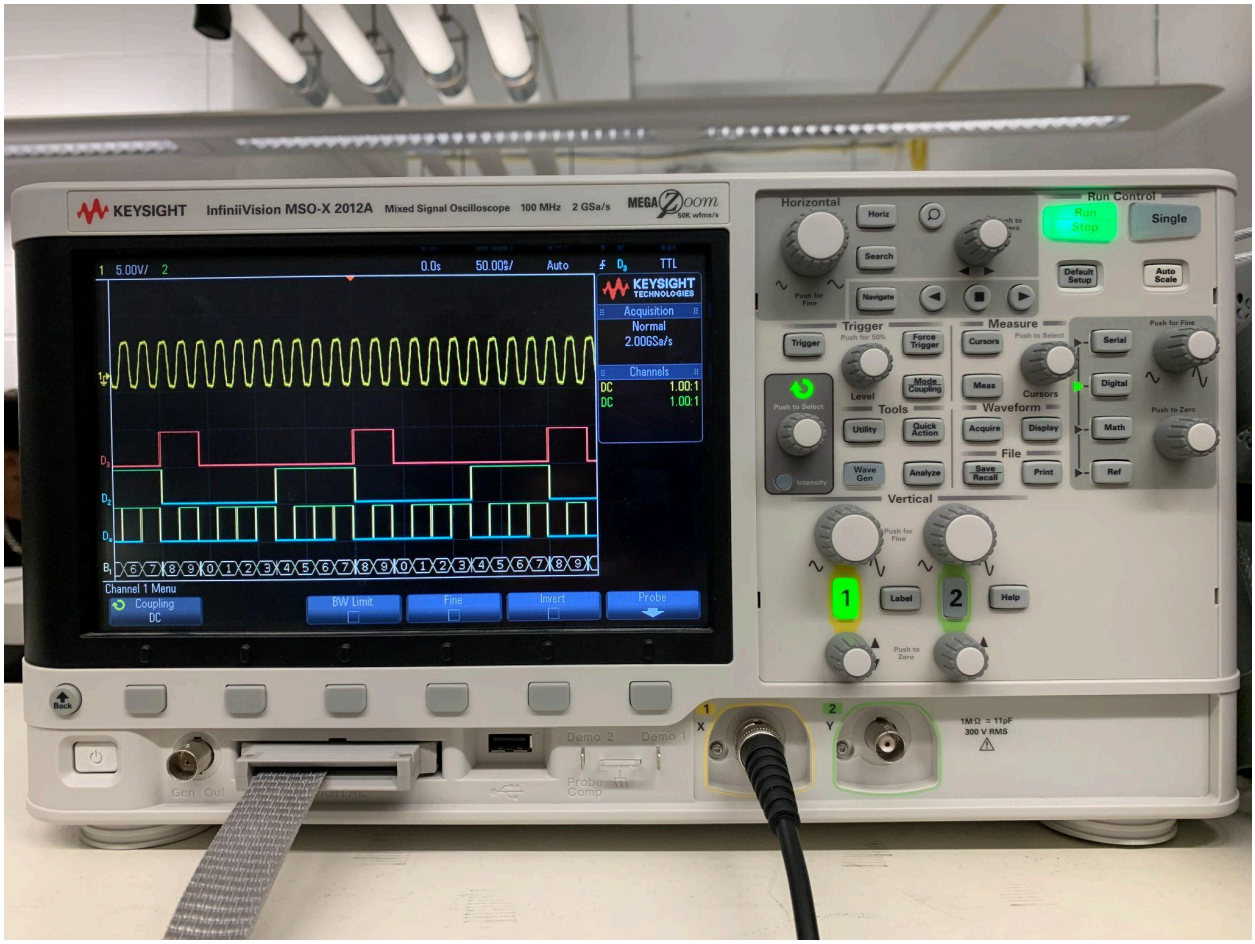

Figure 30: Visualization of BCD counter outputs on an oscilloscope

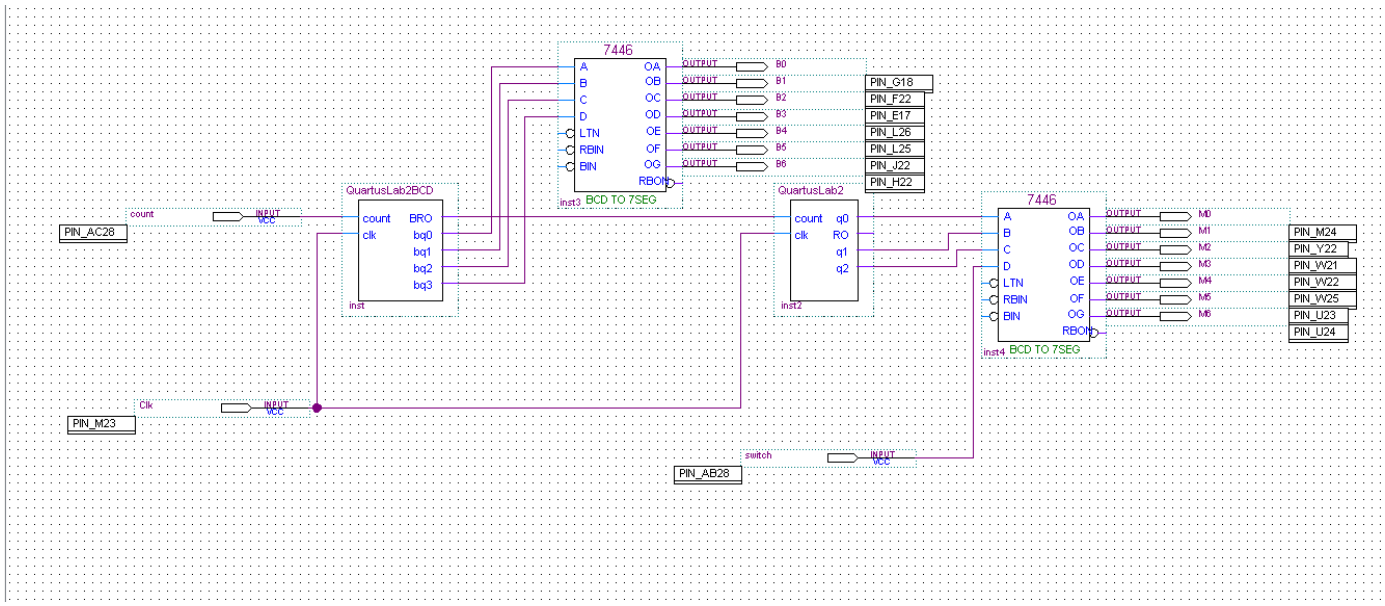

Figure 31: Circuit diagram representing a modulo 60 counter