Homework 4 – Jeremy Tandjung

Q1. (10pts) Cache and Memory mapping

Suppose a byte-addressable memory has 2M byte capacity and cache consists of 64 blocks, where each block contains 32 bytes.

Main memory = 2 MB = $2 \cdot 2^{20} = 2^{21}$

cache (# blocks) = 64 blocks = 2^6

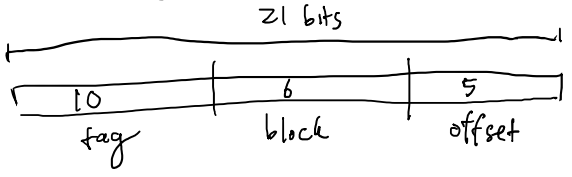
block size = 32 B = 2^5

cache size = $2^6 \cdot 2^5 = 2^{11}$

1. Direct Mapping

a) tag : $\frac{\text{main memory}}{\text{cache size}} = \frac{2^{21}}{2^{11}} = 2^{10}$ -> 10 bits

block : 6 bits ; offset : 5 bits



b) $123A63

1 0010 0011 1010 0110 0011

tag block offset

03

2 4 7 13

tag : $247

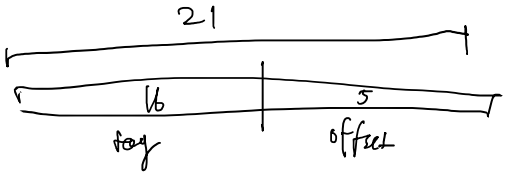
block/line : $13

offset : $03

2. Fully Associative Mapping

tag : 16

offset : 5



$123A63

1 0010 0011 1010 0110 0011

offset

tag

9 1 D 3 0 3

tag : $9103

offset : $03

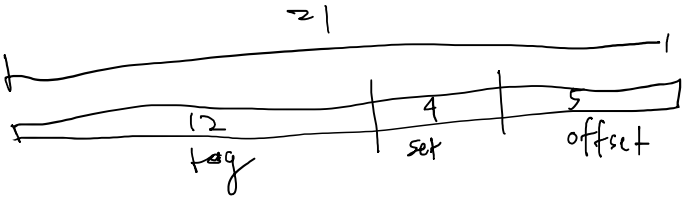
3. 4 – way set associative mapping

n = 4

offset = 2^5 ; block = 2^6

set = $\frac{2^6}{2^2} = 2^4$

tag = 21 - 5 - 4 = 12



1 0010 0011 1010 0110 0011

9 1 D 3 0 3

tag : $91D ; set: $3 ; offset $03

Q2. (10 pts) Cache hit and miss

Main memory: 256 B = 2^8
Cache size: 16 B = 2^4
Block size: 4 B = 2^2
blocks: 2^4/2^2 = 2^2

Direct Mapping (8 bits)

4	2	2
Tag	block	offset

Address	Binary	Tag	Block	Hit/Miss
$91	1001 0001	1001	00	Miss
$A8	1010 1000	1010	10	Miss
$A9	1010 1001	1010	10	Hit
$AB	1010 1011	1010	10	Hit
$AD	1010 1101	1010	11	Miss
$93	1001 0011	1001	00	Hit
$6E	0110 1110	0110	11	Miss
$B9	1011 1001	1011	10	Miss
$17	0001 0111	0001	01	Hit
$E2	1110 0010	1110	00	Miss
$4E	0100 1110	0100	11	Miss
$4F	0100 1111	0100	11	Hit
$50	0101 0000	0101	00	Miss
$A4	1010 0100	1010	01	Miss

1. Hit ratio = # hits / # address
   = 5 / 14
   = ~35.714%
2. Updated cache table

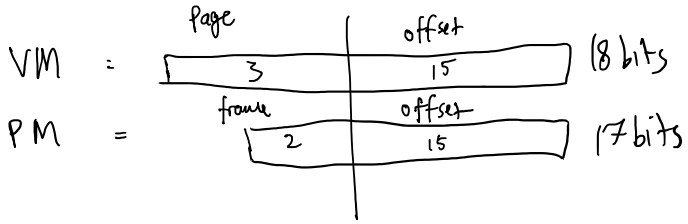
Tag	Block #	Offset 0	Offset 1	Offset 2	Offset 3
0101	0	50	51	52	53
1010	1	A4	A5	A6	A7
1011	2	B8	B9	BA	BB
0100	3	4C	4D	4E	4F

Q3. (10pts) Virtual memory and cache

1) VM = 256K = 2^{18}

PM = 128k = 2^{17}

frame = 32k = 2^{15}

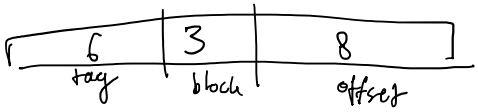


2) Tag = $\frac{2^{17}}{2^{11}} = 2^6$ ← main memory

blocks = $\frac{2^{11}}{2^8} = 2^3$

each block → 256 B = 2^8

cache size = 2^{11}



3) $ 32764

11 0010 0111 1110 0100

page ↓ offset ↓

$110_2 = 6_{10}$

∴ This will cause a page fault as the page key 6 doesn't exist (or invalid) in our initial page table

Updated tables

Mem LRU

6
0
5
4

Page table

Page	Frame
0	**2**
4	**0**
5	**3**
6	**1**

TLB

6	**1**	**1**
0	**2**	**1**

TLB LRU

6
0

Page (6; 3 bits) -> Frame(1; 2 bits)
PM -> $0A764

Cache

Line #	Tag	Data
0	10	*
1	0A	*
2	3C	*
3	14	*
4	28	*
5	04	*
6	37	*
7	**14**	*

Extra question (5 pts) Circuit and memory

1) Suppose you want to write a data 1 0 1 to the word 3 (address 3). How you will set the values in each case?

RESET	S1	S0	Bit2	Bit1	Bit0	~WE
0	1	1	1	0	1	1

2) Suppose you want to read a data from the address 1. Give the correct values in each case. If some bits do not affect, then mark as X (don't care).

RESET	S1	S0	Bit2	Bit1	Bit0	~WE
0	0	1	x	x	x	0