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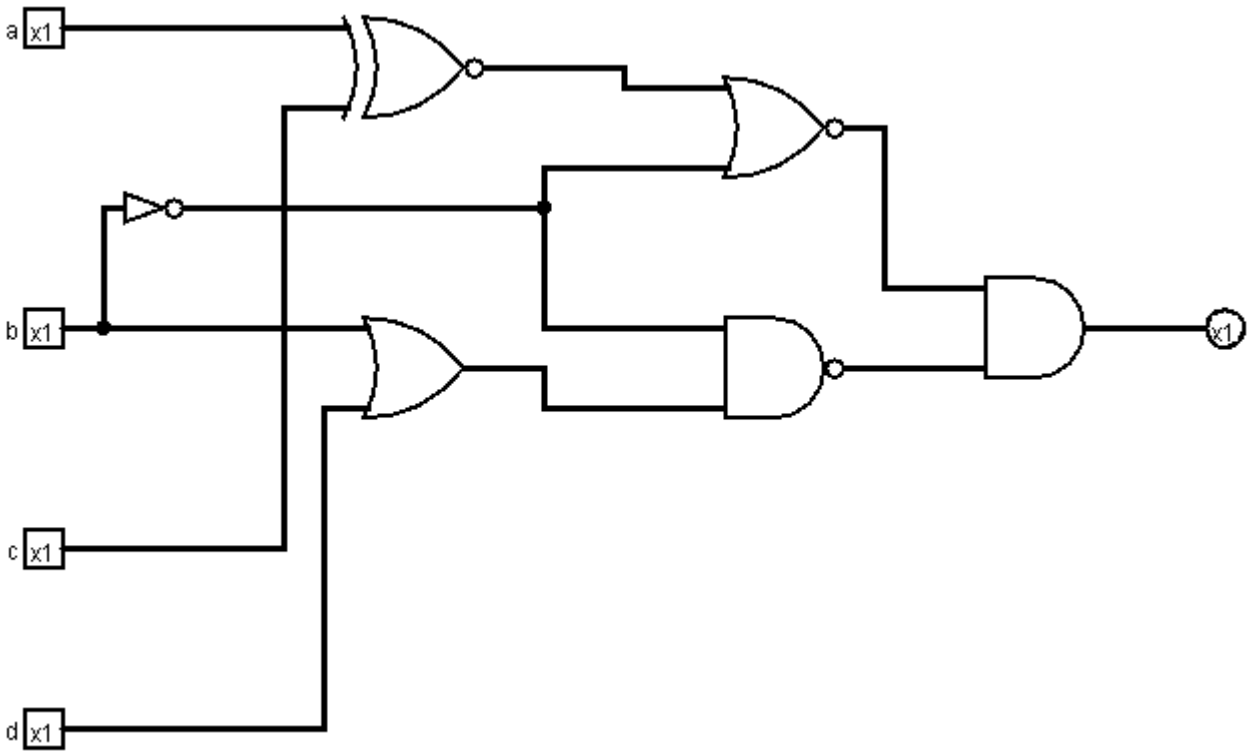
CSS 422
05/23/2020

Q1. Consider the logic gate circuit shown below

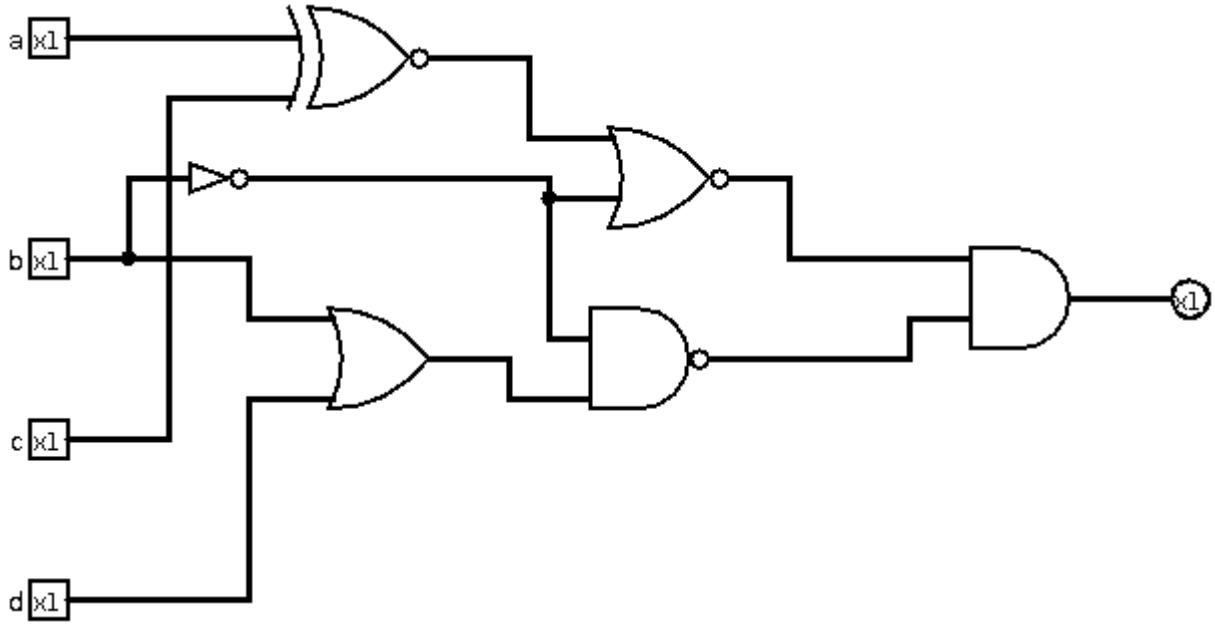


(1) ~(~(a ^ c) + ~b) * ~((b + d) * ~b)

(2)

a	b	c	d	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

(3) Also attached on canvas submission



(4) I apologize for the dark header, as the logisim on my ubuntu defaults to dark mode even when I changed my ubuntu system theme to light mode.

a b c d | x

a	b	c	d	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Q2. Design a combinational circuit system.

(1)

a	b	c	A	B	C
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

(2) & (3)

A K-map

	~x~y	~xy	xy	x~y
~z	0	1	1	0
~z	0	1	1	1

A = y + xz

B K-map

	~x~y	~xy	xy	x~y
~z	1	0	0	1
~z	1	0	1	0

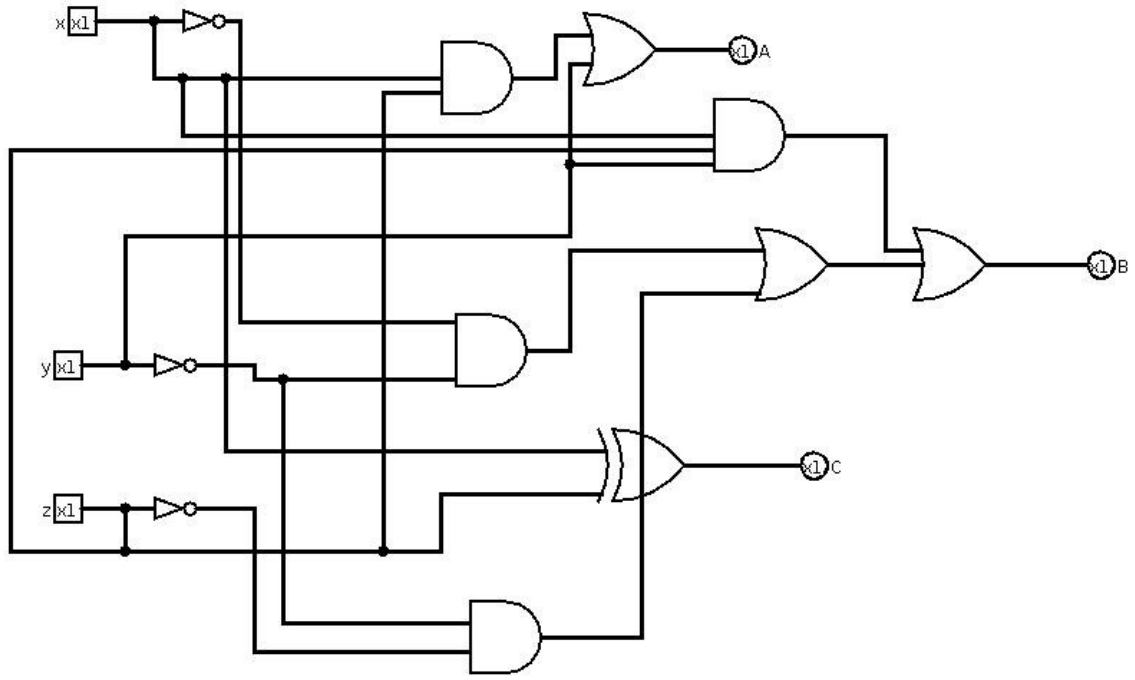
B = ~x~y + ~y~z + xyz

C K-map

	~x~y	~xy	xy	x~y
~z	0	0	1	1
~z	1	1	0	0

C = ~xz + x~z = x ^ z

(4) Also attached in canvas submission



(5)

x y z | A B C

x	y	z	A	B	C
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

Q3. Combinational circuit and Full Adder

(1)

x	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(2) S K-map

	~x~y	~xy	xy	x~y
~z	0	1	0	1
~z	1	0	1	0

S = ~x~yz + ~xy~z + xyz + x~y~z

(3) C K-map

	~x~y	~xy	xy	x~y
~z	0	0	1	0
z	0	1	1	1

C = xy + yz + xz

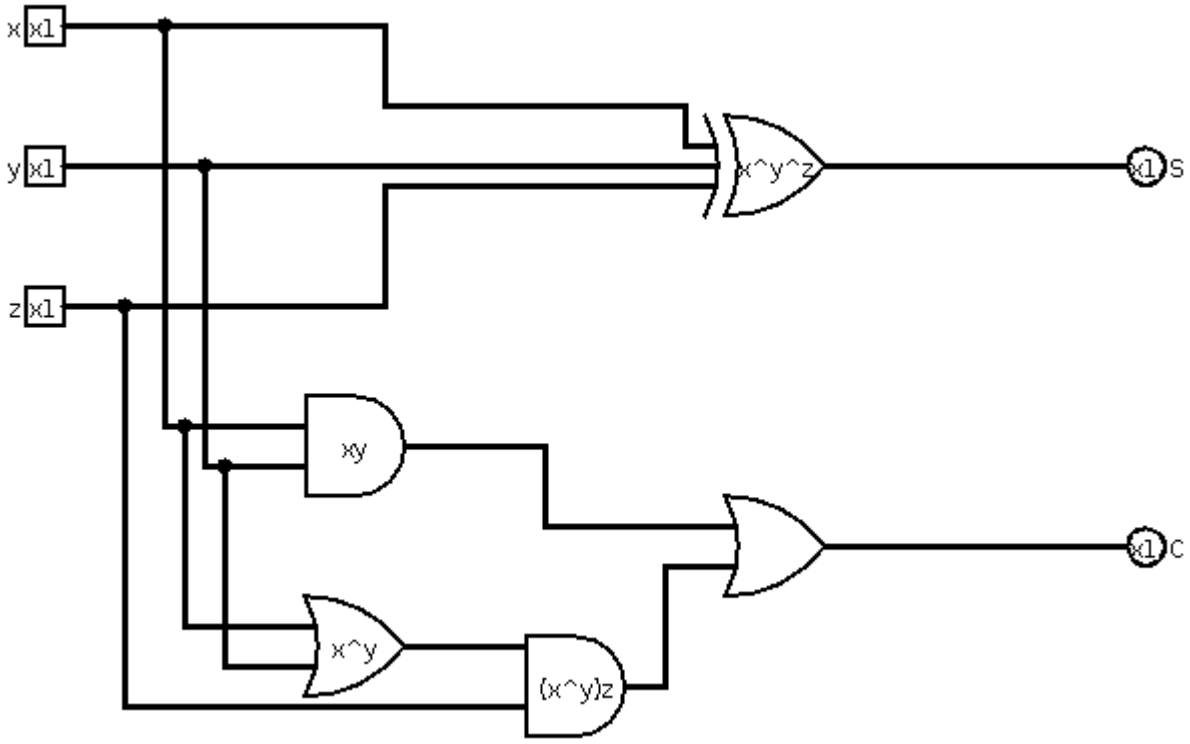
(4) (x ^ y) ^ z == ~x~yz + ~xy~z + xyz + x~y~z

(x ^ y) ^ z = (~xy+ x~y) ^ z
= ~(~xy+ x~y)z + (~xy+ x~y)~z
= (x + ~y)(~x + y)z + ~xy~z + x~y~z
= x~xz + xyz + ~x~yz + ~yyz + ~xy~z + x~y~z
= ~~x~xz~~ + xyz + ~x~yz + ~~~yyz~~ + ~xy~z + x~y~z
= xyz + ~x~yz + ~xy~z + x~y~z

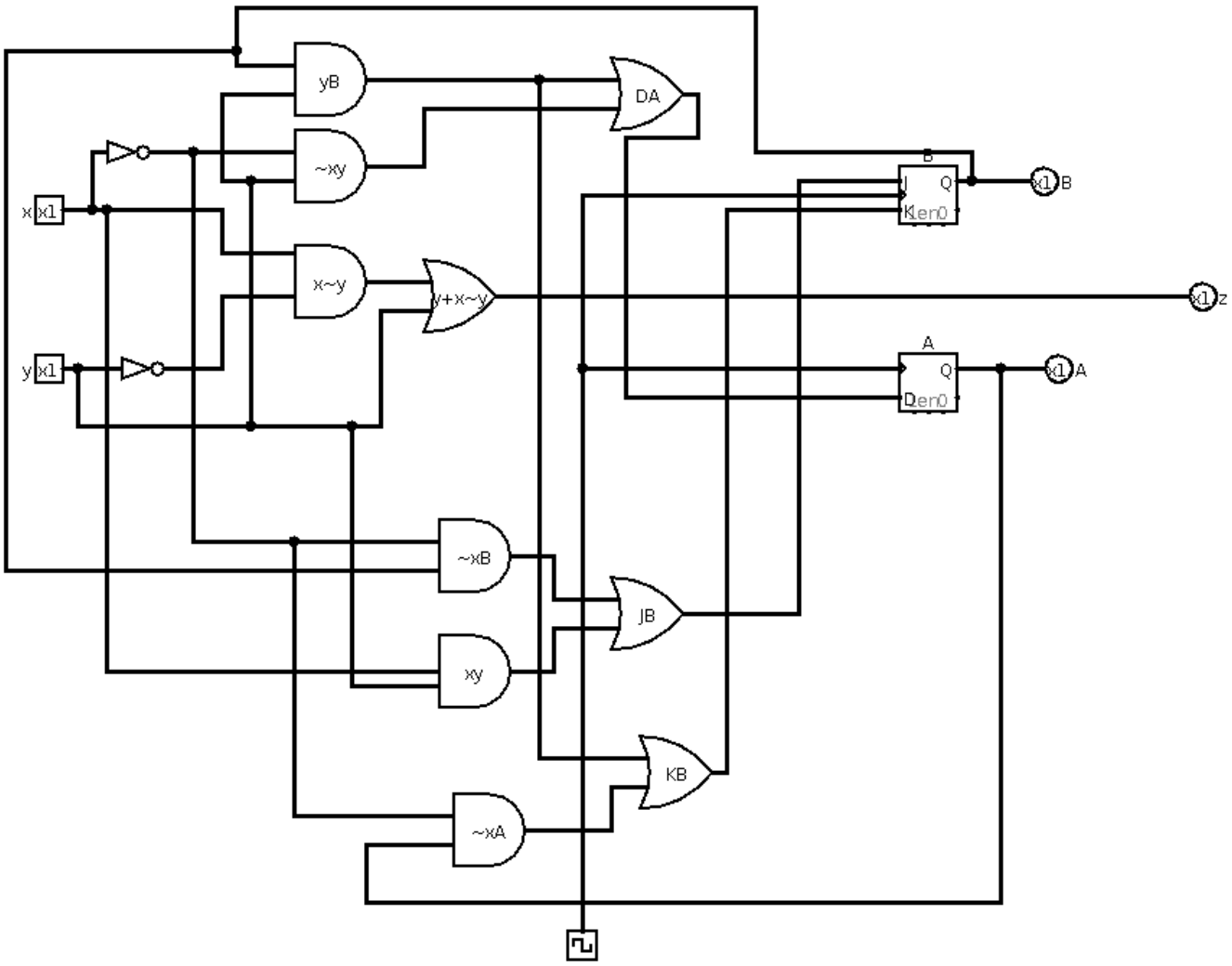
(5) xy + (x ^ y) z == xy + yz + xz

xy + (x ^ y) z = xy(1+z) + x~yz + ~xyz
= xy + xyz + x~yz + ~xyz
= xy + xz(y+~y) + ~xyz
= xy + xz + ~xyz
= xy(1+z) + xz + ~xyz
= xy + xyz + xz + ~xyz
= xy + xz + xyz + ~xyz
= xy + xz + yz (x+~x)
C = xy + yz + xz

(6)

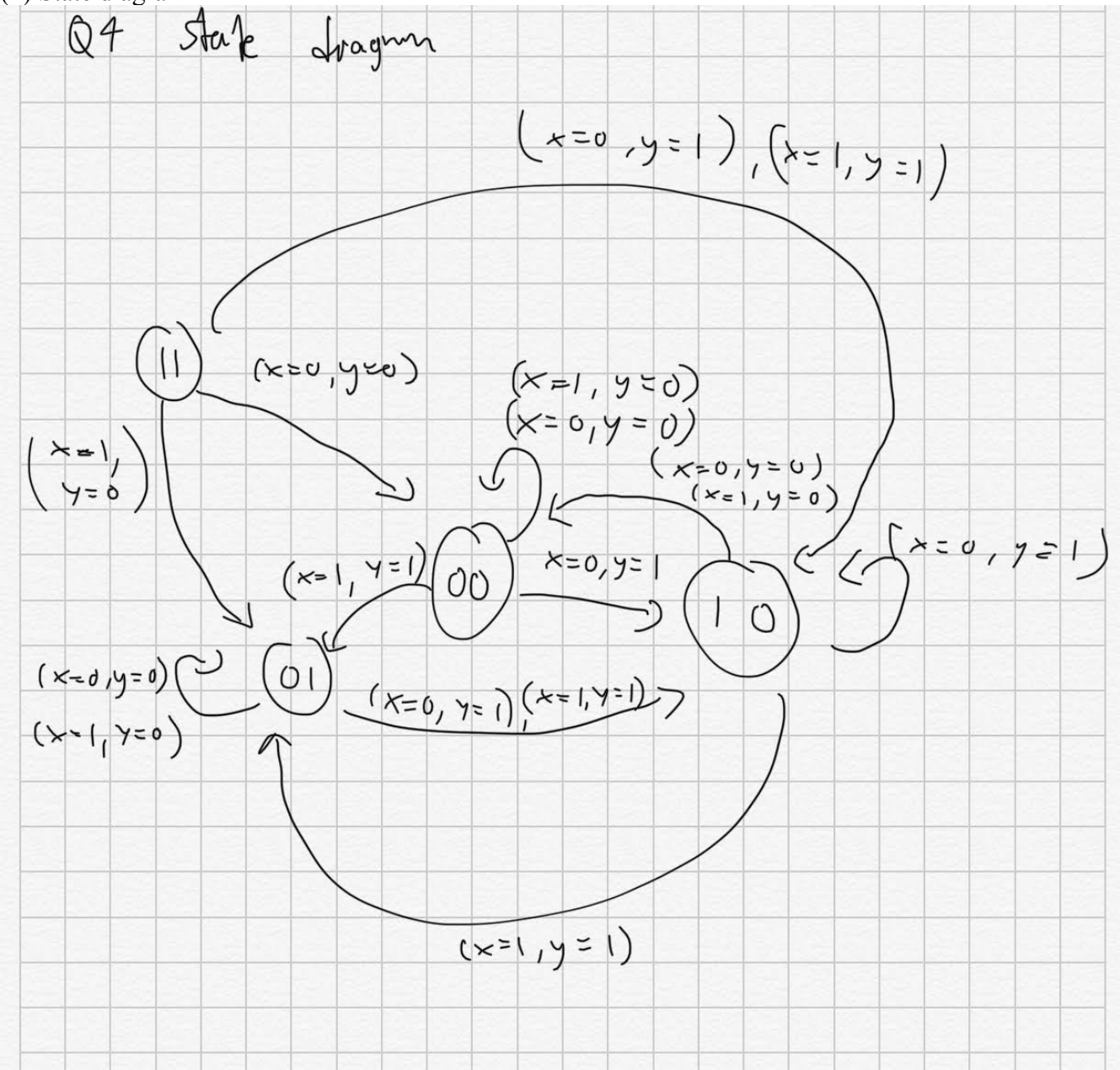


Q4. Design a sequential circuit



A(t)	B(t)	x	y	z	A(t+1)	B(t+1)
0	0	0	0	0	0	0
0	0	0	1	1	1	0
0	0	1	0	1	0	0
0	0	1	1	1	0	1
0	1	0	0	0	0	1
0	1	0	1	1	1	0
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	1	0	0	0	0	0
1	1	0	1	1	1	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0
1	0	0	0	0	0	0
1	0	0	1	1	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	1

(2) State diagram



Q5.

(2) Excitation table

Current state			Next state			Excitation					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	1	1	1	1	x	1	x	1	x
1	1	1	1	1	0	x	0	x	0	x	1
1	1	0	1	0	1	x	0	x	1	1	x
1	0	1	1	0	0	x	0	0	x	x	1
1	0	0	0	1	1	x	1	1	x	1	x
0	1	1	0	1	0	0	x	x	0	x	1
0	1	0	0	0	1	0	x	x	1	1	x
0	0	1	0	0	0	0	x	0	x	x	1

(3)

J2 K-map

	~Q1~Q0	~Q1Q0	Q1Q0	Q1~Q0
~Q2	1	0	0	0
Q2	x	x	x	x

J2 = ~Q1~Q0

K2 K-map

	~Q1~Q0	~Q1Q0	Q1Q0	Q1~Q0
~Q2	x	x	x	x
Q2	1	0	0	0

K2 = ~Q1~Q0

J1 K-map

	~Q1~Q0	~Q1Q0	Q1Q0	Q1~Q0
~Q2	1	0	x	x
Q2	1	0	x	x

J1 = ~Q0

K1 K-map

	~Q1~Q0	~Q1Q0	Q1Q0	Q1~Q0
~Q2	x	x	0	1
Q2	x	x	0	1

K1 = ~Q0

J0 K-map

	~Q1~Q0	~Q1Q0	Q1Q0	Q1~Q0
~Q2	1	x	x	1
Q2	1	x	x	1

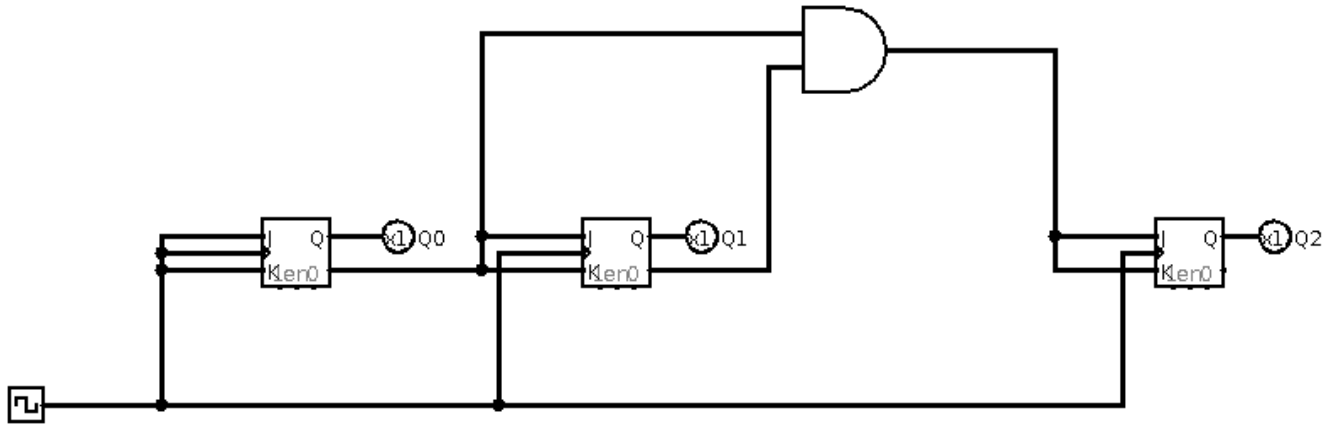
J0 = 1

K0 K-map

	~Q1~Q0	~Q1Q0	Q1Q0	Q1~Q0
~Q2	x	1	1	x
Q2	x	1	1	x

K0 = 1

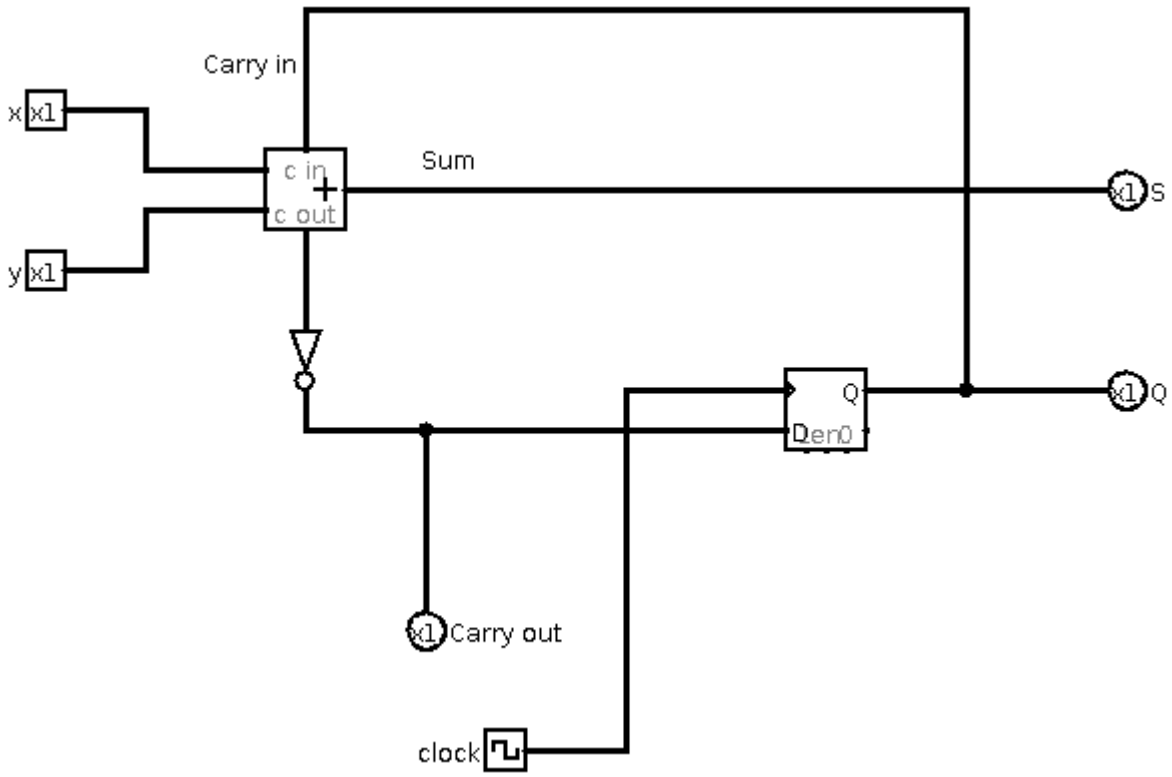
(4)



(5)

Q2	Q1	Q0
x	x	x
0	0	0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0
1	1	1

Extra Credit



X	Y	Carry in	S(t)	Carry-out (t)	S(t+1)	Carry-out (t+1)
0	0	0	0	1	1	1
0	0	1	1	1	1	1
0	1	0	1	1	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	0
1	0	1	0	0	1	1
1	1	0	0	0	0	0
1	1	1	1	0	0	0