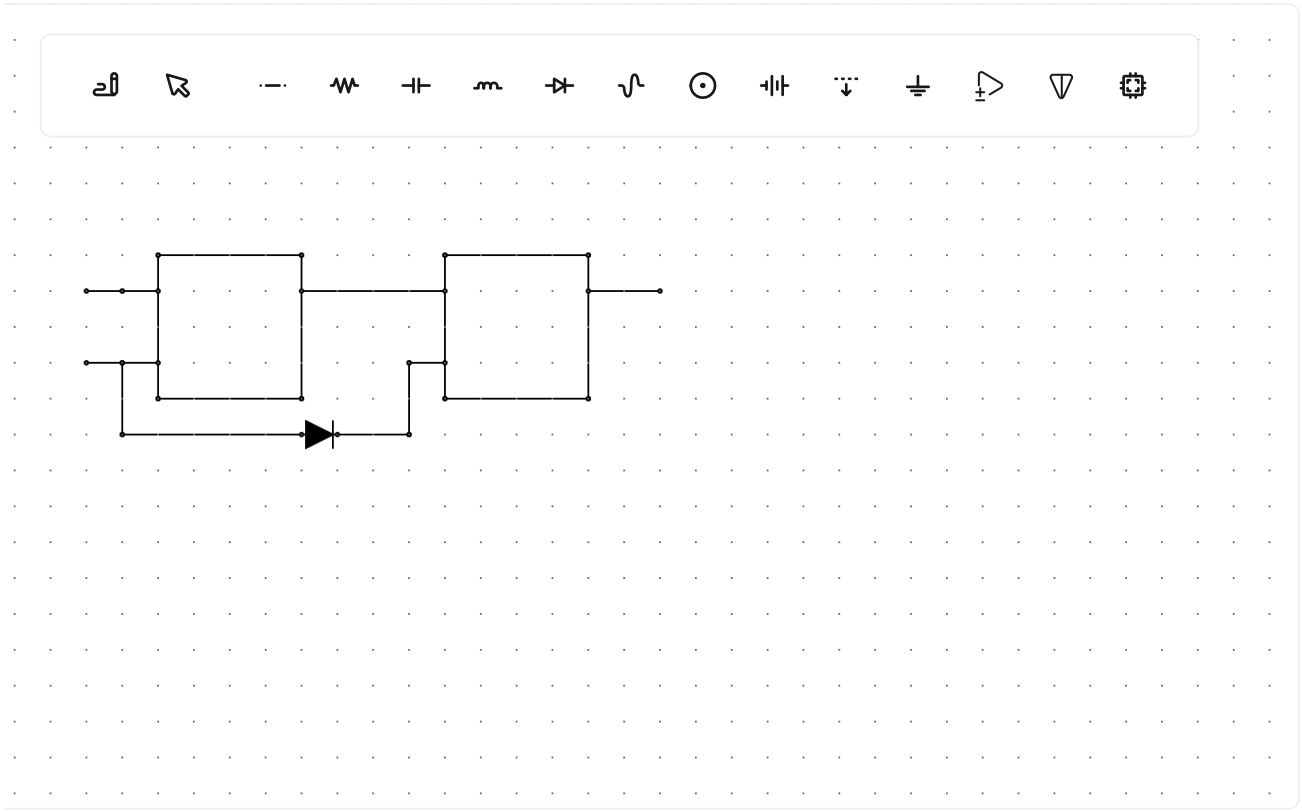


nput: D

om input: C

utputs: y1, y2

CD + C'y1

C'y1 + Cy2

'2

he tables below, stable states are coloured red.

: under standard mode of operations, only one bit can change at a time (unspecified entries due to this ar
ured yellow.

TATION TABLE:

; (y1, y2)	NS; CD = (00, 01, 10, 11) : (y2y1)	output z
	00 00 00 01	0
	11 11 00 01	0
	00 00 10 11	1
	11 11 10 11	1

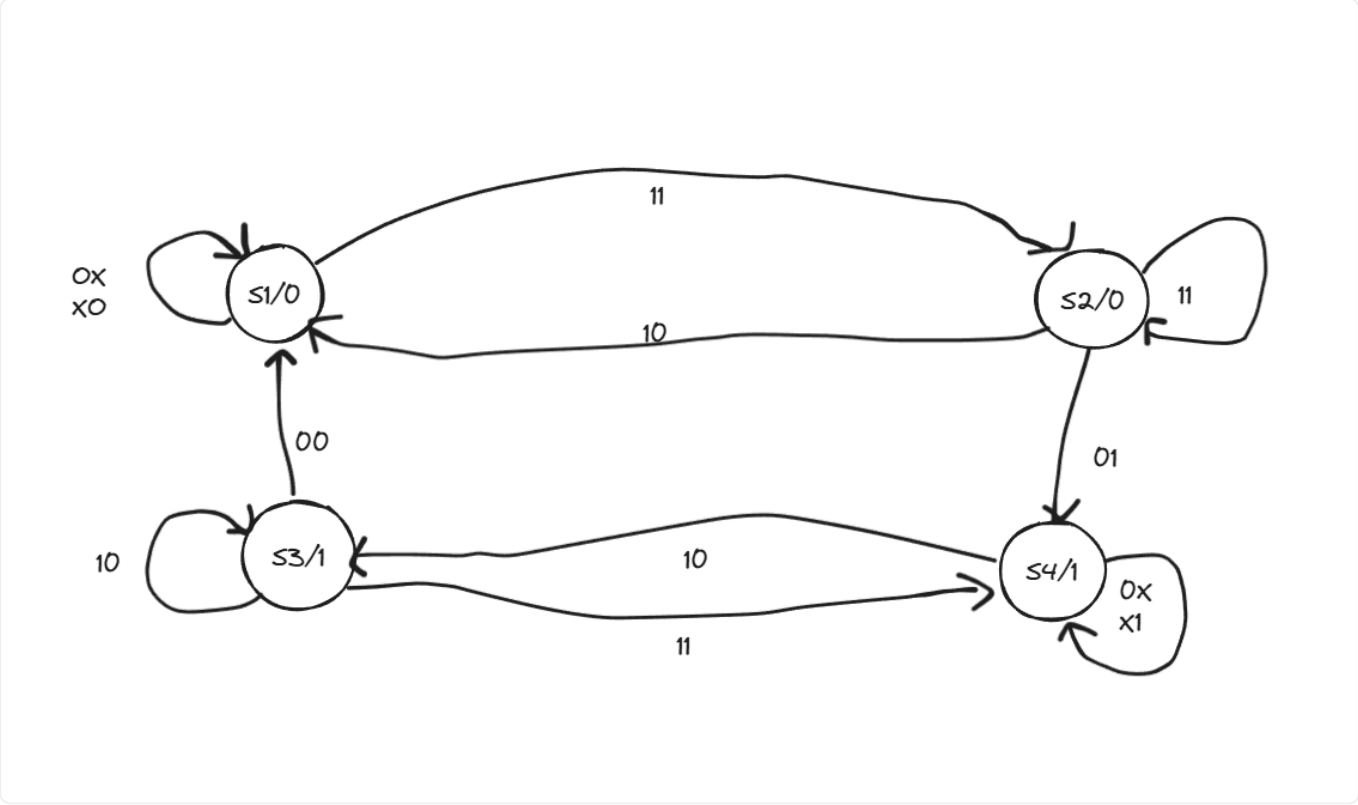
N TABLE:

; (y1, y2)	NS; CD = (00, 01, 10, 11)	Z
	S1 S1 S1 S2 S4 S4 S1 S2 S1 S1 S3 S4 S4 S4 S3 S4	0 0 1 1

IFIED FLOW TABLE:

; (y1, y2)	NS; CD = (00, 01, 10, 11)	Z
	S1 S1 S1 S2 — S4 S1 S2 S1 — S3 S4 S4 S4 S3 S4	0 0 1 1

Diagram:



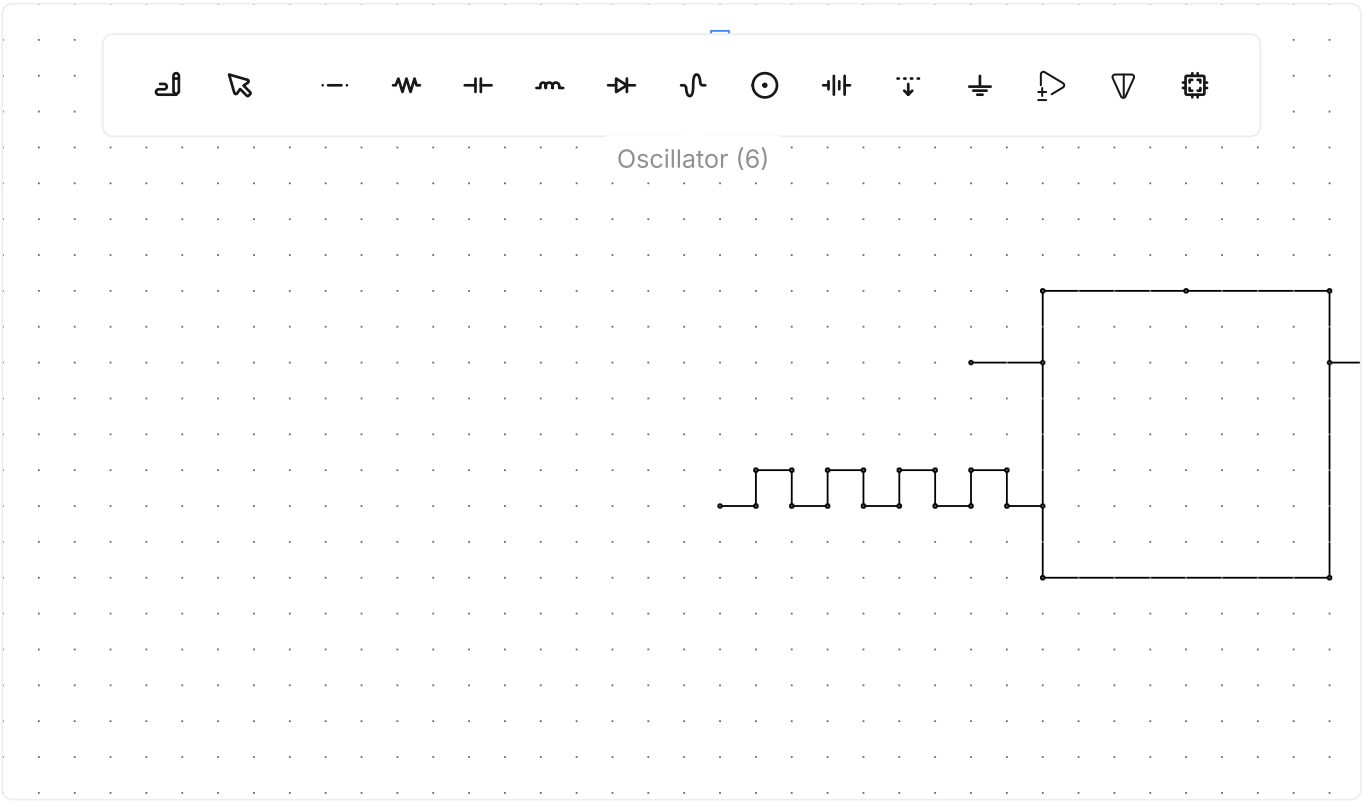
N FLOW TABLE

; (y1, y2)	NS; CD = (00, 01, 10, 11)	Z
	A B C — D B — D A C C C D C C C	0 0 1 0

C → D

YNTHESIS OF ASC

ıl Parity Generator / 1 Bit Counter/ Modulo 2 Counter:



ıput: W

ıutput: z

es, on clock signal: A, B, C, D

c ... # of pulses	z
	0 1 0 1 0

e Diagram: