Jeremy Shaw

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Work Experience

Caltrans - Engineering Intern (Office of Professional Development) 20-40 hrs/week July 2018 - Jan 2020

- Enabled greater statewide collaborative efforts between project managers to update our central project development manual with current procedures, standards, and financial methods ("Workflow Task Manual").
- Created greater internal awareness of my office's services and mission.
- Digitized in-class, professional development content and administered it via a learning management system (Moodle) to Caltrans' licensed professional engineers and engineers in training.

Projects

Skills covered: C, Python, microcontrollers, x86 asm, CAD, Verilog, RTL/EDA, UVM

"JAWOS" Time sharing OS for Intel x86 systems, developed in C and x86 assembly; gdb Fall 2019
https://github.com/jeremyshaw/JAWOS - lead a team of 3

- Worked with several other teams; the process of assisting peers required continuous revaluation and improvement of my design decisions and coding practices.
- Utilized basic Test Driven Development (TDD) techniques to rapidly iterate and test new functions using scalable, reusable methods.
- Utilized Linux-based development environment and copious amounts of GDB

"MicroGreenHouse" Web controlled & monitored greenhouse, using rPi, Python, Arduino, & C Spring 2018
https://github.com/jeremyshaw/microgreenhouse - lead a team of 4

- Learned the necessity of properly documenting my self-developed APIs and providing better code examples, as to prevent wasted work and alleviate time spent debugging the system.

"EAR" In-home robot for storing & retrieving items, using rPi, Python, Arduino, & C Fall 2019 - Spring 2020
https://github.com/JAJA-CSUS/EAR - part of a 4 person cross-disciplinary team

- Utilized design documentation to guide the team & protect the project from feature creep while setting expectations for advisors and mentors.
- Project was part of a Senior Design course (in Systems Design), covering product design, market evaluation, ethics, IEEE documentation, and design for testing.

CPU 5 stage Accumulator CPU in Verilog; UVM verification & testbenching Spring 2019

- In this project, I utilized Verilog to implement a simple, reduced ISA CPU, tested it with an instruction stream, and validated its output against expected results.

Fan Duct FreeCAD modeled, 3D Printed using PLA Summer 2019
https://github.com/jeremyshaw/fan-duct

- Iteratively created a fan duct for my desktop computer, preventing hot air recirculation and lowering load temperatures by ~8C for the CPU (from ~85C in Cinebench R15 to ~77C; 33C ambient)

GPU accelerated VM Windows Guest, Linux Host with GPU passthrough using KernelVM March 2020

- Utilized KVM & IOMMU to enable high performance GPU-accelerated applications in Win10 guest OS

Education

California State University, Sacramento GPA 3.41 January 2017 - May 2020

B.S Computer Engineering Honors and Activities: Dean's Honor List, Tau Beta Pi, IEEE, IPC, ACM

Relevant Courses

Advanced Logic Design (Digital Logic Synthesis & RTL, using **Xilinx Vivado**)
PCB Design Fundamentals (layout to manufacturing using **Altium Designer**)
CMOS and VLSI (VLSI Design and Analog Effects, using **Cadence Virtuoso** in Linux environment)
Advanced Computer Organization (Computer Architecture, x86 & MIPS)
Operating System Pragmatics (OS Architecture)
Computer Interfacing (Embedded Microcontrollers and Devices - arm)
Intermediate Object Oriented Programming
Data Structures and Algorithms
Computer Networking and Internet