# Jeremy Shaw

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Please contact me via Linkedin!

## Experience

Caltrans - Engineering Intern Worked 20-40 hours per week

July 2018 - Jan 2020

- •Created greater internal awareness of my office's services and mission by upgrading and updating our internal website (Caltrans Onramp Professional Development).
- •Enabled greater statewide collaborative efforts to update the manual with current procedures, standards, and financial methods by modernizing an ancient, central document (Workflow Task Manual).
- •Digitized in-class, professional development content and delivered it via an internal learning management system (Moodle) to Caltrans' licensed professional engineers and engineers in training.

## **Projects**

**JAWOS** Time sharing OS for Intel x86 systems, developed in C and x86 assembly <a href="https://github.com/jeremyshaw/JAWOS">https://github.com/jeremyshaw/JAWOS</a> - lead a team of 3

Fall 2019

- •Developed strong problem solving skills by working with several other teams; this required continuous reevaluation of my coding practices and design decisions.
- •Utilized basic Test Driven Development (TDD) techniques to rapidly iterate and test new functions.

**MicroGreenHouse** Web controlled & monitored greenhouse, using rPi, Python, Arduino, & C Spring 2018 <a href="https://github.com/jeremyshaw/microgreenhouse">https://github.com/jeremyshaw/microgreenhouse</a> - lead a team of 4

•Learned the necessity of properly documenting my self-developed APIs and providing better code examples, as to prevent wasted work and alleviate time spent debugging the system.

**EAR** In-home robot for storing and retrieving items, using rPi, Python, Arduino, & C Fall 2019 - Spring 2020 <a href="https://github.com/JAJA-CSUS/EAR">https://github.com/JAJA-CSUS/EAR</a> - cross disciplinary team

- •Learned documentation is to guide, but also protect the team from feature creep while setting expectations for advisors and mentors.
- •Systems Design course covering product design, market evaluation, ethics, IEEE documentation, and design for testing.

CPU 5 stage Accumulator CPU in Verilog; UVM verification & testbenching

Spring 2019

• In this project, I utilized Verilog to implement a simple, reduced ISA CPU.

**Fan Duct** FreeCAD modeled, 3D Printed using PLA <a href="https://github.com/jeremyshaw/fan-duct">https://github.com/jeremyshaw/fan-duct</a>

Summer 2019

•Iteratively created a fan duct for my desktop computer, preventing hot air recirculation and lowering load temperatures by ~8C for the CPU (from ~85C in Cinebench R15 to ~77C; 33C ambient)

**GPU powered VM** Windows Guest, Linux Host with GPU passthrough using KernelVM

March 2020

•Utilized KVM & IOMMU to enable high performance GPU-accelerated applications in Win10 guest OS

## Education

#### California State University, Sacramento GPA 3.41

January 2017 - May 2020

**B.S Computer Engineering** 

Honors and Activities: Dean's Honor List, Tau Beta Pi, IEEE, IPC, ACM

#### **Relevant Courses**

Advanced Logic Design (Digital Logic Synthesis & RTL, using **Xilinx Vivado**)

PCB Design Fundamentals (layout to manufacturing using **Altium Designer**)

CMOS and VLSI (VLSI Design and Analog Effects, using **Cadence Virtuoso**)

Operating System Pragmatics (OS Architecture)

Data Structures and Algorithms

Computer Networking and Internet

Intermediate Object Oriented Programming
Advanced Computer Organization (Computer Architecture, x86 & MIPS)
Computer Interfacing (Embedded Microcontrollers and Devices)