

JEREMY SZETO (916) 696-1333

jjszeto@calpoly.edu | jeremyjszeto@gmail.com | [linkedin.com/in/jeremyszeto](https://www.linkedin.com/in/jeremyszeto) | github.com/jeremyszeto | devpost.com/jeremyszeto

EDUCATION

California Polytechnic University SLO – Computer Engineering

Expected Grad **June 2022**

Overall GPA: **3.7**

Relevant Coursework: Computer Architecture, Systems Programming, Computer Digital Design, Embedded Systems, Data Structures, Object-Oriented Programming, Electric Circuit Analysis I, II & III, Electronics Manufacturing, Technical Writing

Programming Languages: Python, Java, C, RISC-V Assembly, ARM Assembly. *Currently learning JavaScript, C++.*

Skills: SystemVerilog, FPGA, Vivado, Git, Bash, Web Development, Arduino, Raspberry Pi

PROJECTS – Available on GitHub

ARM Thumb Simulator

Spring 2020

Implementing an ARM Thumb Simulator in C++ to study performance metrics of several sample programs. Collecting benchmark performance and operation statistics and understanding how to best optimize code samples. Includes support for most instructions in the ARM Thumb instruction set.

Skills Developed: ARM Assembly, pipelining, cycle timings and interlock behavior, CPU performance optimization, branch prediction, memory cache usage.

C Shell

Winter 2020

Programmed a basic Unix shell using C89. Implemented pipelining, fork-exec calls, and I/O functionality. Used dynamic memory allocation. Shell included “built-in” commands such as exit and cd. Pipeline supported a maximum of 20 commands and file input/output for each command. Errors were checked and handled.

Skills Developed: Pipeline workflow, fork-exec behavior, programming for portability, C language, error handling.

Custom RISC-V Microcontroller Etch-A-Sketch

Fall 2019

Used SystemVerilog to model the various components and architecture of a RISC-V microcontroller. Created individual datapath modules and control unit, tested via virtual simulation and physically programming a Xilinx BASYS3 FPGA. Wrote assembly code and C to study the low-level interactions between hardware and software. Programmed Etch-A-Sketch tool in C, using an interrupt service routine for the reset functionality and polling for directional inputs via button presses. Implemented eraser toggle, drawing speed controls, and color options via switches, with visual feedback via the onboard seven-segment display.

Skills Developed: C and RISC-V assembly programming, memory and runtime efficiency, writing hardware drivers. Structural modeling, timing diagrams, finite state machine implementation, load-store architecture flow.

Collect the Clovers Game

Fall 2019

Refactored a large (>2500 lines) codebase in Java with object-oriented programming conventions and simplified the code structure, added functionality and user-interactive elements: mouse click, character movement via directional keys, character interaction and behavior changes based on distance to enemies, hazards, obstacles, and collectible items. Implemented various pathing algorithms (A*, Dijkstra, etc)

Skills Developed: Java programming, OOP fundamentals, UML diagrams, Factory Design Method, Strategy Design Pattern.

Huffman File Compressor

Spring 2019

Implemented a Huffman file compression system using a binary tree data structure. Program parsed through a text file and arranged characters as nodes in the tree to assign smaller bit values to each, making it more space efficient than the standard 8-bit ASCII values assigned to each character.

Skills Developed: Python programming, data structures, sorting algorithms, efficient coding practices, Big O notation.

WORK EXPERIENCE

Instructional Student Assistant – Computer Digital Design Class

Winter 2020 - Current

Assist students with designing and testing RISC-V MCU in the lab portion of course. Responsible for debugging individual projects, designing thorough simulation cases for testing, and validating hardware assignments (SystemVerilog) and software assignments (Assembly and C). Advise student groups on final project implementations, including general programming help, MMIO concepts, and workarounds for hardware limitations of the Xilinx BASYS3 FPGA board.

Skills Developed: Technical communication, proficiency in RISC-V architecture and Assembly programming techniques.