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Lab 3

NMOS Die with ESD Protection

Introduction:

The goal for this lab is to have students design a die with basic ESD protection that allows connections to an NMOS transistor in the center. Figure 1 shows the general goal for the lab which is a die with a 8 pin connections, an NMOS transistor in the center, and diodes protecting each pin from ESD.

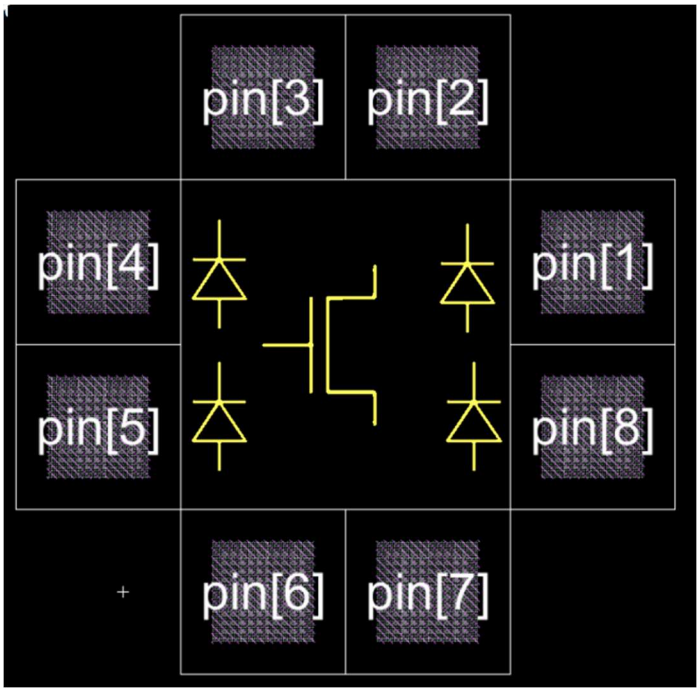

Figure 1: NMOS Die with ESD Protection

Methods and Materials:

The lab was completed by following the steps outlined by the "ENCE_3501_Lab_3.pdf" and "Lab_3_NMOS_ESD.pdf" handouts on the course Canvas page. In addition, the lab was built on top of the "lab_3_nmos_esd_template.jelib" template found on the course Canvas page. The template will be references as the "Lab 3 template" in this report. The software used for this lab was Electric VLSI and LTSpice.

Schematics:

ESD protection works but putting two diodes on a pin connection. One diode clamps positive voltage spikes to VDD, and the other clamps negative voltage spikes to ground. The first two foundational schematics of this lab are the pWell-nActive and pActive-nWell diodes (Figure 2 and Figure 3 respectively) which will be used for the ESD protection on the die. These schematics were provided by the Lab 3 template.

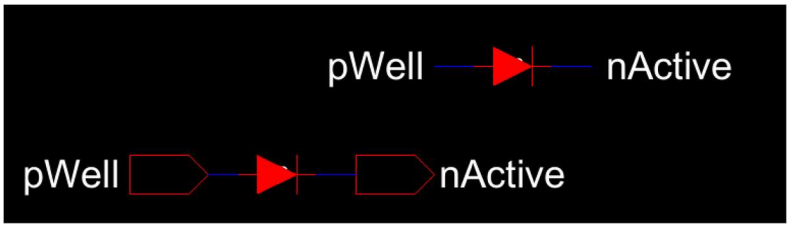

Figure 2: pWell-nActive Diode Schematic

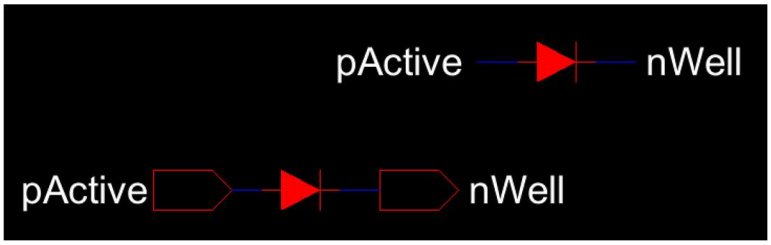

Figure 3: pActive-nWell Diode Schematic

Next, ESD protection is added to the pad cell. The pad cell was already designed in Lab 2 and explanations for the pad cell schematic can be seen in the respective report. The diodes are added to the pad cell connection such that there is a diode with the cathode to VDD and diode with the anode to GND (Figure 4). During normal voltage operation range (0-VDD), the VDD connection to the upper diode will prevent any current flowing up to VDD and the input voltage will not be enough to reverse bias the lower diode. If there is a positive ESD, the voltage on the input will be larger than VDD and the current will be shunted to VDD. If there is a negative ESD, the input voltage is significantly enough below GND, and current will be shunted to GND.

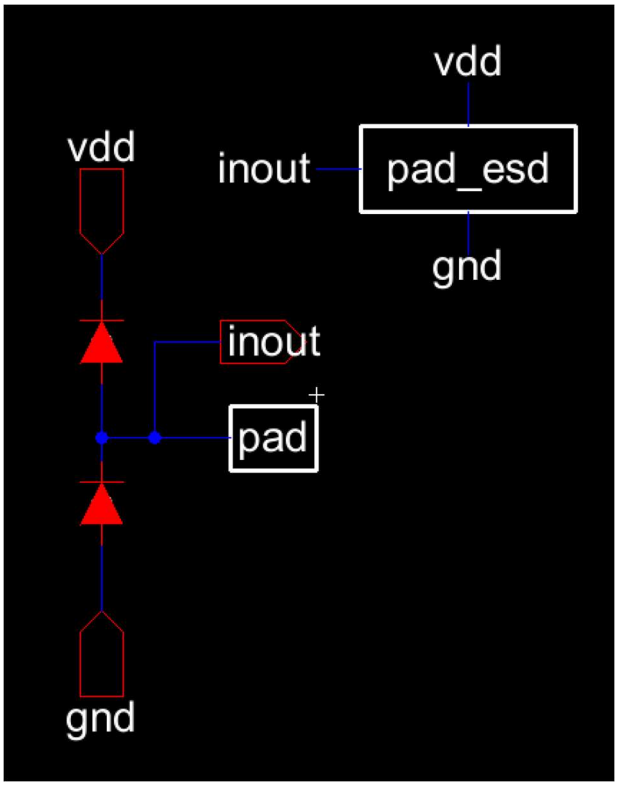

Figure 4: Pad Cell with ESD Protection Schematic

Now, each pad cell is incorporated into a pad frame with 8 pin connections, each on a bus (Figure 5). 8 pads allow for the die to be a square and will allow for each pin connection from the NMOS.

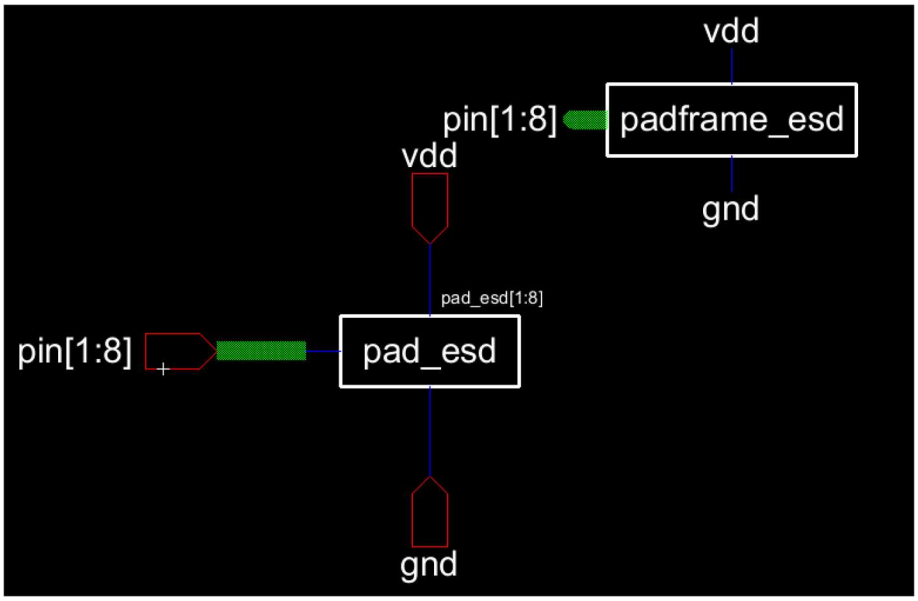

Figure 5: Padframe with ESD Protection Schematic

Next, the NMOS is added to the pad frame schematic (Figure 6). Each connection from the NMOS is given a pin connection to the pad frame.

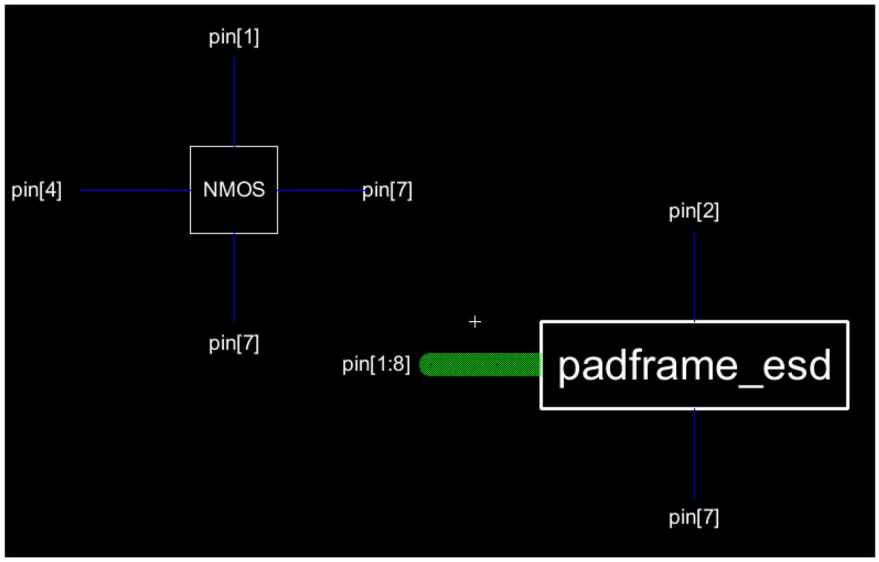

Figure 6: Padframe with ESD Protection and NMOS Schematic

Layouts:

The pWell-nActive and pActive-nWell diodes used for ESD protection are laid out in Figure 7 and Figure 8 respectively. They are made from pWell, nActive, pActive, and nWell metal 1 connections. These layouts were also provided in the Lab 3 template.

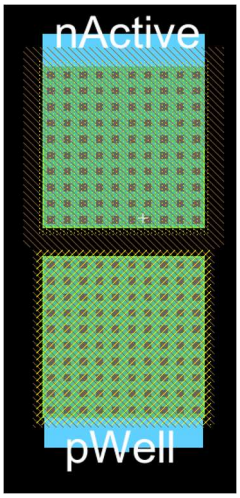

Figure 7: pWell-nActive Diode Layout

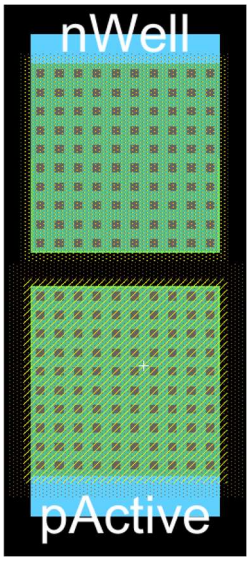

Figure 8: pActive-nWell Diode Layout

Next, the diodes are connected to the pad cell layout (Figure 9). The pad cell was laid out in Lab 2 and the necessary explanation to lay out the pad cell can be found in the respective report. The pWell-nActive diode is connected to a ground rail to prevent negative ESD from damaging the pad. The pActive-nWell diode is connected to VDD to prevent positive ESD from damaging the pad.

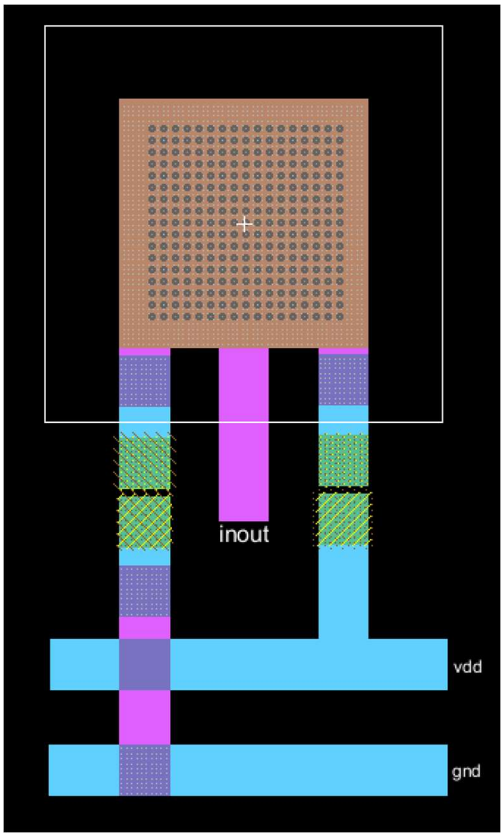

Figure 9: Pad Cell with ESD Protection Layout

Lastly, each pad cell is duplicated to create a pad frame with 8 pad cells, each having ESD protection (Figure 10). An NMOS layout was provided in the Lab 3 template which is placed in the center of the pad frame (Figure 10). Each connection from the NMOS is connected to the respective pad cell according to Figure 6.

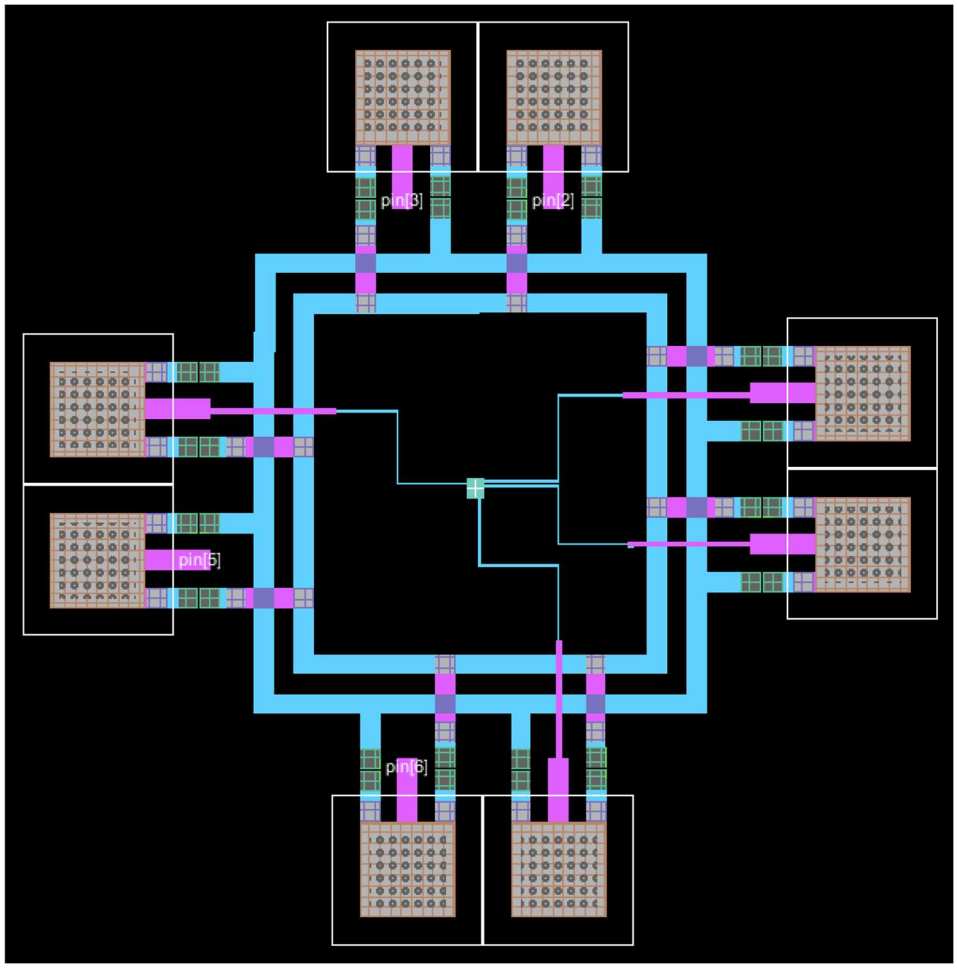

Figure 10: Padframe with ESD Protection and NMOS

The NMOS transistor die with basic ESD protection is now complete.

Conclusion:

In conclusion, students create a die that allows for connecting an NMOS transistor to the outside world, with ESD protection. Each pad cell has two diodes to prevent the die from damage from positive or negative ESD.