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Lab 4

Electric VLSI Inverter

Introduction:

The goal for this lab was to have students create schematics, layouts, and symbols for two inverters. The second inverter was to be made 4 times the width of the first. Once the inverters were created, students were to simulate the inverter's switching points and behaviors when driving a capacitor load.

Methods and Materials:

The lab was completed by following the steps outlined by the "ENCE_3501_Lab_4.pdf" and "Lab_4_Inverters.pdf" handouts on the course Canvas page. The software used for this lab was Electric VLSI and LTSpice.

Schematics:

First, students created the schematic for the first inverter (Inverter 1), seen in Figure 1. Students were guided by the lab handouts for the dimensions of the PMOS and NMOS.

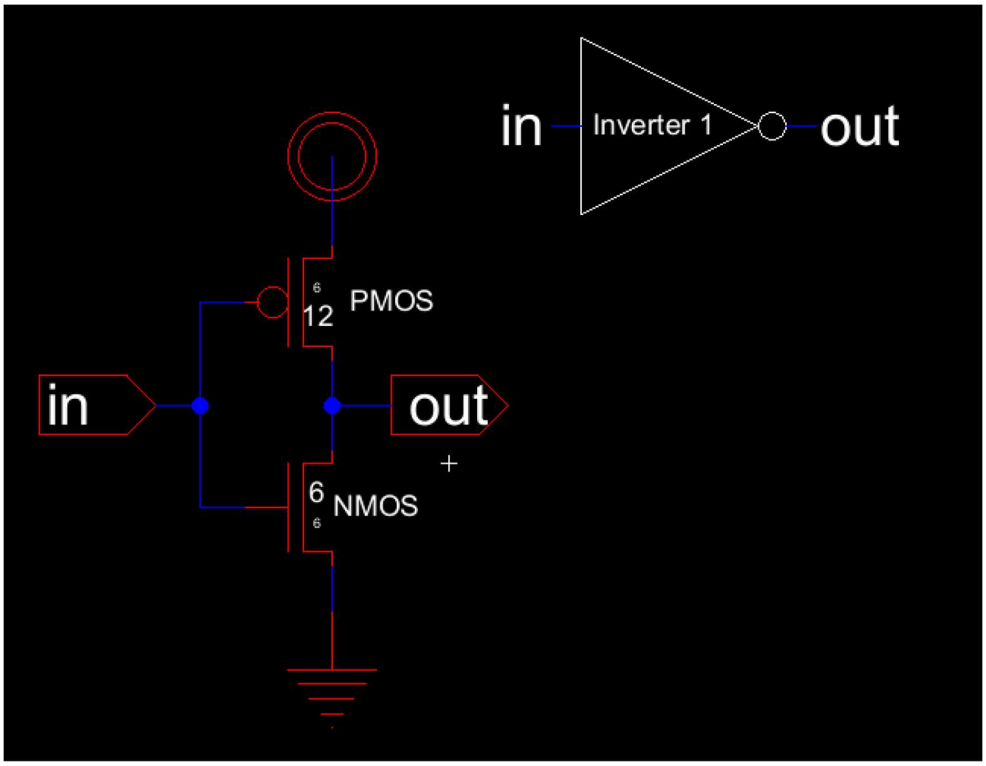

Figure 1: Inverter 1 Schematic

Next, the second inverter (Inverter 2) schematic was created, having a width of 4 times the first. Inverter 2's schematic is seen in Figure 2.

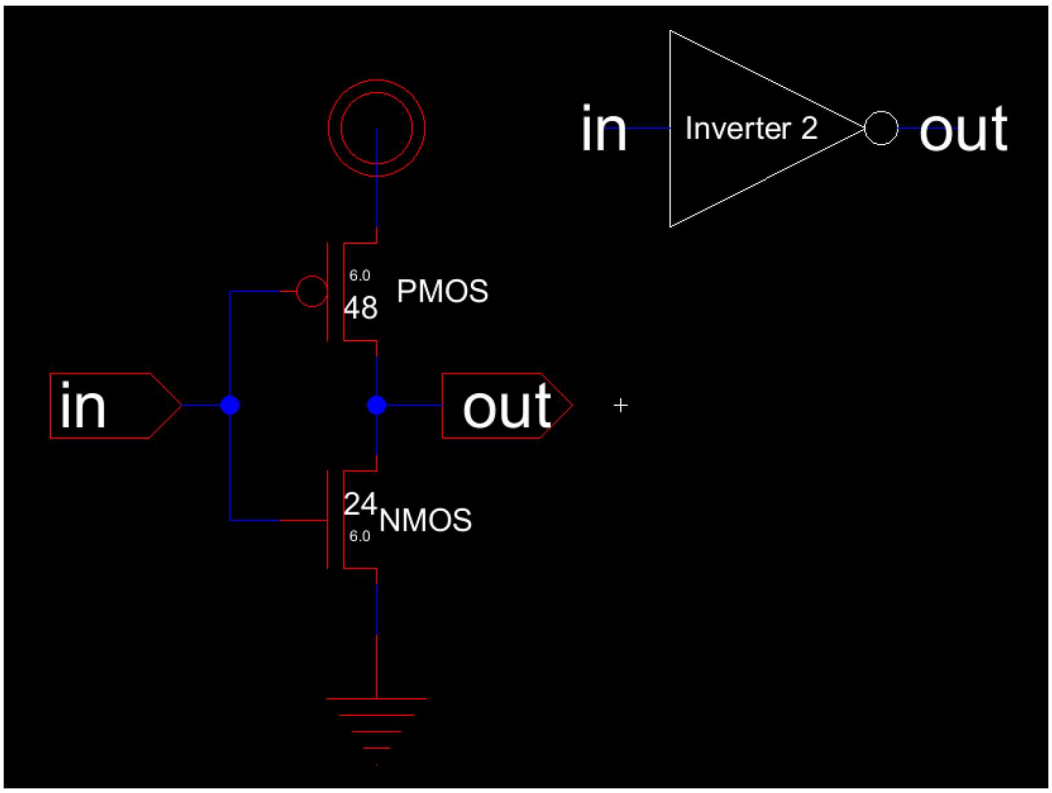

Figure 2: Inverter 2 Schematic

Now, both the switching points for Inverter 1 and 2 can be simulated using the schematic in Figure 3.

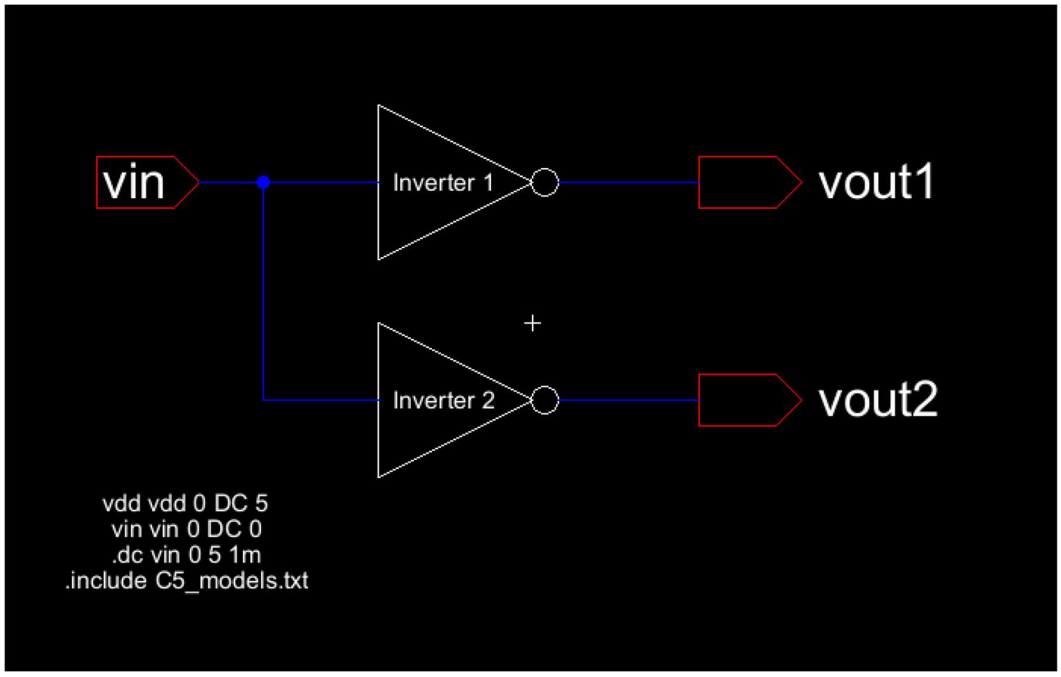

Figure 3: Inverter Switching Point Simulation Schematic

The results of both inverters switching points can be observed in Figure 4.

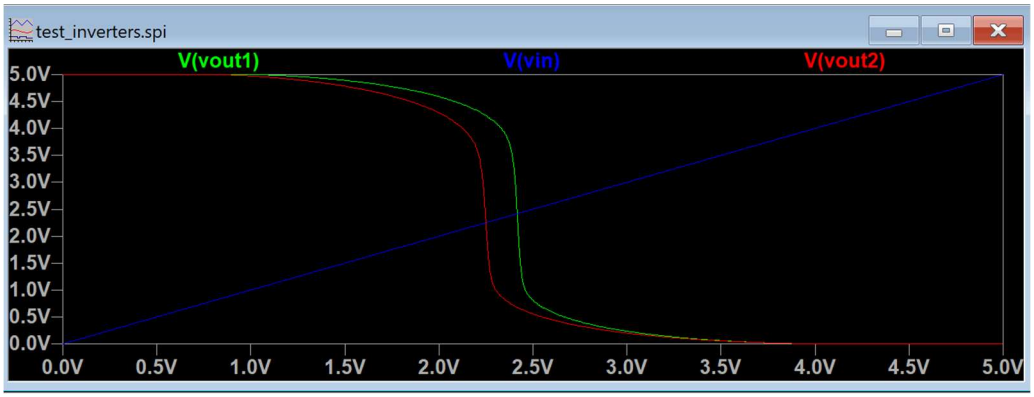

Figure 4: Inverter Switching Point Simulation Result

It can be observed that Inverter 1's switching point is slightly more desirable since the voltage curve from vout1 is just slightly more symmetrical than vout2. In general, both inverter's switching points are acceptable.

Next, the behavior of the inverters when driving a capacitor load is simulated using the schematic in Figure 5. The capacitors are given the values 100fF, 1pF, 10pF, and 100pF.

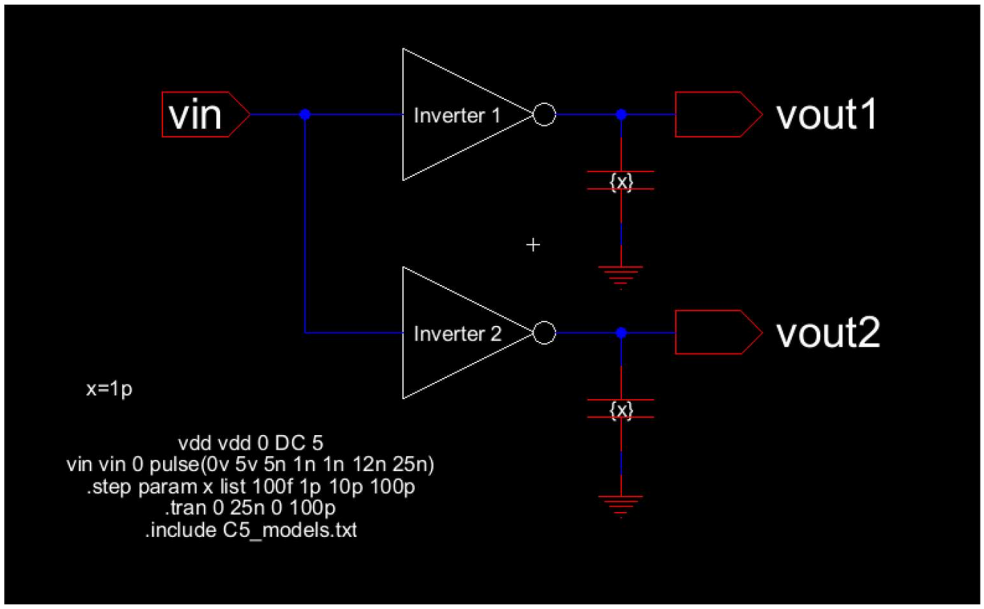

Figure 5: Inverters Driving Capacitor Loads Simulation Schematic

The results of Figure 5 for Inverter 1 and Inverter 2 are seen below in Figure 6 and Figure 7, respectively.

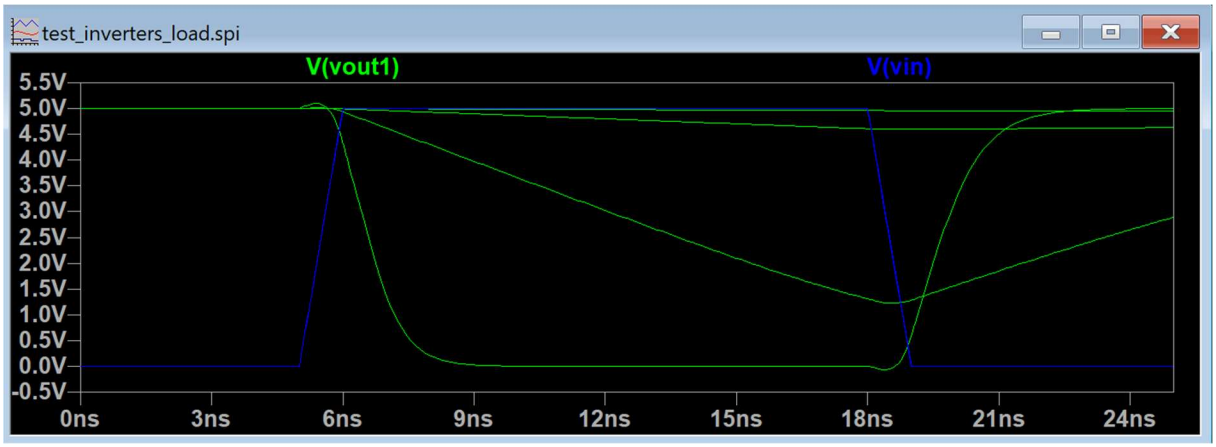

Figure 6: Inverter 1 Driving Capacitor Loads Simulation Schematic Results

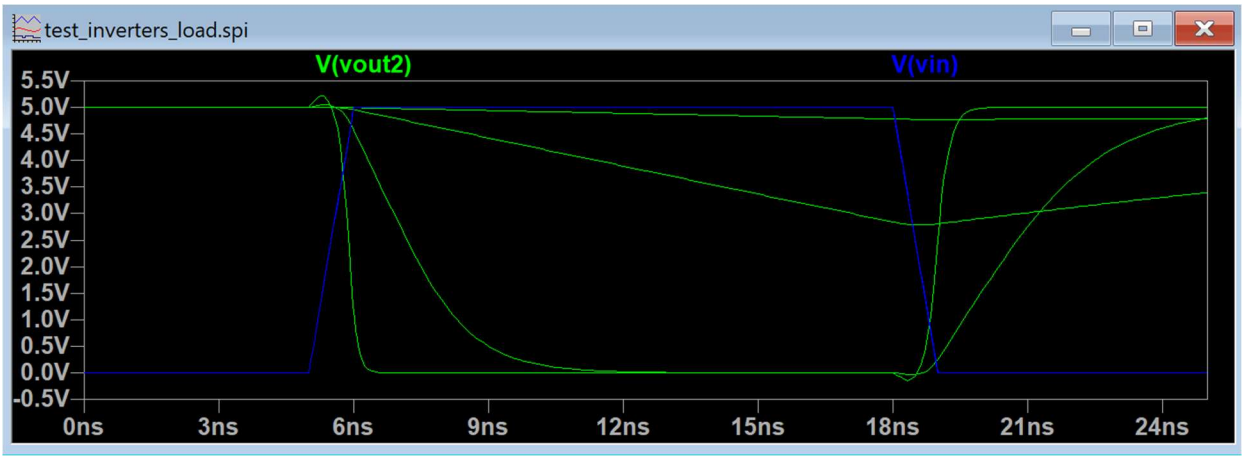

Figure 7: Inverter 2 Driving Capacitor Loads Simulation Schematic Results

It can be observed from the results that when the inverter is driving a capacitor, there is a delay in the output of the inverter. For all but one capacitor value in Figure 6, vout never fully reaches 0V for the time the input is 5V which means the inverter is so delayed that it is not functional. For one capacitor value (likely 100pF), the delay is so large that vout isn't even effected by vin. It can be assumed that the larger a capacitor value, the larger the delay will be since it holds more charge and cannot discharge in time for vout to get to zero. When comparing Inverter 1 to Inverter 2, Inverter 2 is less impacted by the delays from the capacitors. This is because Inverter 2 can discharge current more effectively with the extra transistor width.

Layouts:

The layout for Inverter 1 is seen in Figure 8. The power is coming from the top of the cell via Metal 1 and the ground is running from the bottom of the cell also via Metal 1. The PMOS and NMOS dimensions match those seen in Figure 1.

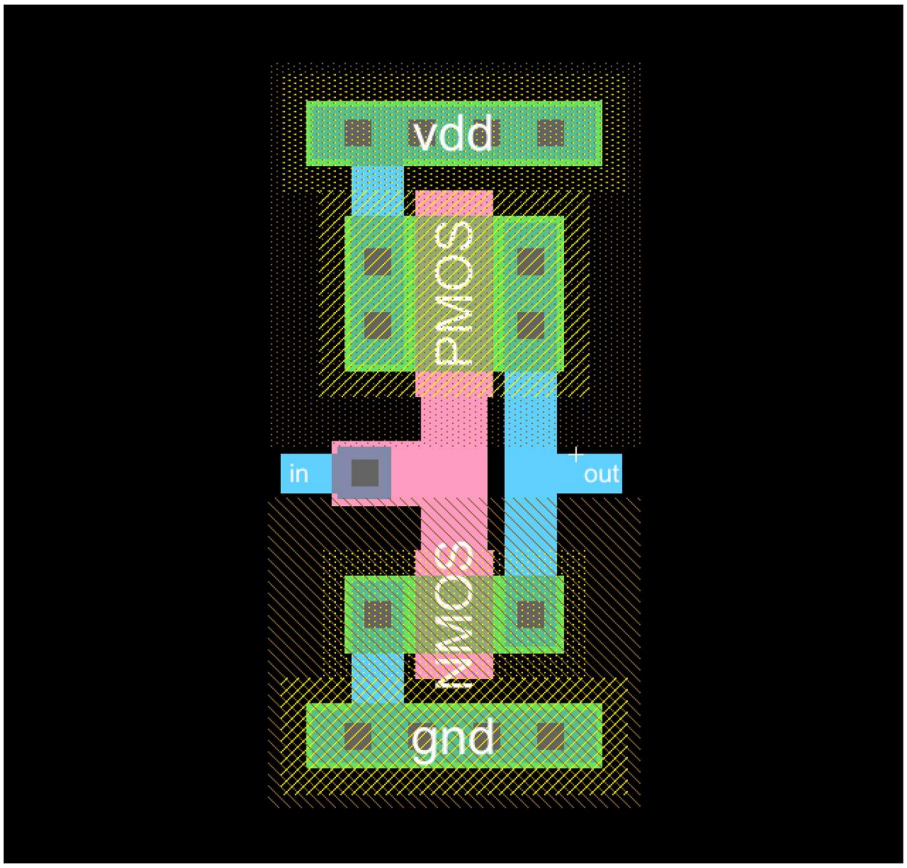

Figure 8: Inverter 1 Layout

The layout for Inverter 2 is seen in Figure 9. It is essentially the same as Inverter 1's layout, but it has a device multiplier of 4. It can easily be seen how the device multiplier of 4 means there are 4 PMOS and 4 NMOS, individually the same size as Figure 1's transistors, but when combined, create the size of the transistors in Figure 2. Each PMOS and NMOS are sharing drain and source connections to make the layout compact.

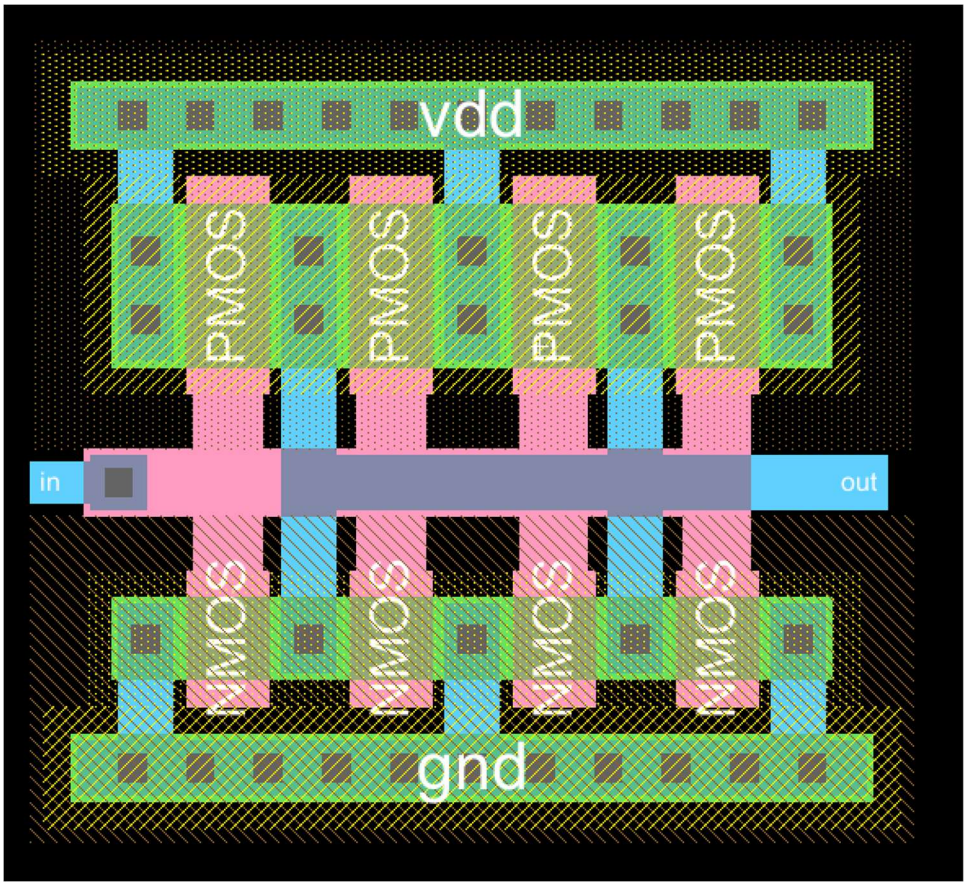

Figure 9: Inverter 2 Layout

Conclusion:

In conclusion, students created schematics, layouts, and symbols for two inverters. One inverter was 4 times as wide as the other. The inverters were simulated to observe switching points, which each sufficed. The inverters were also simulated when driving a capacitor load and it was observed that a capacitor load creates a delay in the inverter's output. In some cases, the delay was so significant that the inverter's output doesn't change in response to quick input pulses. It can also be noted that wider transistors are more resilient to capacitor caused delays.