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Lab 1

Electric VLSI DAC

Introduction:

The aim of this lab is to create a 5- Bit DAC (Figure 1) using Electric VLSI. Students are expected to create schematics and layouts for their DAC and verify the functionality using SPICE simulations. DACs are critical circuits that take discrete inputs and convert them into continuous or analog outputs.

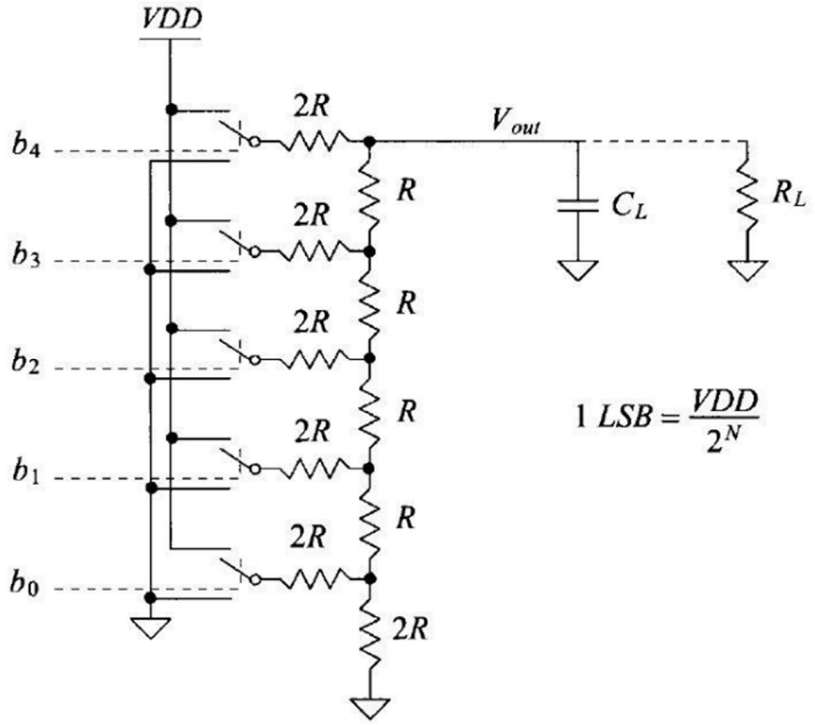

Figure 1: Voltage-mode (5-bit) DAC without an op-amp

Methods and Materials:

The lab was completed by following the steps outlined by the “ENCE_3501_Lab_1.pdf” and “Lab_1_DAC.pdf” handouts on the course Canvas page. The software used for this lab was Electric VLSI and LTSpice.

Schematics and Layouts:

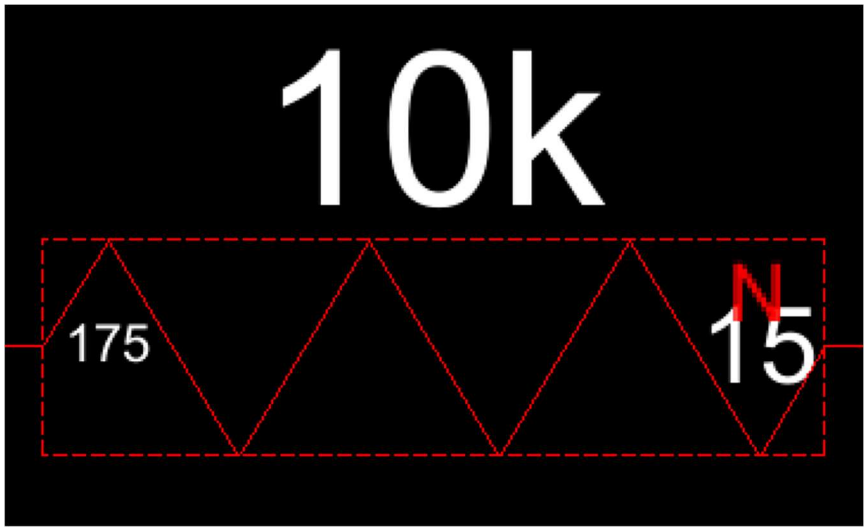

Figure 2: 10k N-well Resistor Schematic

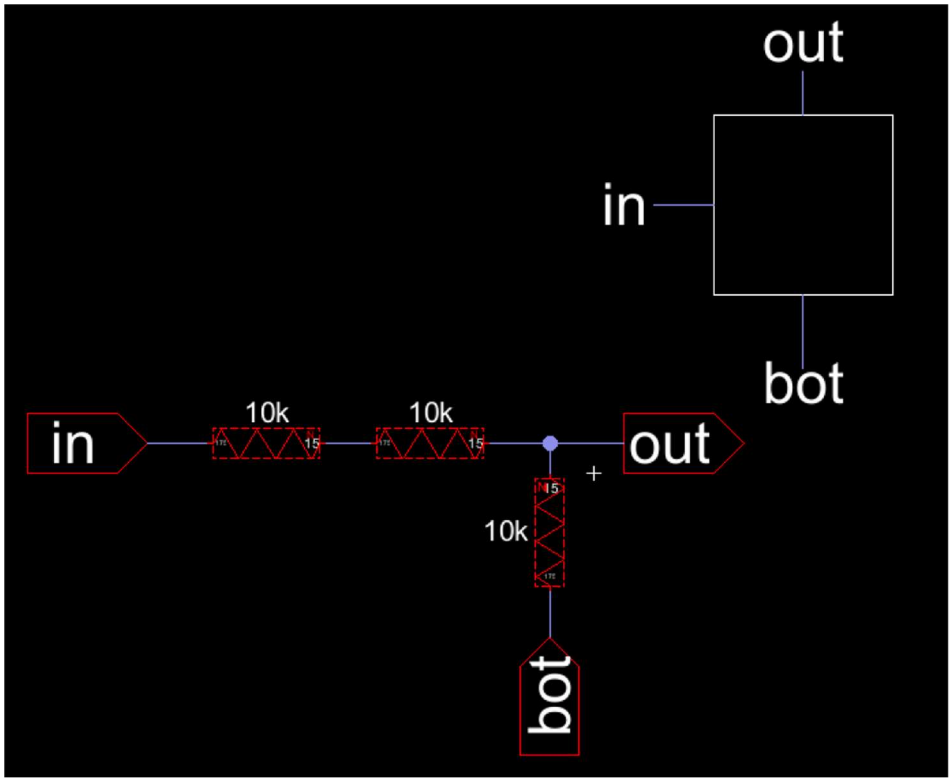

Figure 3: R Divider Schematic

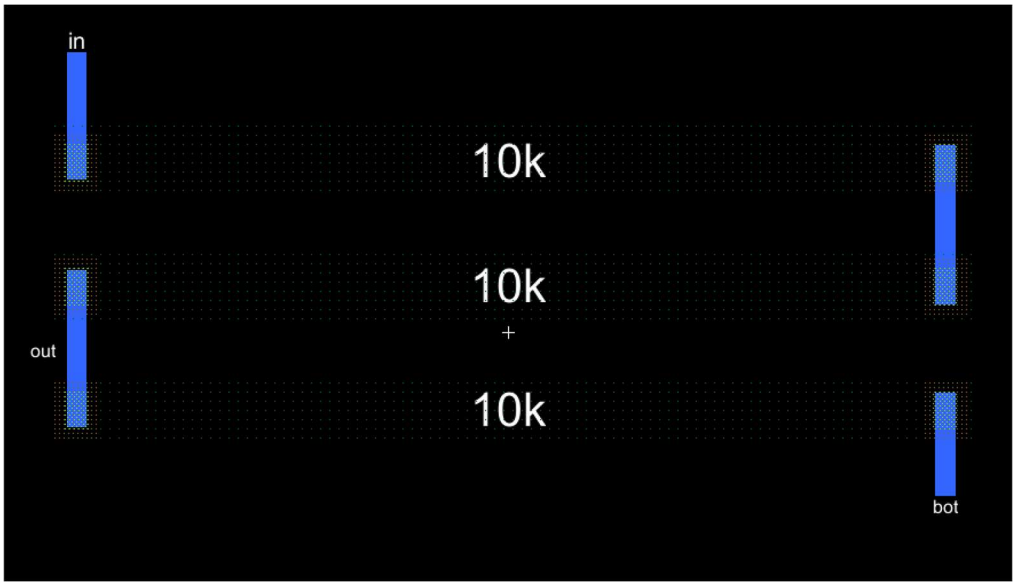

Figure 4: R Divider Layout

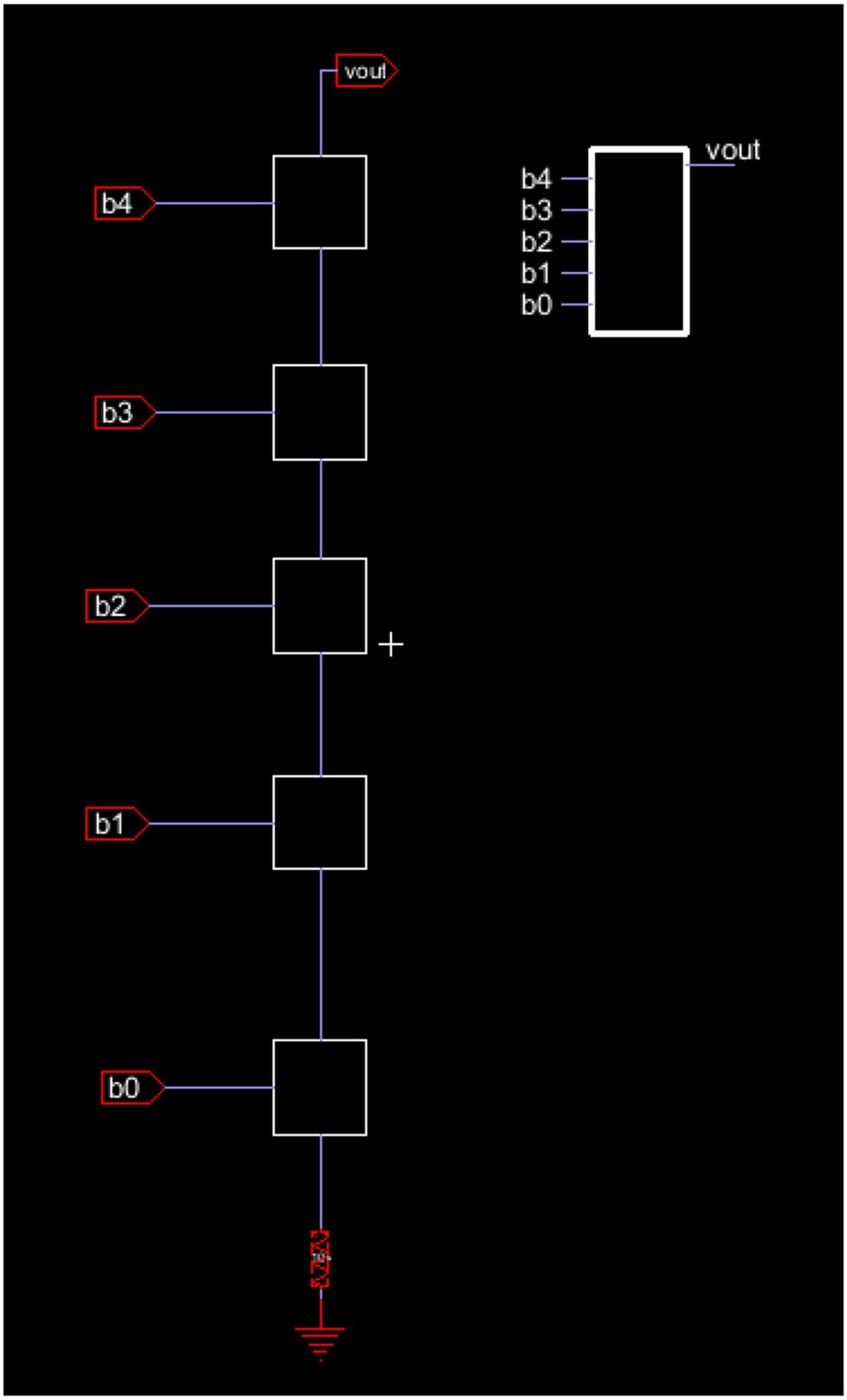

Figure 5: 5-bit DAC Schematic

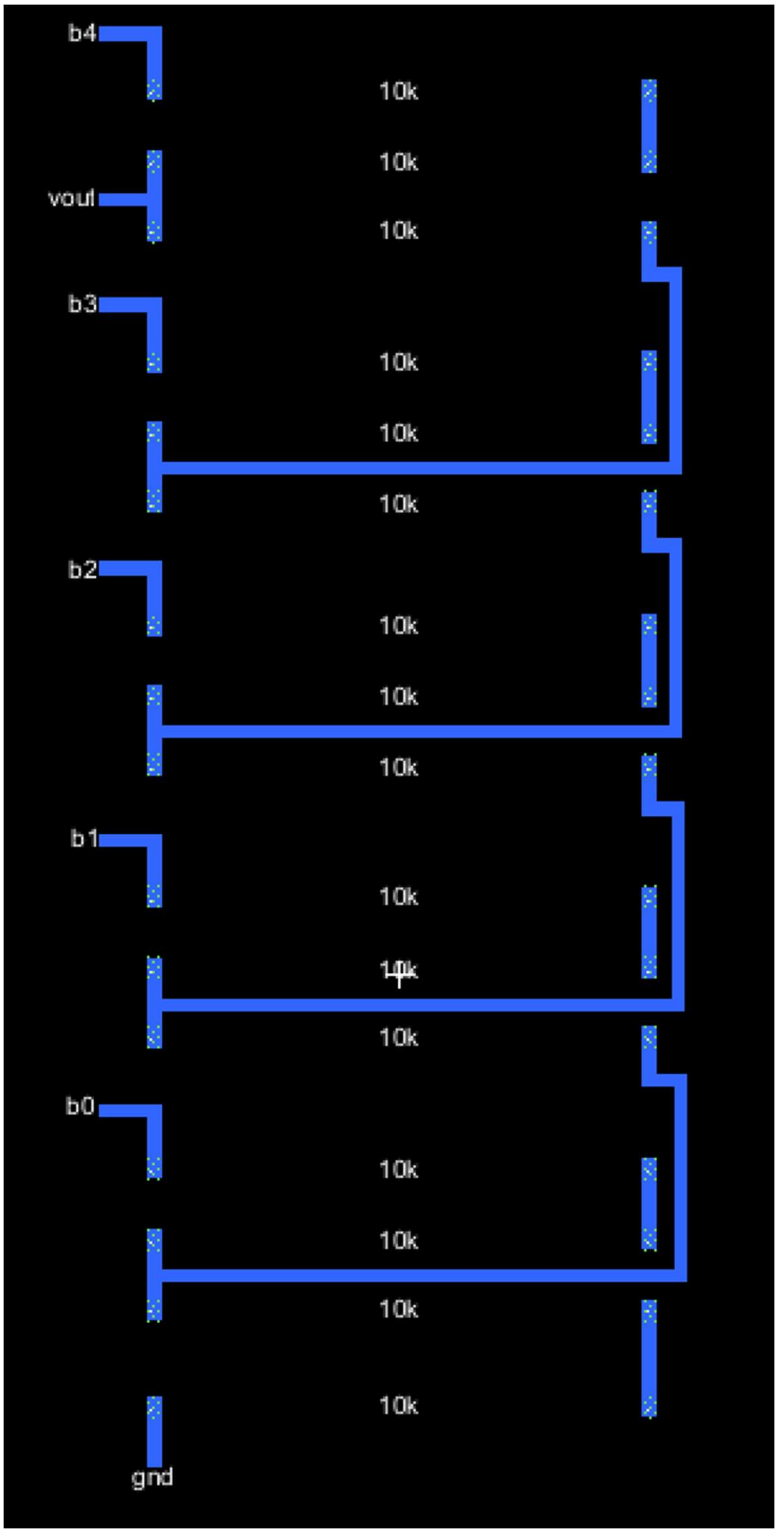

Figure 6: 5-Bit DAC Layout

Discussion and Hand Calculations:

***NOTE:** For the ease of grading, all questions from "Lab 1 – Directions" are answered in this section in order that they appear on the handout with the exception of the resistor dimension calculation since it's a foundational component for the layouts and schematics.

The resistance dimensions in Figure 2 are derived in the steps below.

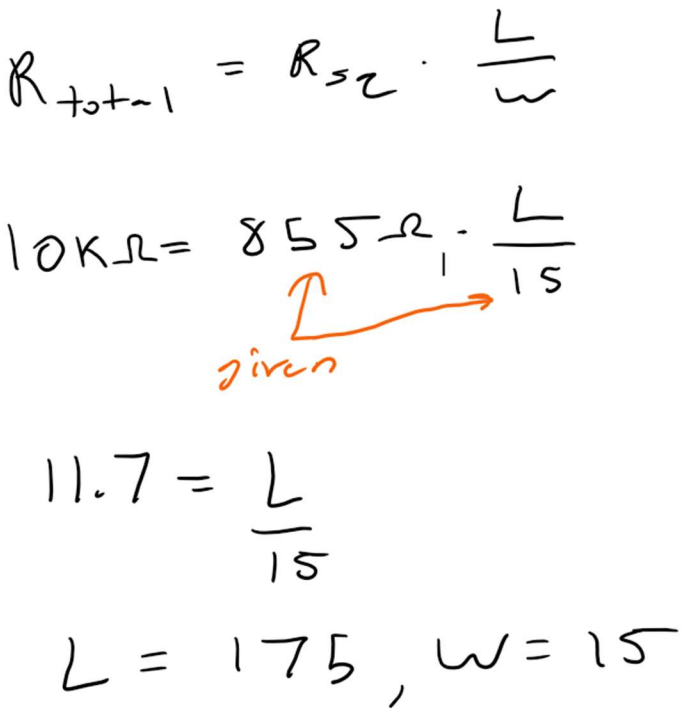

Figure 7: 10k N-Well Resistor Dimensions Hand Calculation

To determine the output resistance of the 5-Bit DAC (Figure 1), the Thevenin equivalence can be analyzed. Below are the chronological hand calculations necessary to determine the Thevenin equivalence and the output resistance.

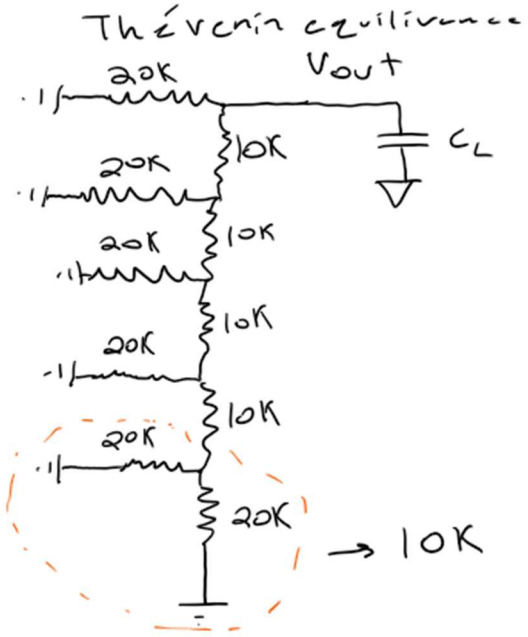

Figure 8: Step 1 of Output RHand Calculation

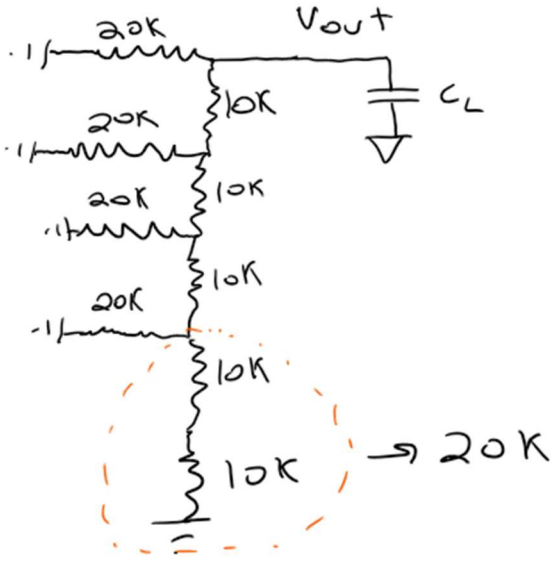

Figure 9: Step 2 of Output R Hand Calculation

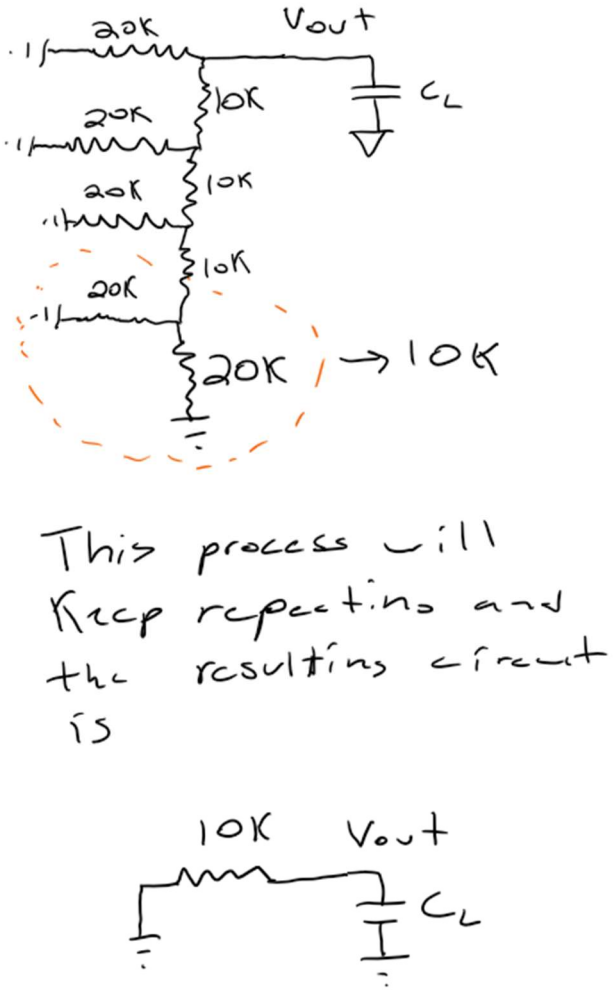

Figure 10: Step 3 of Output R Hand Calculation

From Figure 10, the output resistance of the 5-Bit DAC will be 10k ohms. To calculate the delay of the 5-Bit DAC, the following steps are taken. Note that the R value of 10k ohms comes from Figure 10 which concludes the output resistance is 10k ohms.

$$t_d = .7\,R \cdot C$$

$$t_d = .7 \cdot 10K\Omega \cdot 10pF$$

$$t_d = .7 \cdot 10 \cdot 10^{3}\,\Omega \cdot 10 \cdot 10^{-12}\,F$$

$$t_d = .7 \cdot 100 \cdot 10^{-9}\,s$$

$$t_d = 70 \cdot 10^{-9}\,s$$

$$t_d = 70ns$$

Figure 11: Time Delay Hand Calculation

A simulation is utilized to verify the hand calculations.

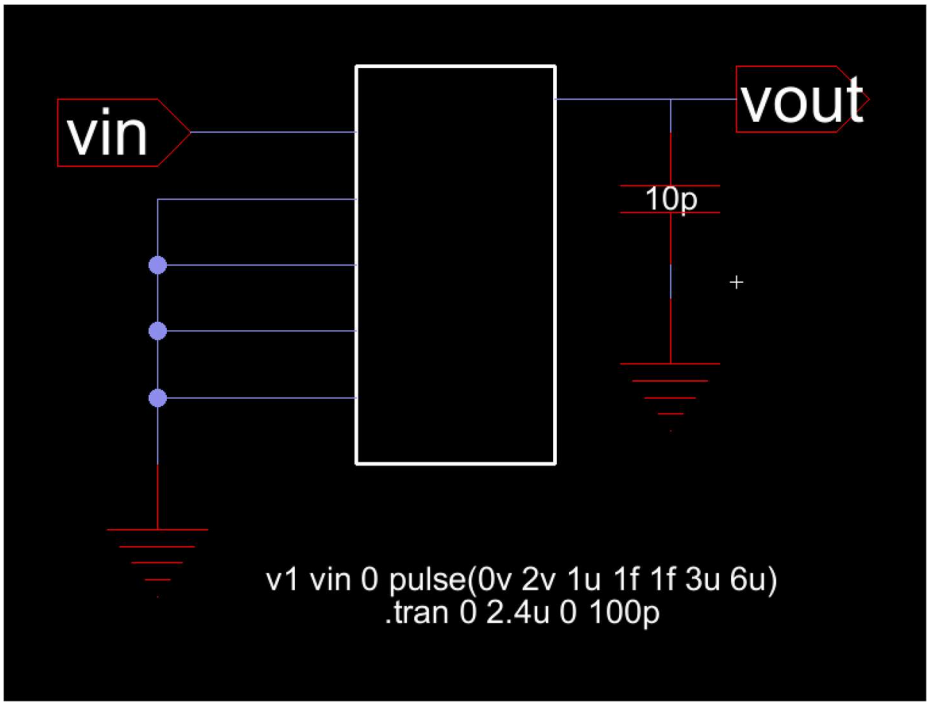

Figure 12: Time Delay Simulation Schematic

Figure 13: Time Delay Simulation Results

Figure 14 verifies that the delay of the 5-Bit DAC will be 70ns. It is also important to verify that the 5-Bit DAC works with test voltage. The simulation used to verify the 5-Bit DAC is using an input of 5V.

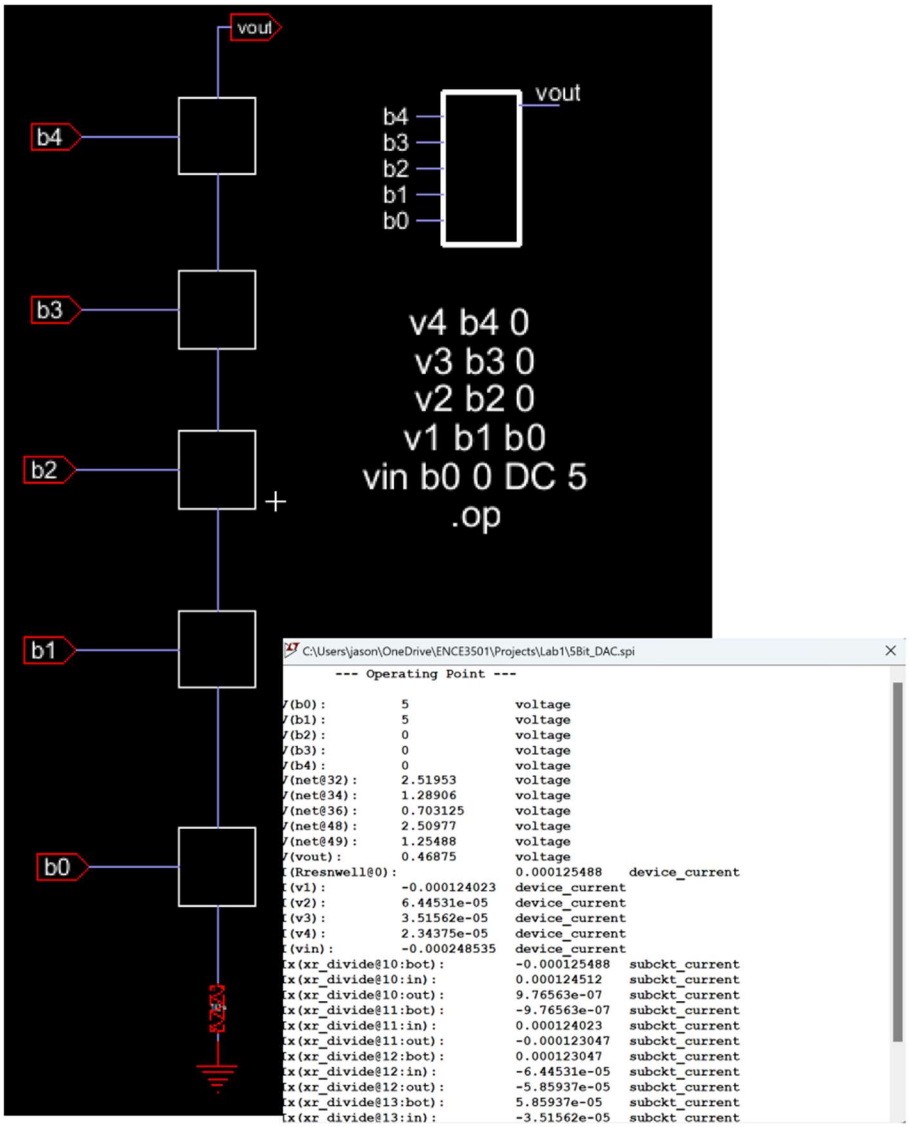

Figure 14: 5-Bit DAC Simulation Result

The result of the simulation is Vout = .46875V. This value exactly matches the Vout from Dr. Martins simulation in the lab handout. If the DAC drives a 10k ohm load, there will be a voltage divider on the output and therefore the output voltage will be halved.

DRC and LVS:

Below are the successfully DRC and LVS results for each component of the library.

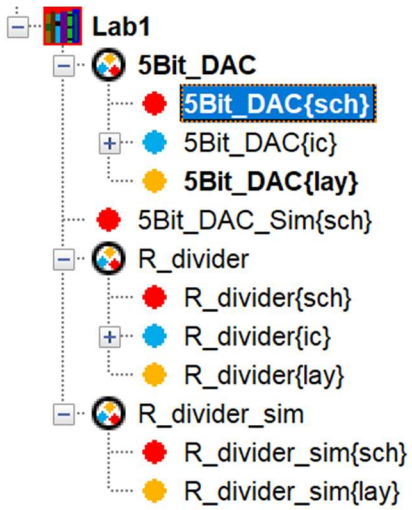

Figure 15: Lab 1 Library Structure

```
Checking schematic cell 'R_divider{sch}'
   No errors found
Checking schematic cell '5Bit_DAC{sch}'
   No errors found
Checking schematic cell '5Bit_DAC_Sim{sch}'
   No errors found
Checking icon cell 'R_divider{ic}'
   No errors found
Checking icon cell '5Bit_DAC{ic}'
   No errors found
0 errors and 0 warnings found (took 0.001 secs)
```

Figure 16: DRC 1

```
Checking schematic cell 'R_divider{sch}'
   No errors found
Checking schematic cell 'R_divider_sim{sch}'
   No errors found
Checking icon cell 'R_divider{ic}'
   No errors found
0 errors and 0 warnings found (took 0.001 secs)
```

Figure 17: DRC 2

```
Running DRC with area bit off, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 13 networks
Checking cell '5Bit_DAC{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.028 secs)
```

Figure 18: DRC 3

```
Hierarchical NCC every cell in the design: cell '5Bit_DAC{sch}'  cell '5Bit_DAC{lay}'
Comparing: Lab1:R_divider{sch} with: Lab1:R_divider{lay}
  exports match, topologies match, sizes not checked in 0.033 seconds.
Comparing: Lab1:5Bit_DAC{sch} with: Lab1:5Bit_DAC{lay}
  exports match, topologies match, sizes not checked in 0.005 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.047 seconds.
```

Figure 19: LVS

All components pass DRC and LVS.

Conclusion:

In this lab, students designed, implemented, and simulated a 5-Bit DAC in Electric VLSI. Students demonstrated the functionality of their DAC and analyzed the circuits' performance. All in all, this lab ensures students have the foundational skills to work in Electric VLSI.