

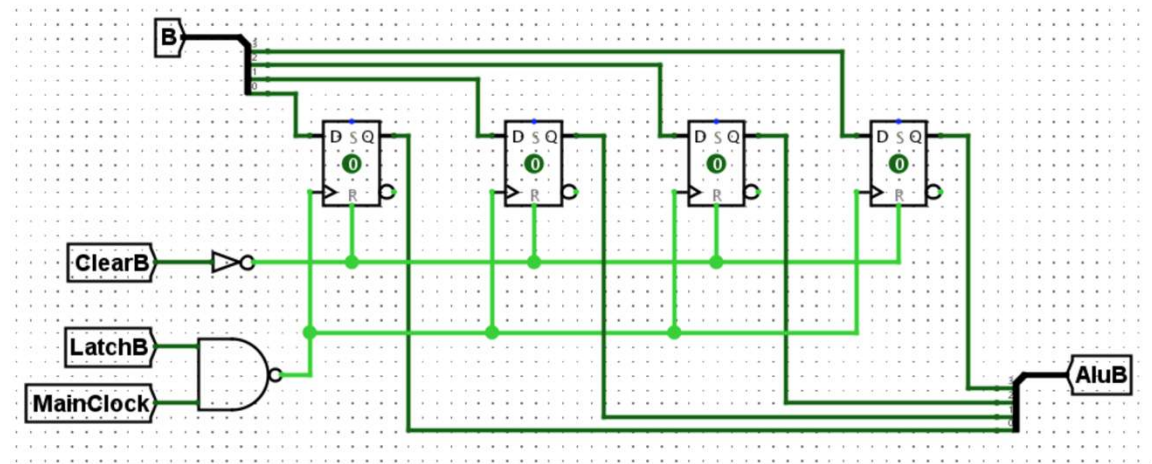
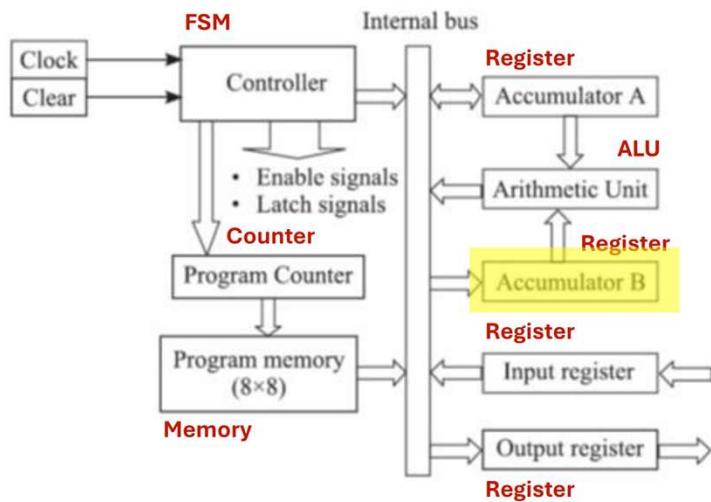
Accumulator B for a Very Simple Microprocessor

Jeremy Trafas

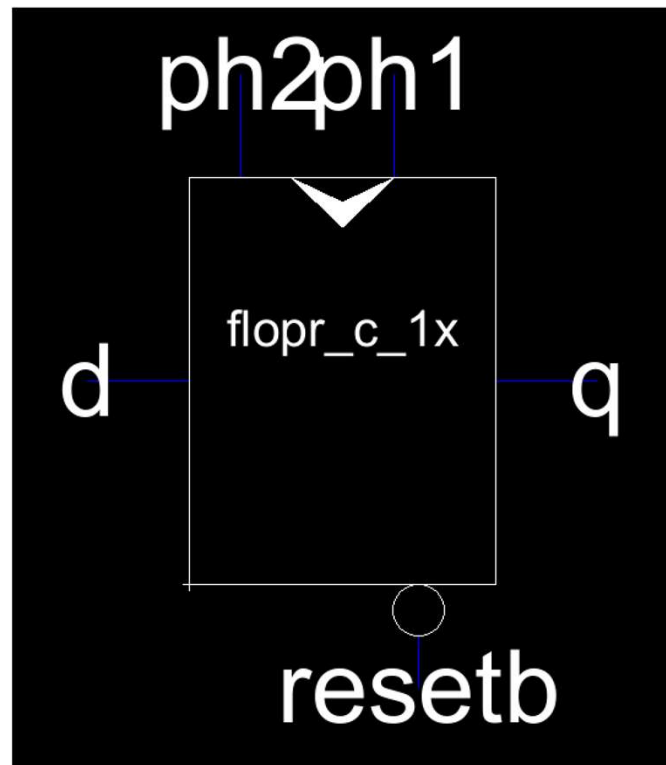
Accumulator B

Necessary Components

- D Flip-flops
- NAND
- Inverter



Design Challenge 1: What is ph1 and ph2?



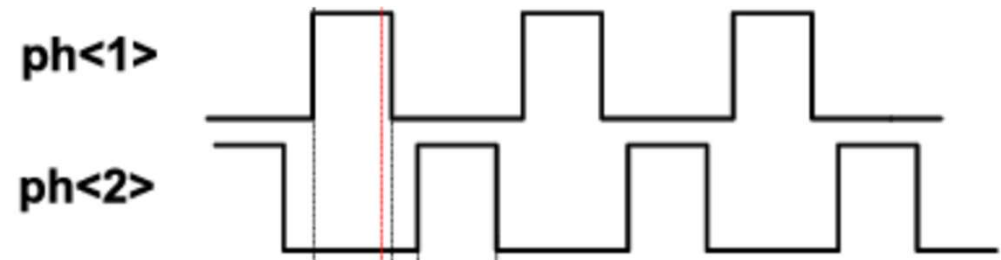
Let's Ask Gemini

How a Two-Phase Clock Works

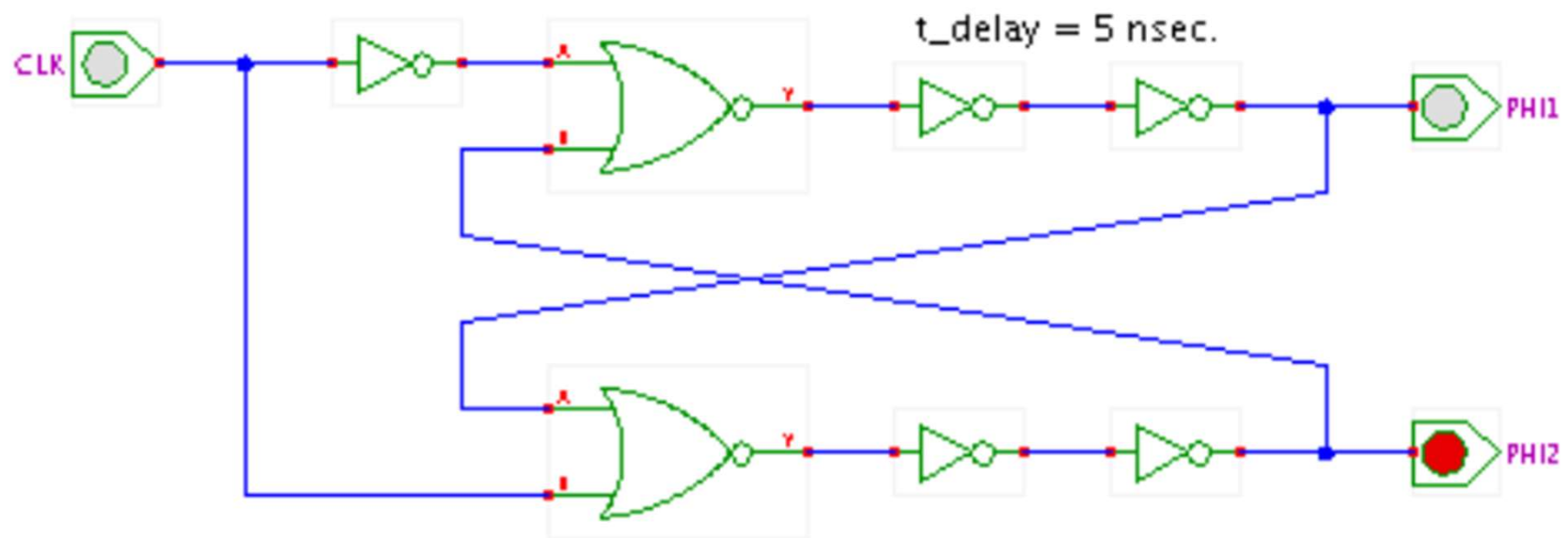
This type of flip-flop is typically a master-slave design:

1. **When `ph1` is high:** The "master" latch accepts the value from the `d` input.
2. **When `ph1` goes low:** The "master" latch holds the value.
3. **When `ph2` is high:** The "slave" latch accepts the value *from the master latch* and outputs it to `q`.
4. **When `ph2` goes low:** The "slave" latch holds the value, and the output `q` is stable.

The key is that `ph1` and `ph2` must have a **non-overlap** period (where both are low) to ensure the master latch closes before the slave latch opens.

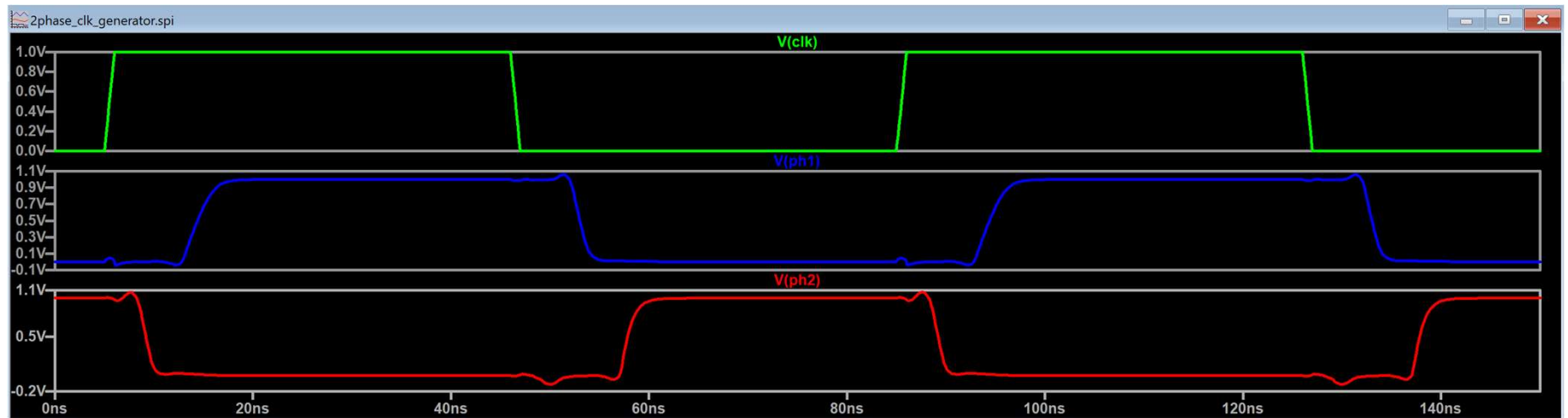
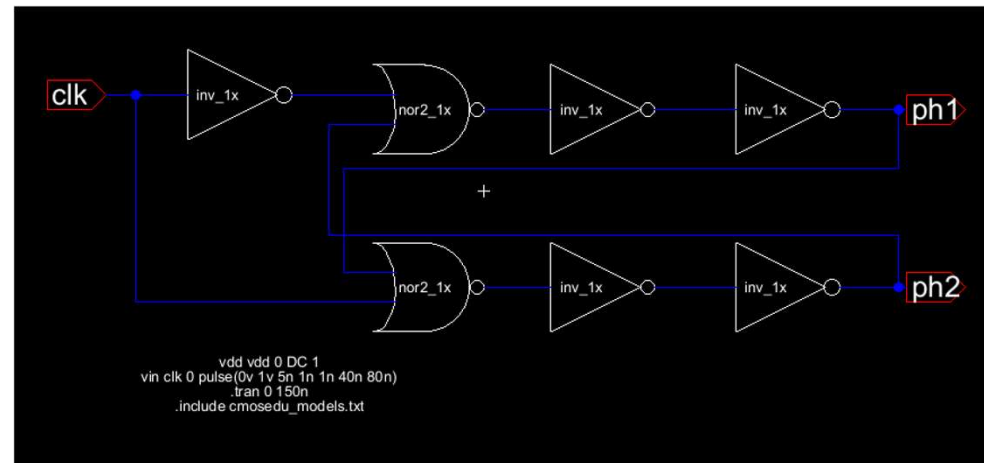


Two-Phase Clock Generator Circuit



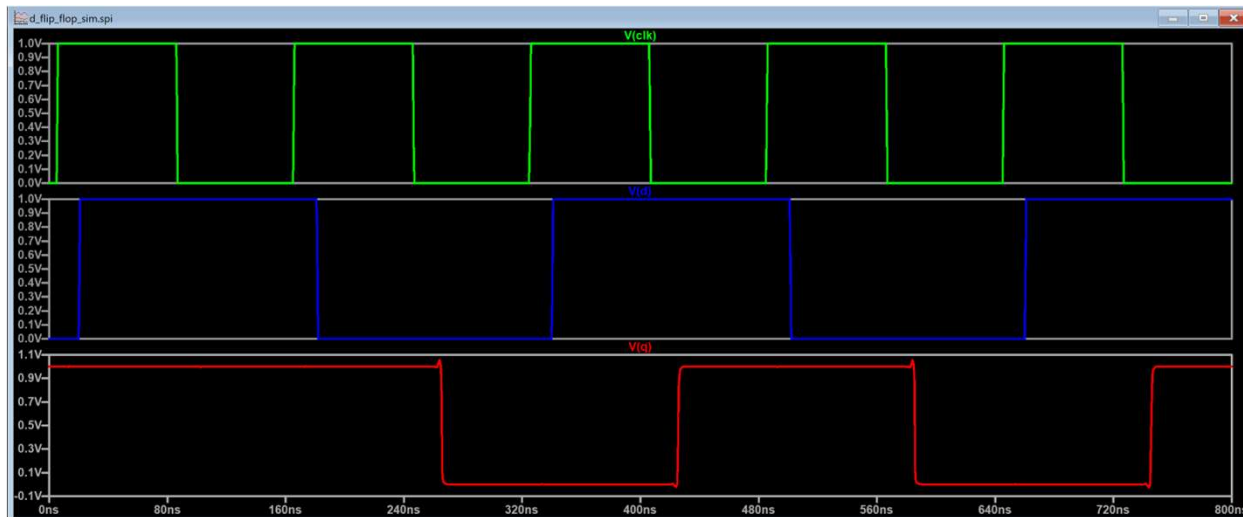
Two-phase Clock Generator

Two-Phase Clock Generator Schematic and Simulation

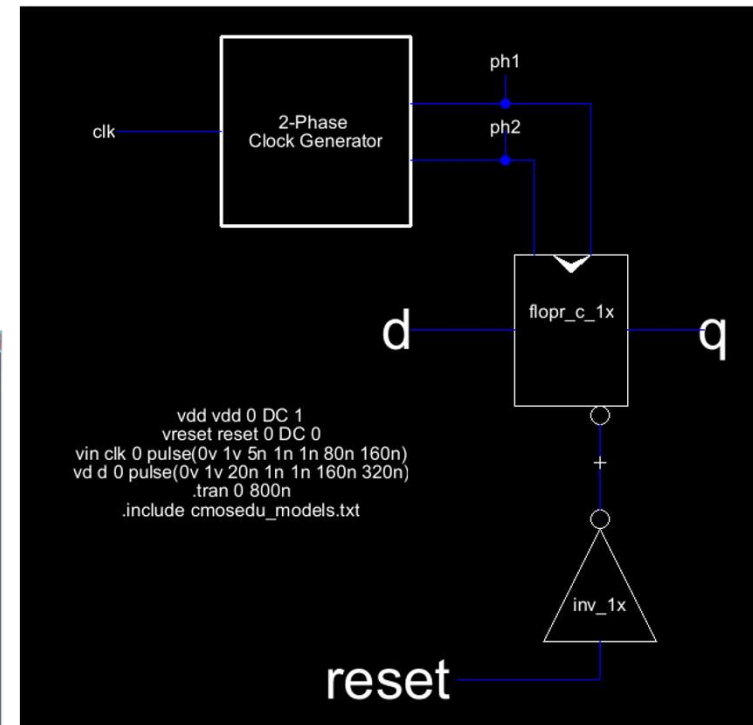


Inverted and non-overlapping!

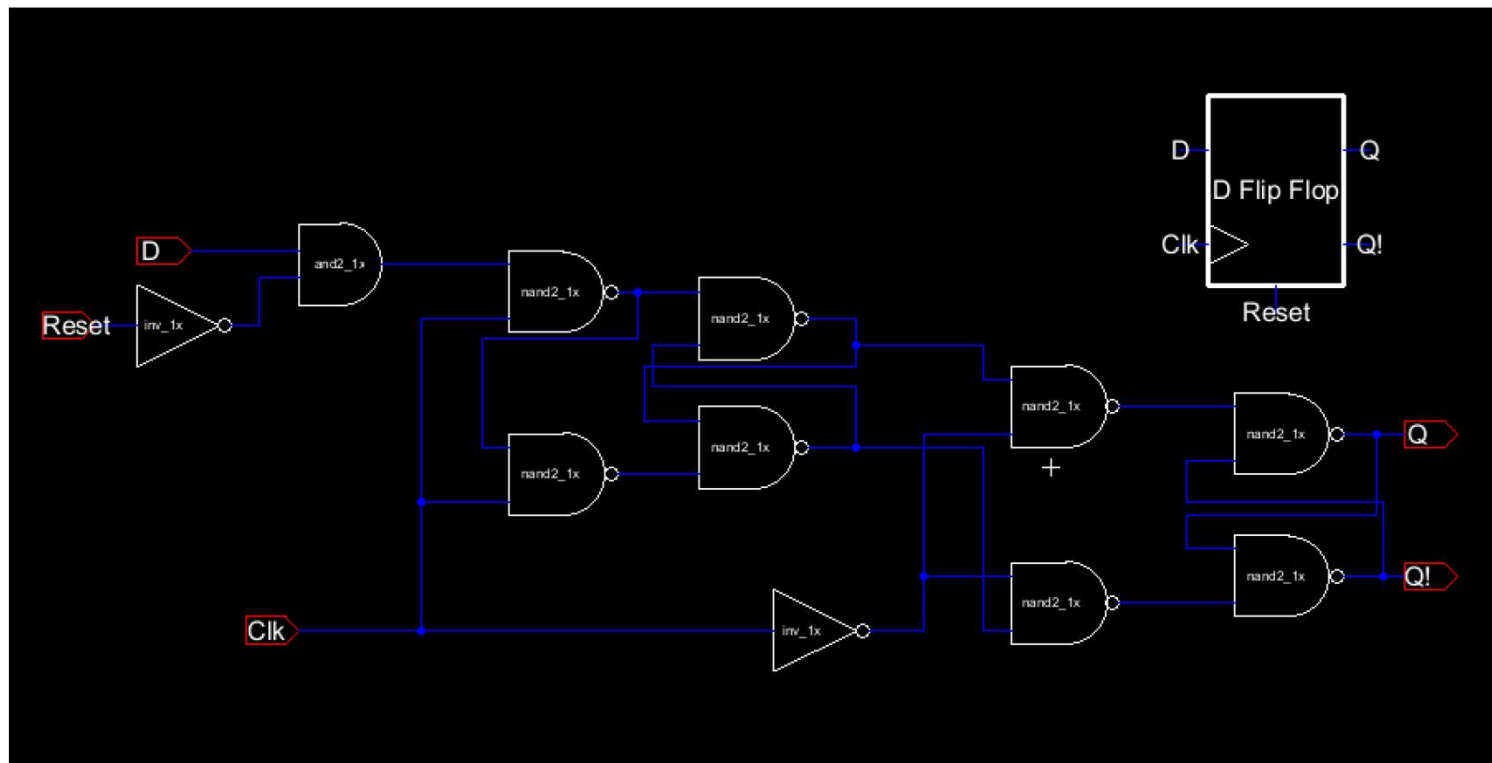
Testing D Flip-flop



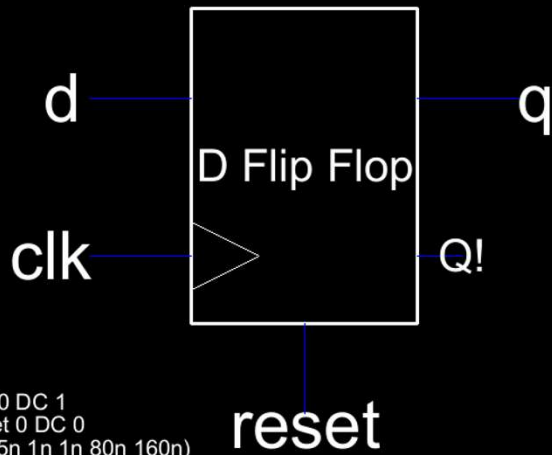
Negative edge, I gave up



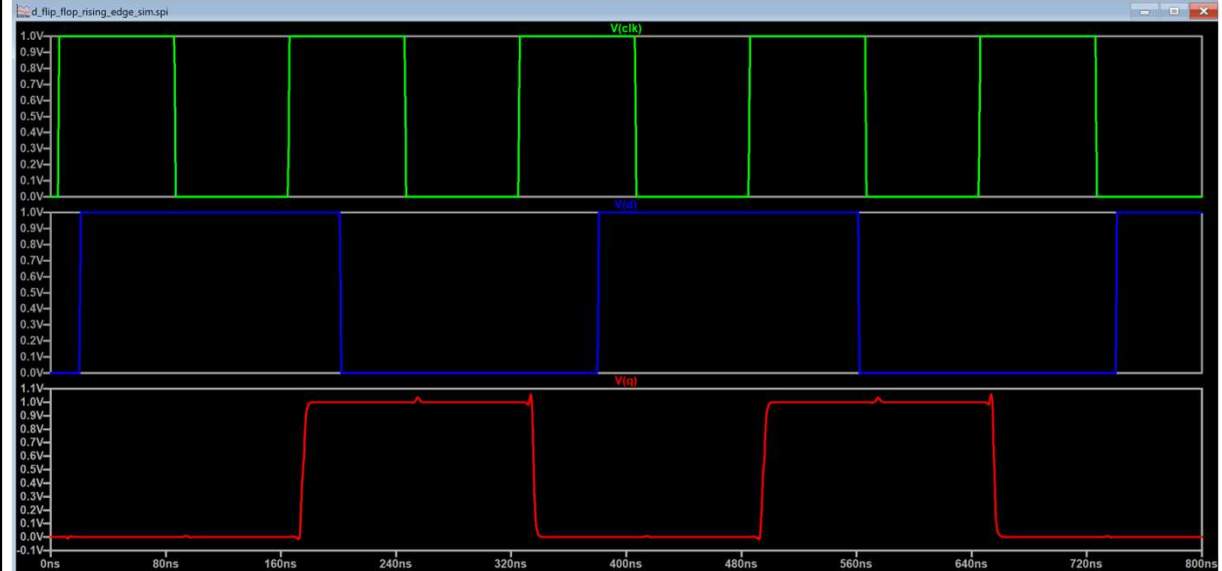
Making my own D Flip-flop



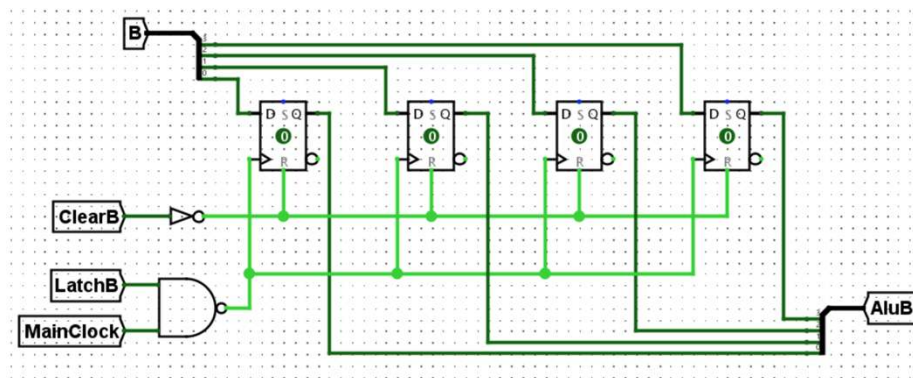
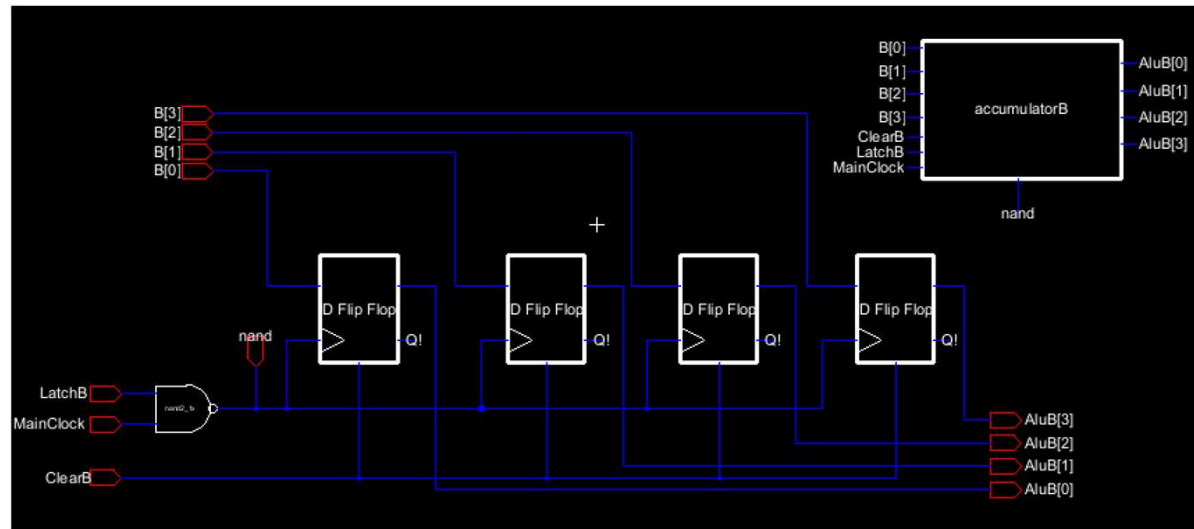
Making my own D Flip-flop



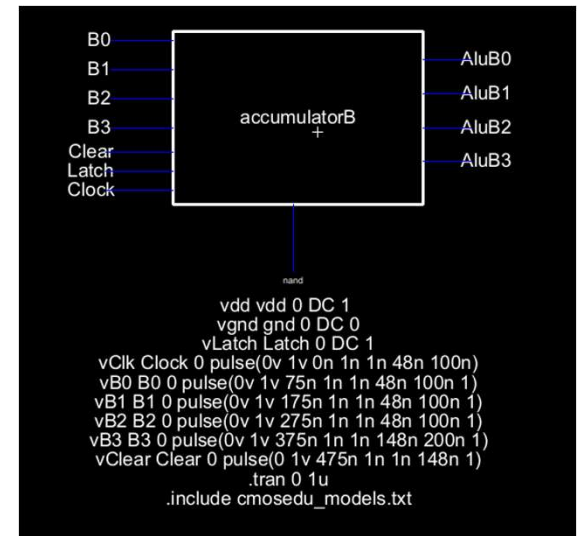
```
vdd vdd 0 DC 1
vreset reset 0 DC 0
vin clk 0 pulse(0v 1v 5n 1n 1n 80n 160n)
vd d 0 pulse(0v 1v 20n 1n 1n 180n 360n)
.tran 0 800n
.include cmosedu_models.txt
```



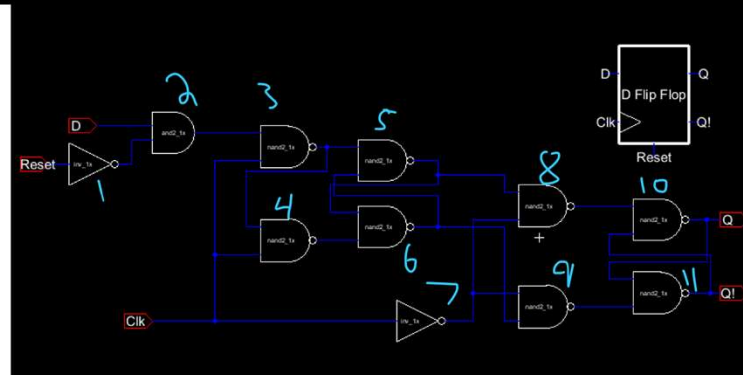
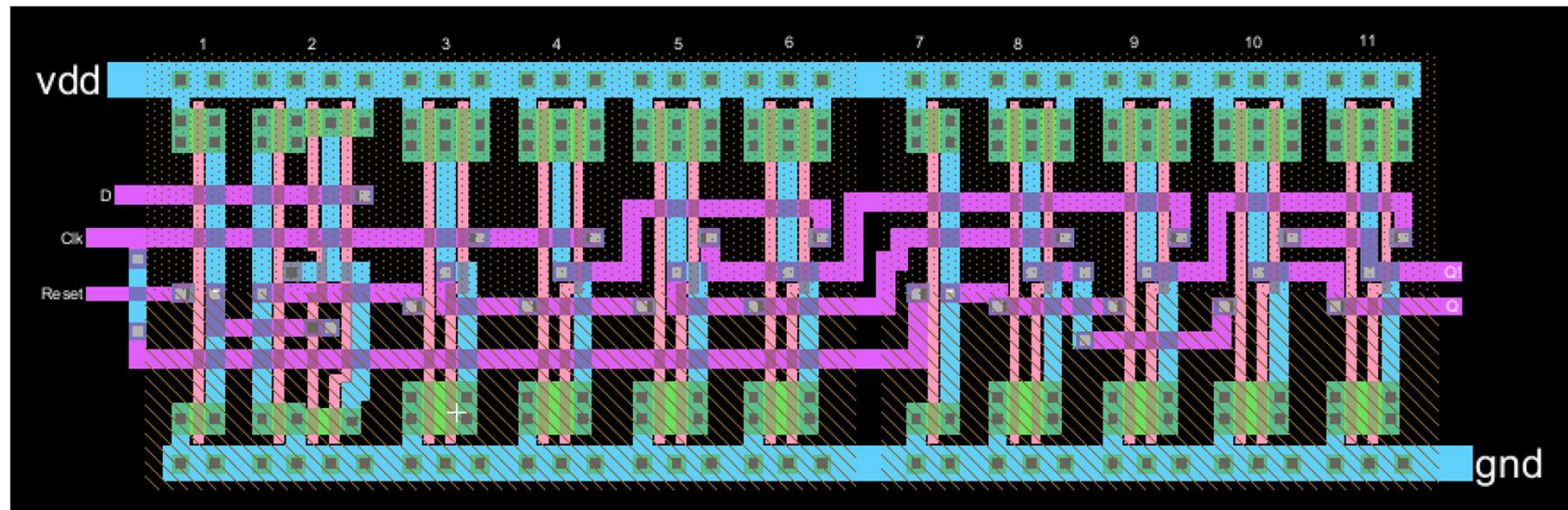
At last! Accumulator B



Testing Accumulator B



Positive Edge D Flip-flop Layout



Thank you!