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11/14/2025

VLSI Design

Very Simple Microprocessor Accumulator

Introduction

For the final project in the VLSI Design course, students each chose a component of a Very Simple Microprocessor to design in Electric VLSI. The end goal is that each student can combine their components to create the full functioning microprocessor. The chosen component covered in this report is Accumulator B which is seen in Figure 1.

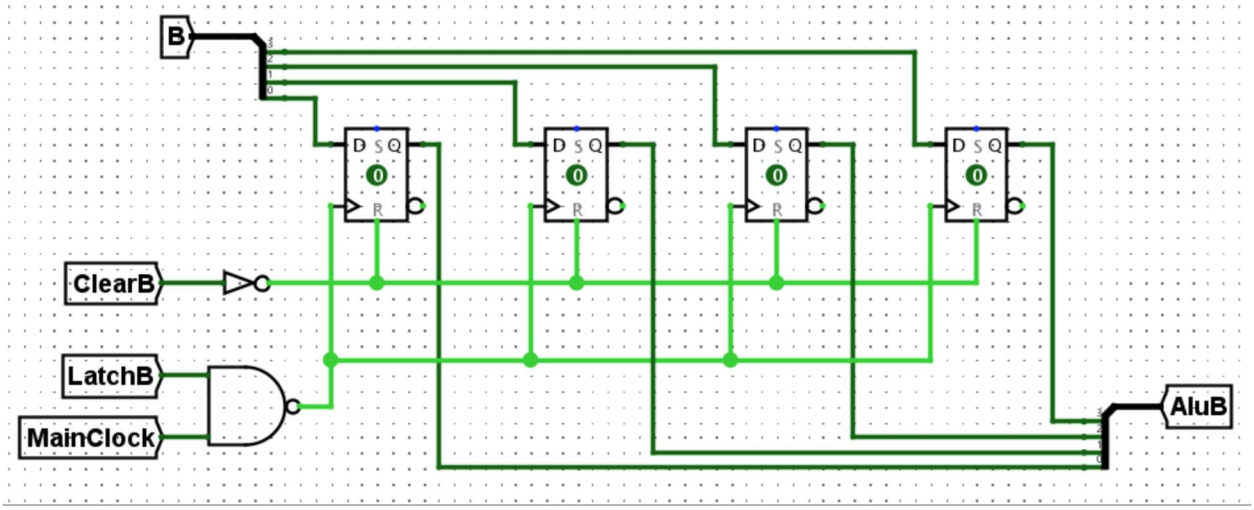

Figure 1: Accumulator B

The accumulator is simply a register in the microprocessor which stores intermediate results from ALU operations. From Figure 1, it is seen that the necessary circuit components are D Flip Flops, a NAND, and an Inverter.

Materials

Schematics, layouts, and simulations were created using Electric VLSI alongside LTSpice. Students were provided with access to the Harvey Mudd's component library, "muddlib07", which has an extensive list of rudimentary gates and flip-flops with schematics and layouts.

Schematics / Design Process

The first step of the design process was to find a D flip-flop to use since it is at the core of Accumulator B. The simplest D flip-flop from the Harvey Mudd library is seen in Figure 2.

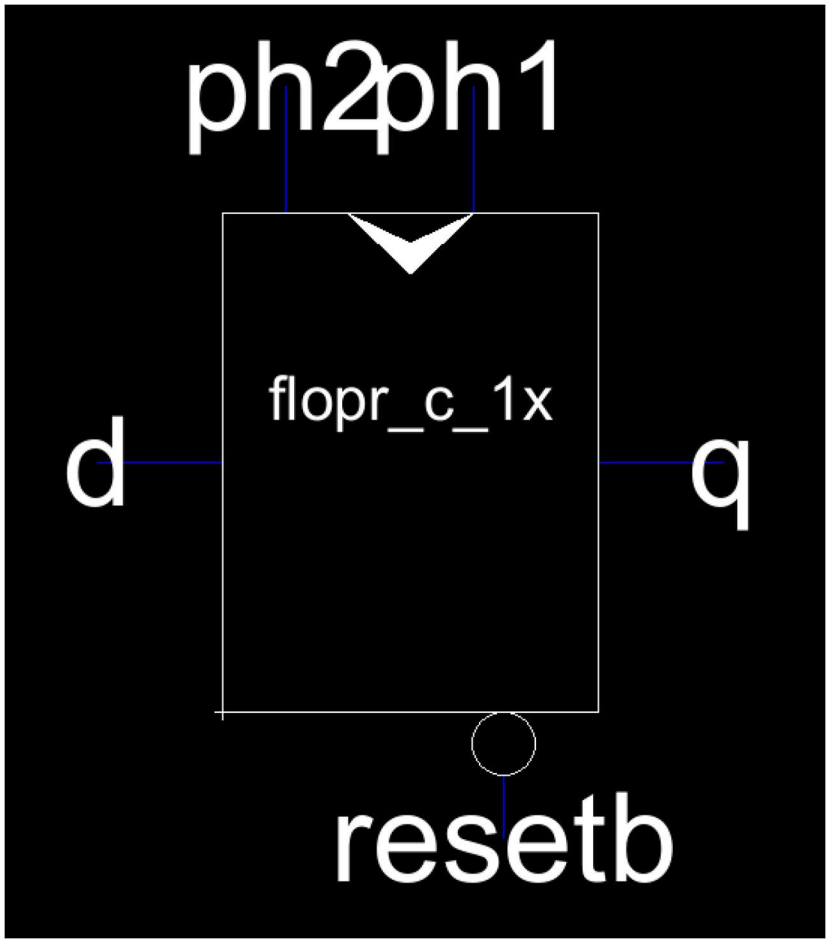

Figure 2: D flip Flop from Harvey Mudd's Library

The confusion began with the “ph2” and “ph1” labels. After researching, it was discovered that the D flip-flop was made in a master-slave latch configuration. Internally, there are two latches that require opposite clock pulses to pass data from the master latch to the slave latch. The master latch must be triggered from the first clock pulse, then the slave is triggered from a second clock pulse. The clock pulses cannot overlap or else there is a risk of both latches being triggered simultaneously. To operate the D flip-flop via a single clock pulse, a two phased clock signal can be created from a two-phase clock generator, seen in Figure 3.

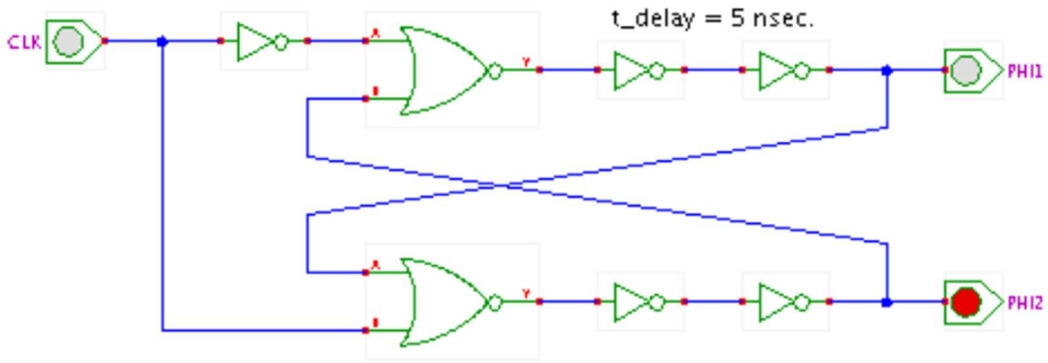

Figure 3: Two-phase Clock Generator

The two-phase clock generator takes in a single clock signal and produces two, non-overlapping inverted signals. In hopes of making the Harvey Mudd D flip-flop work, a schematic for a two-phase clock generator was created and simulated using the schematic seen in Figure 4.

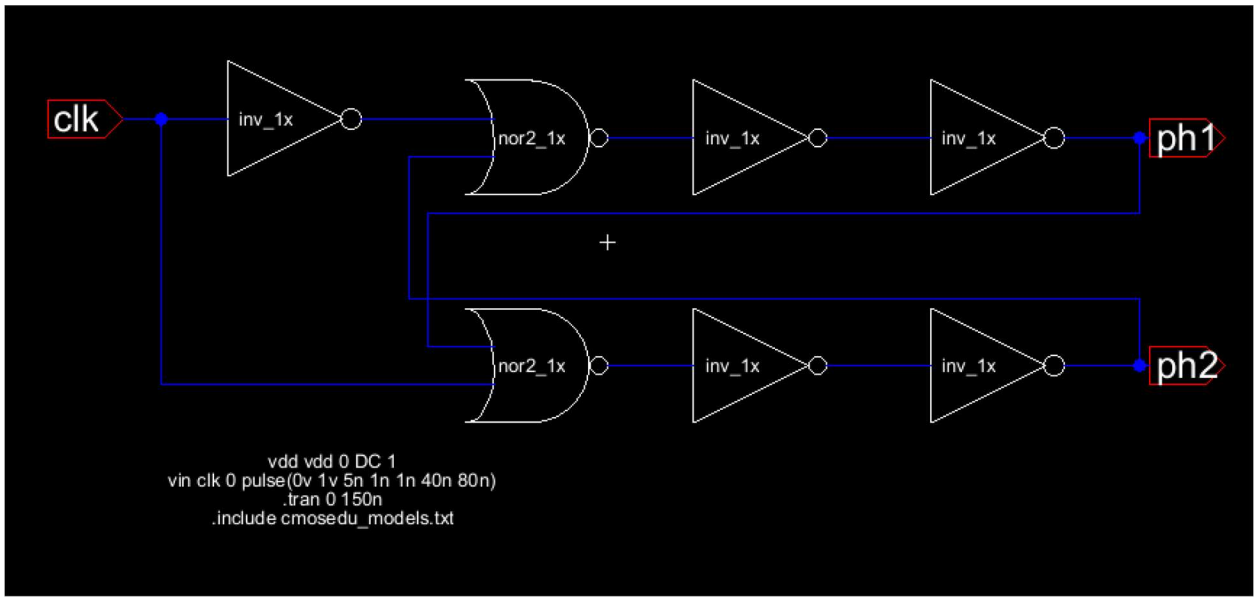

Figure 4: Two-phase Clock Generator Schematic

The results of the two-phase clock generator simulation are seen in Figure 5.

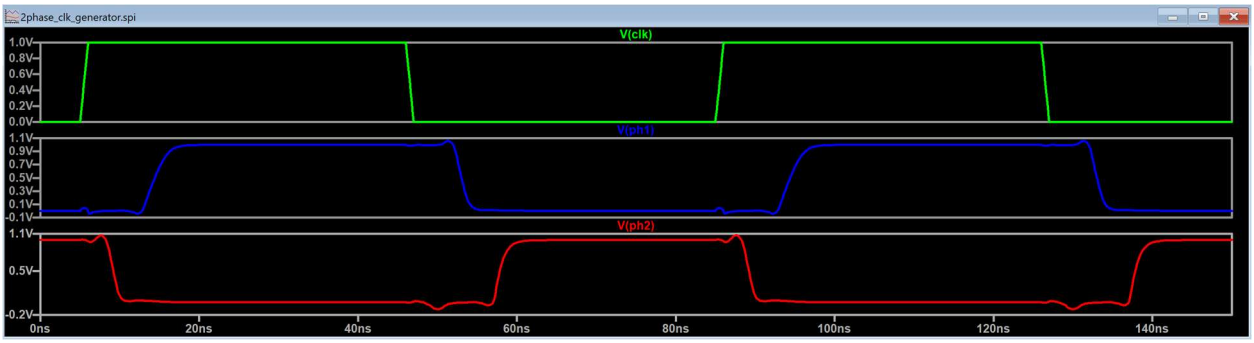

Figure 5: Two-phase Clock Generator Simulation Results

It can be observed that the two-phase clock generator succeeded in creating two clock pulses opposite each other and not having any overlap. The next step was to simulate the two-phase clock generator and the D flip-flop together to see if the flip-flop behaves accordingly. The simulation schematic for the two-phase clock generator and the D flip-flop from the Harvey Mudd library can be seen in Figure 6.

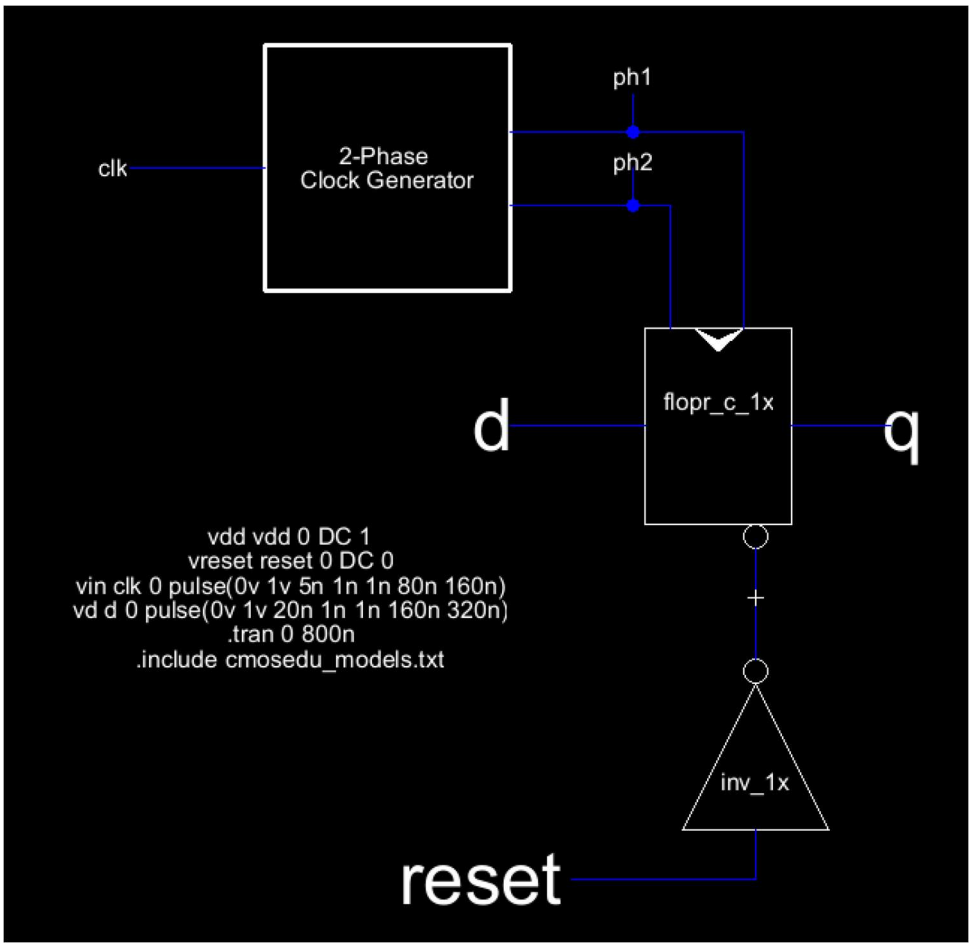

Figure 6: Two-phase D flip-flop Simulation Schematic

The results from the simulation are seen in Figure 7.

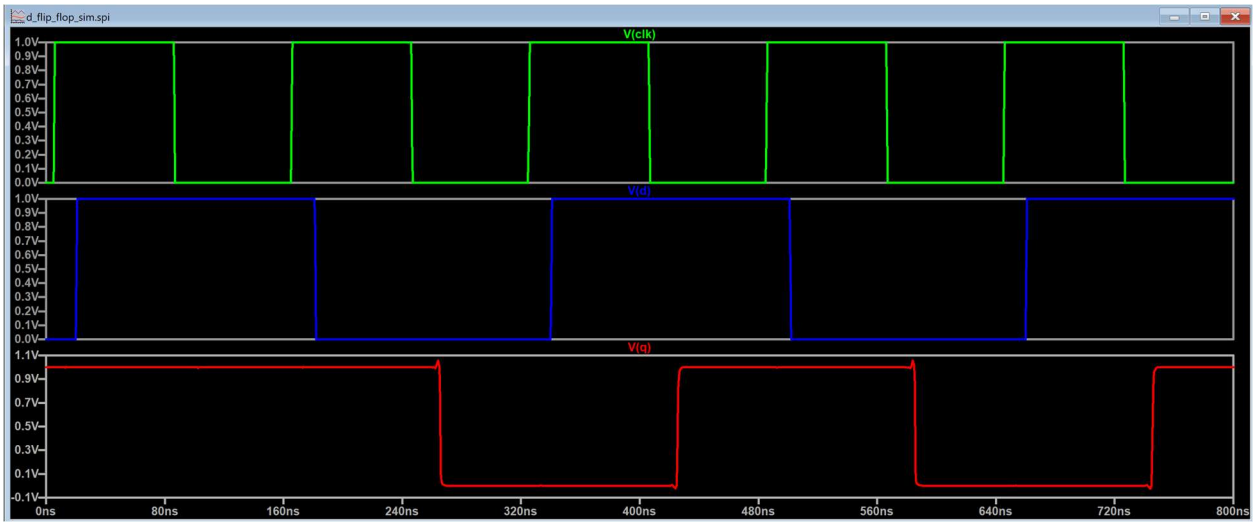

Figure 7: Two-phase D Flip-flop Simulation Result

It can be observed that the D flip-flop works but is triggered on negative edges of the clock pulse. As seen back in Figure 1, Accumulator B requires a positive edge triggered flip-flop. A pseudo positive edge triggered flip-flop could be created by inverting the clock, however, an easier solution presented itself, scrapping the Harvey Mudd flip-flop and making our own D flip-flop! A positive edge triggered D flip-flop was created which is seen in Figure 8. It was built following the schematic seen here.

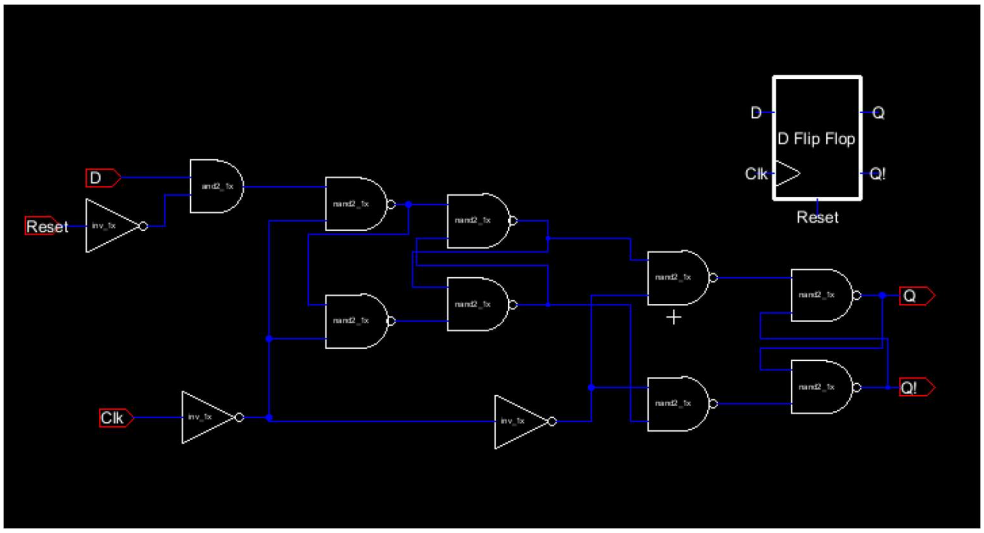

Figure 8: Positive Edge Triggered D Flip-flop Schematic

The only modification to the circuit is the implementation of the reset. The reset was implemented just using an AND gate that takes D and the inverted Reset signal as inputs. The logic is such that if Reset is high, the AND gate will be low and only provide a low input to the D Flip-flop. To ensure functionality of the homemade D flip-flop, it was simulated using the schematic seen in Figure 9.

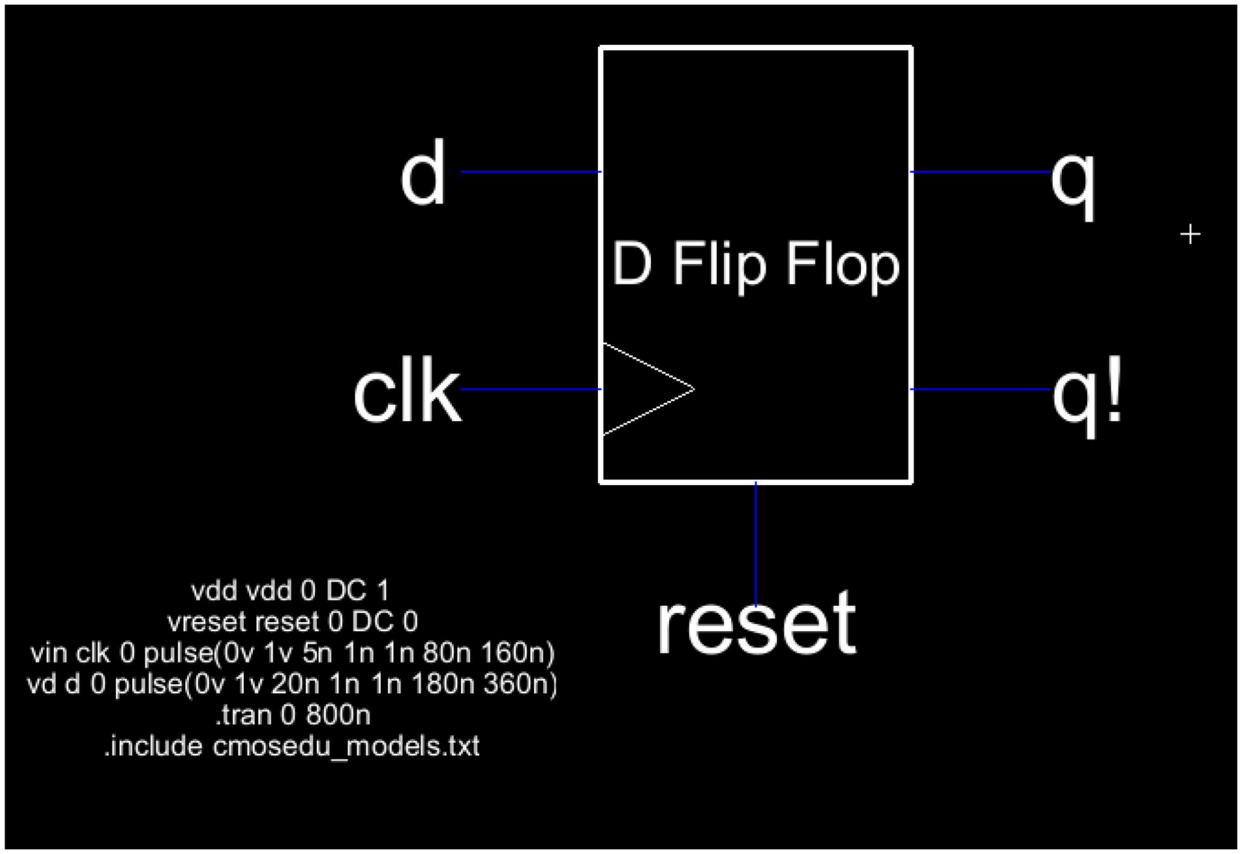

Figure 9: Positive Edge Triggered D Flip-flop Simulation Schematic

The results of the homemade D flip-flop simulation are seen in Figure 10.

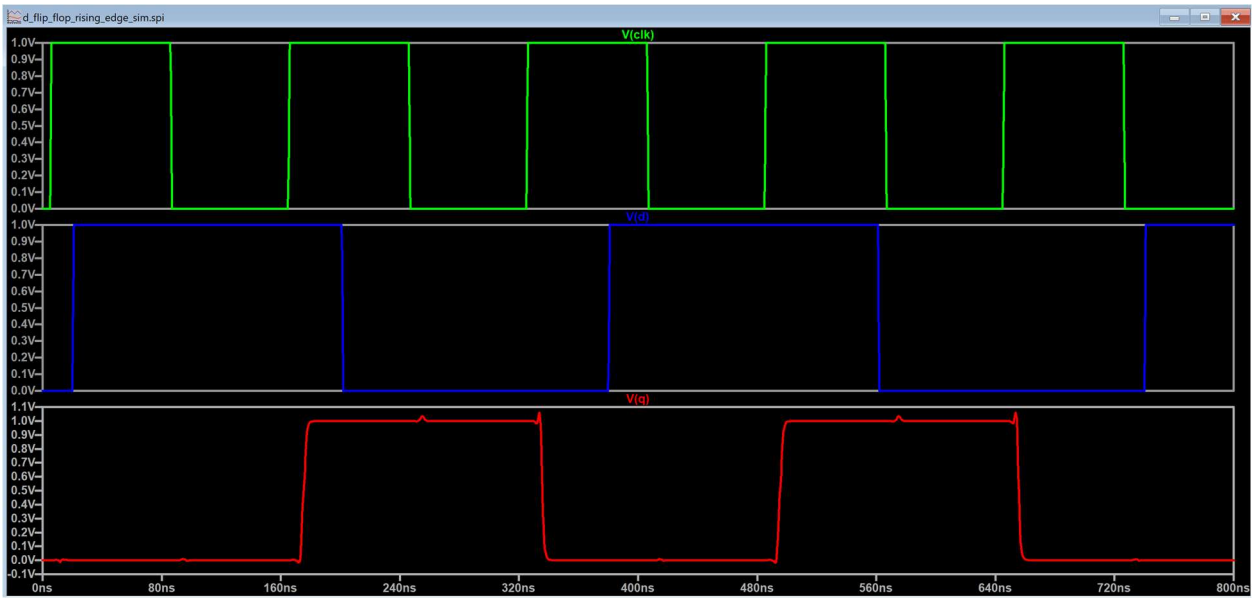

Figure 10: Positive Edge Triggered D Flip-flop Simulation Result

It can be seen in the simulation that the D flip-flop functions properly and only responds to positive clock edges. With the D flip-flop now working, the schematic for Accumulator B was created which is seen in Figure 11.

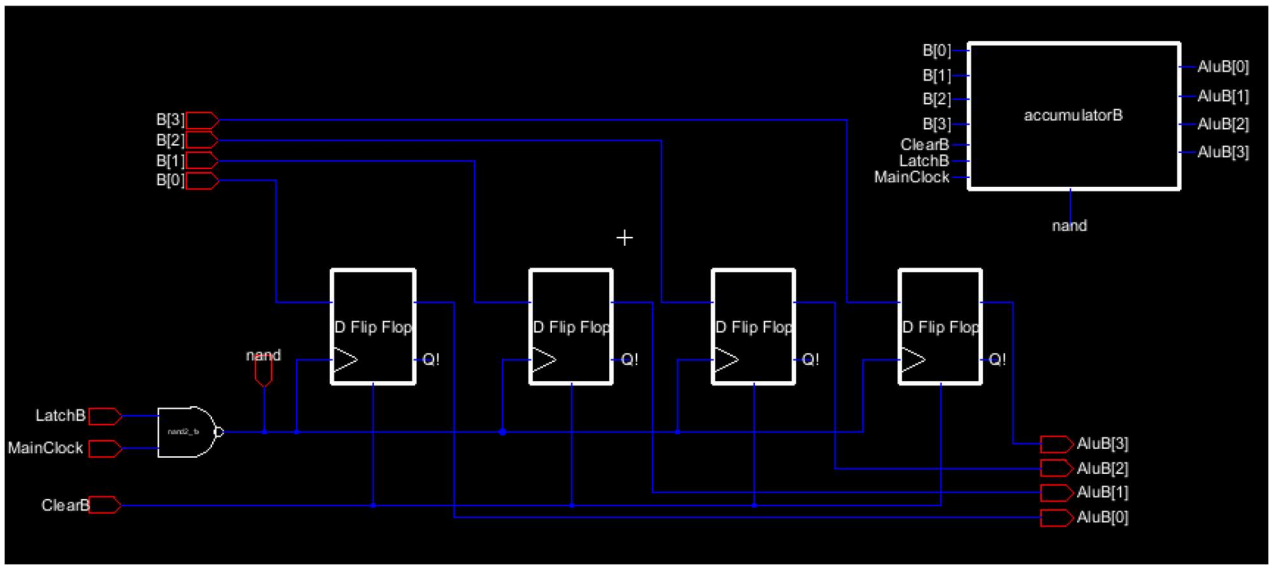

Figure 11: Accumulator B Schematic

The registers B and AluB from Figure 1 were implemented as four different exports, allowing each bit to be controlled and observed independently. Next, Accumulator B was simulated to ensure functionality using the schematic seen in Figure 12.

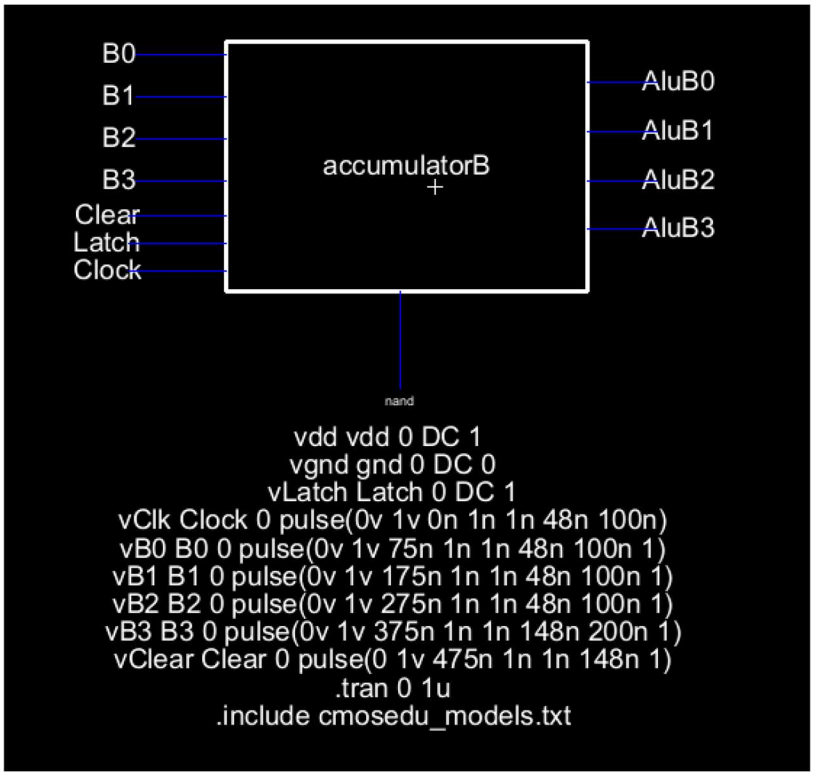

Figure 12: Accumulator B Simulation Schematic

The results of simulating accumulator B are seen in **Error! Reference source not found.**.

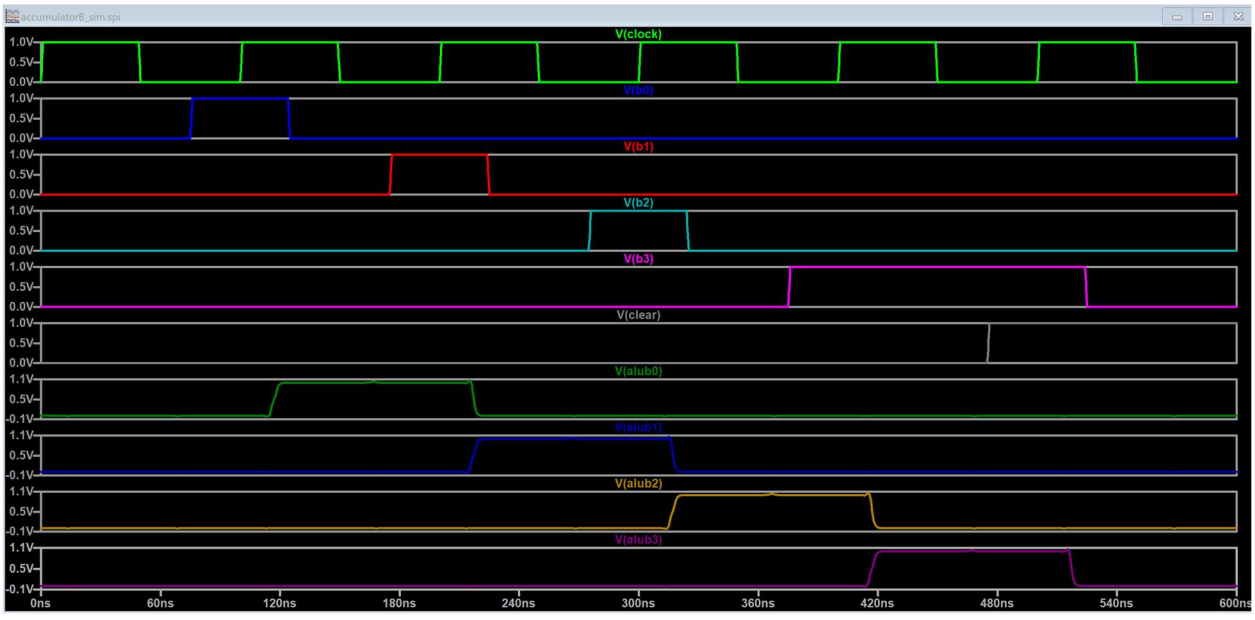

Figure 13: Accumulator B Simulation Result

The simulation raises each input register bit from 0 to 3 sequentially. It is observed that each input is passed to the output register and stored accordingly. It can also be observed from 480ns to 600ns that the clear signal latches the outputs to 0.

Layouts

The layouts for all fundamental gates (NAND, Inverter, NOR, etc.) were provided by the Harvey Mudd library. The first layout to create from the fundamental gates is the rising edge D flip-flop. The layout was created by carefully tracing the schematic and labelling each gate which is shown in Figure 14.

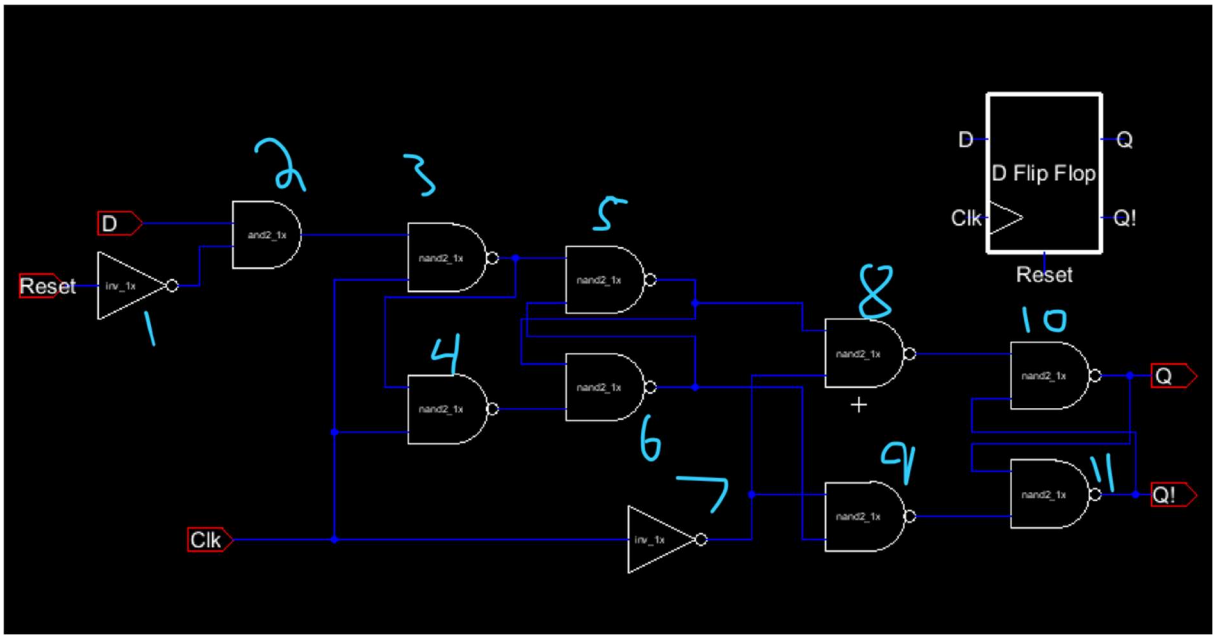

Figure 14: Rising Edge D Flip-Flop Gate Labeling

The resulting rising edge D flip-flop is seen in Figure 15.

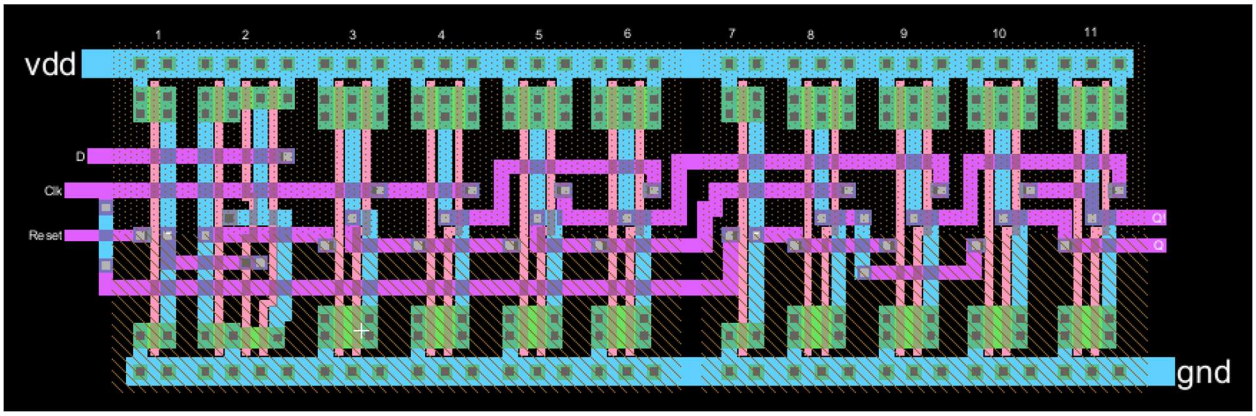

Figure 15: Rising Edge D Flip-Flop Layout

Next, the final accumulator B layout was created which is seen in Figure 16.

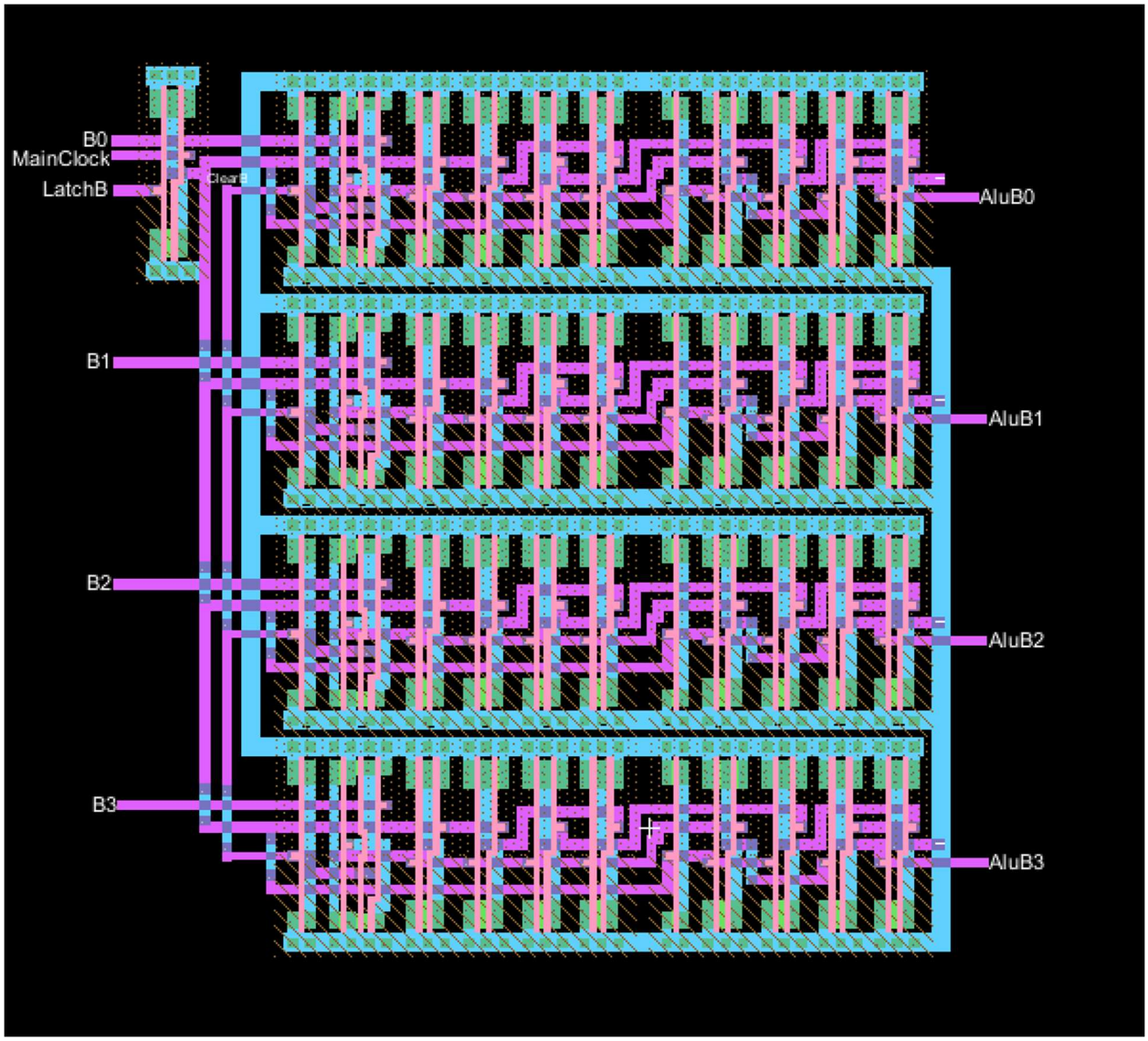

Figure 16: AccumulatorB Layout

Each D flip-flop was stacked vertically to provide ease of access to each of the D flip-flop's inputs and outputs. The only drawback from this decision is that the power rails had to be meticulously brought up from the sides of each D flip-flop.

Conclusion

This project successfully details the design, simulation, and layout of the accumulator B component for a Very Simple Microprocessor. A significant challenge emerged when the provided "muddlib07" D flip-flop was found to be unsuitable, as it operated on a negative edge trigger rather than the required positive-edge trigger. The core of the project became the successful design of a new D flip-flop. Using this new flip-flop, the 4-bit Accumulator B was built and simulated, confirming its ability to correctly store intermediate values and respond to the asynchronous clear signal. Finally, a compact layout was created by stacking the custom D

flip-flops. The resulting Accumulator B component is fully functional and ready for integration with other student components to complete the final microprocessor.