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Lab 2

Electric VLSI DAC Die

Introduction:

The goal for this lab is to have students layout the 5-Bit DAC from Lab 1 into a pad frame to create a die (Figure 1). The pad frame is the critical component of a die and is what allows IC pins to be connected to the actual circuitry inside the chip.

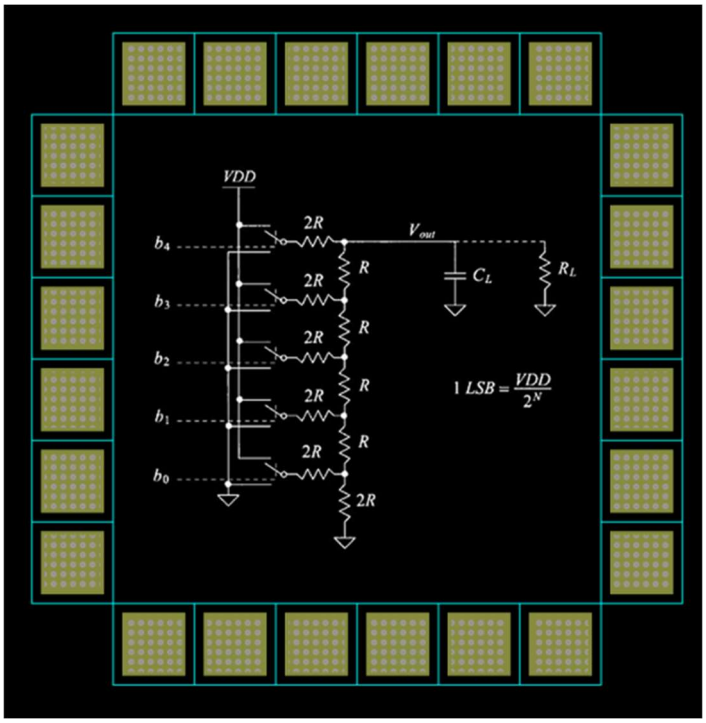

Figure 1: 5-Bit DAC Die

Methods and Materials:

The lab was completed by following the steps outlined by the "ENCE_3501_Lab_2.pdf" and "Lab_2_Padframe_DAC.pdf" handouts on the course Canvas page. The software used for this lab was Electric VLSI and LTSpice.

Schematics:

The circuitry at the center of the die is the 5-Bit DAC. The schematic for the DAC (Figure 2) comes from Lab 1 and the design process is explained in the respective report.

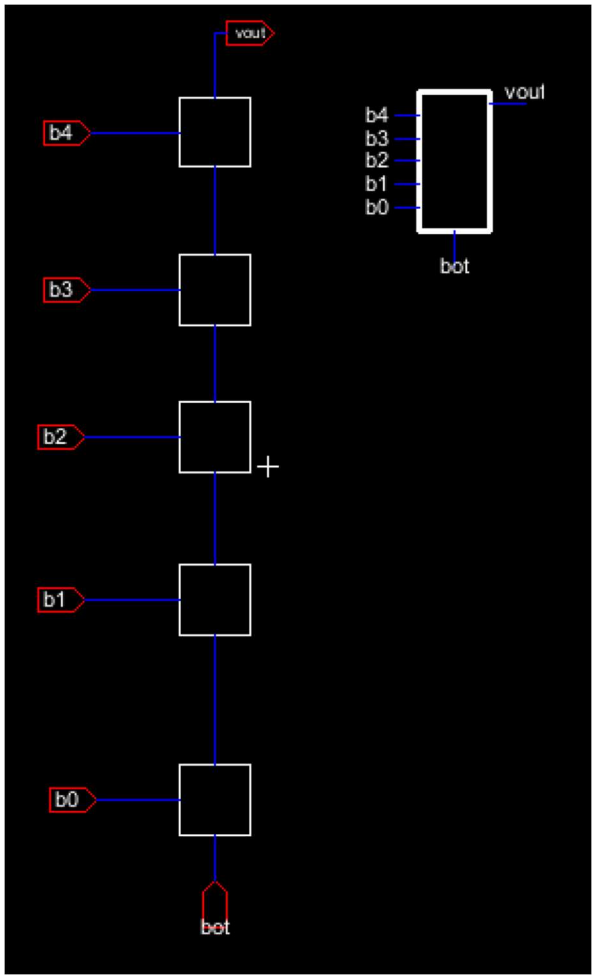

Figure 2: 5-Bit DAC Schematic

The first step of the lab was creating the pad schematic. In Figure 3, the pad is made by using an exported tunnel named “inout”. Secondly, an icon is created for the tunnel which visually represents the pad.

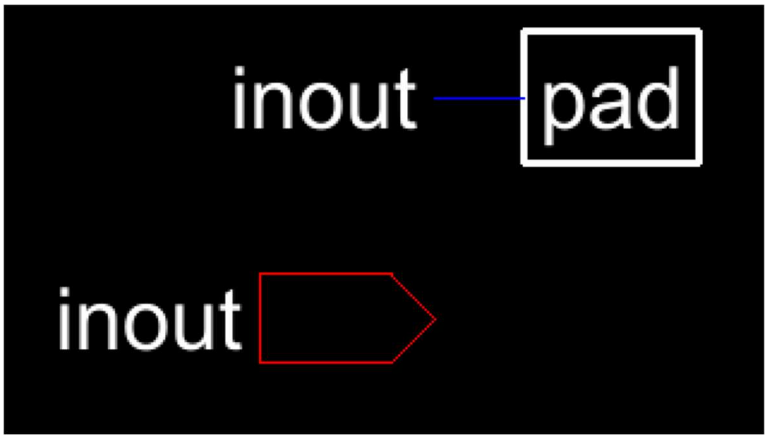

Figure 3: Pad Cell Schematic

Next, Figure 4, the pad frame schematic, is made from the pad schematic. There are 7 pinouts on the 5-Bit DAC (Figure 2). The minimum number of pad cells needed in order to connect all of the DAC pinouts while maintaining a square design is 8. Each pad is connected to a wire and a bus.

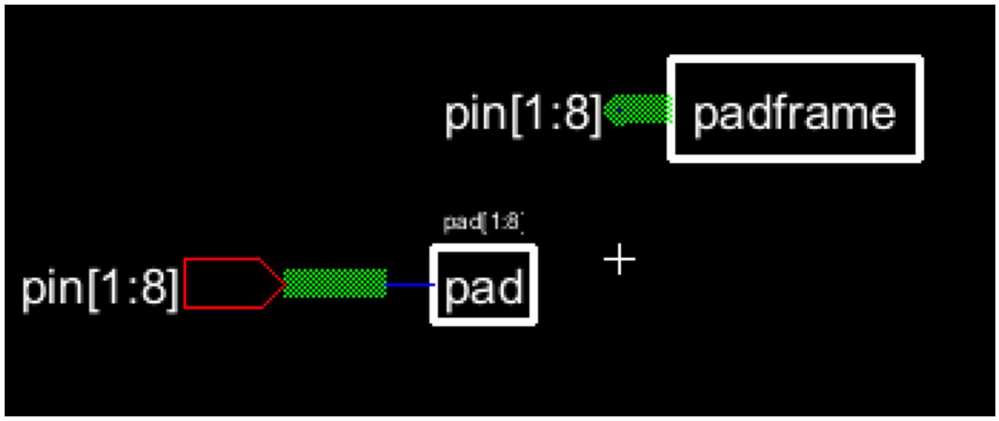

Figure 4: Padframe Schematic

Now that the pad frame schematic with 8 pad cells has been created, the DAC schematic and pad frame schematic can be combined into the final IC schematic (Figure 5). The pin connections from the DAC to the pad frame are decided by the layout in Figure 9.

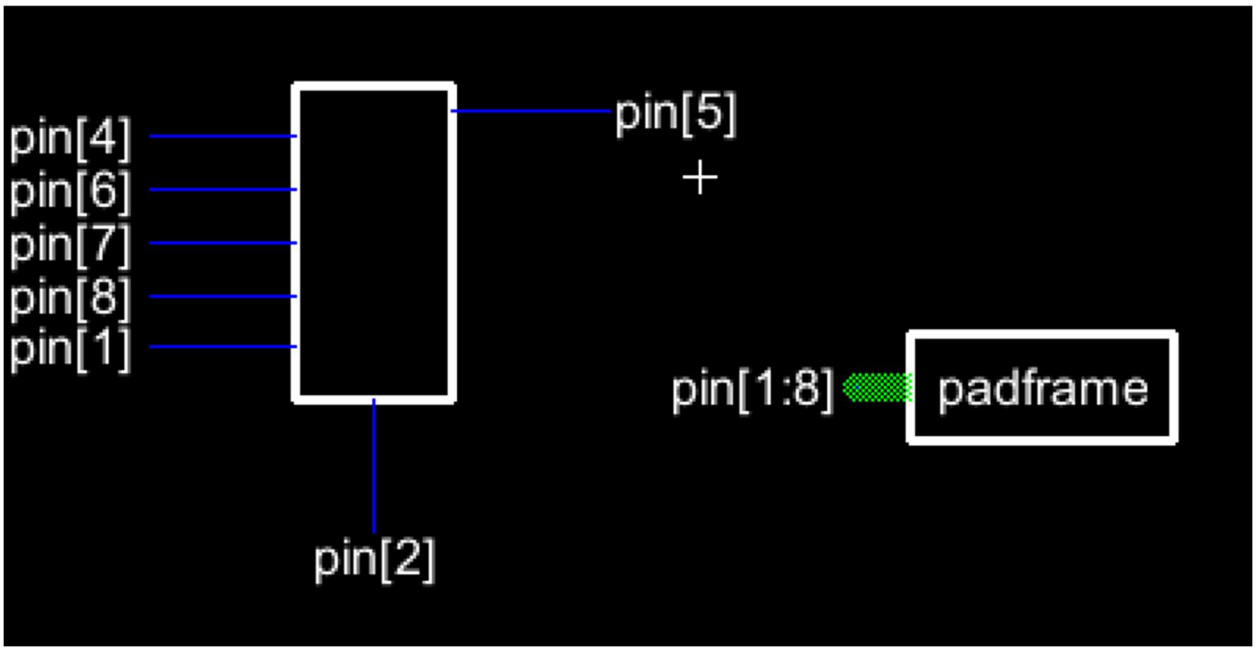

Figure 5: Padframe with DAC Schematic (Final IC)

Layouts:

The first component to layout is the pad. The only size constraint is that the die size must be smaller than 1.5mm x 1.5mm. The scale factor used for the lab is 300nm. Figure 6 shows the

drawn size for the pad that was used. The calculations to support the dimensions in Figure 6 are below.

$$Die\ size = \frac{1.5mm}{300\text{nm}} = 5000$$

$$Pad\ Drawn\ Size = \frac{Die\ Size}{Pads\ per\ side\ including\ corners} = \frac{5000}{10} = 500$$

By using a pad drawn size of 400, it is guaranteed that the die size will remain within 1.5mm x 1.5mm or 5000 x 5000. The bonding pad size was chosen to be 250 x 250 or 75µm x 75µm to ensure there is sufficient spacing between bonding pads.

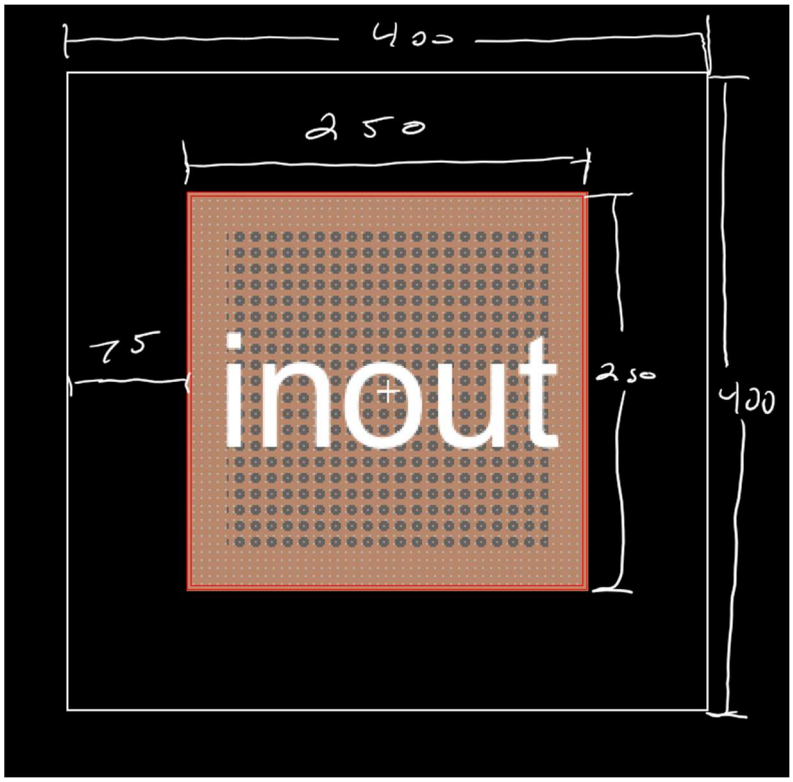

Figure 6: Pad Layout with Relevant Dimensions

Each of the 8 pads is laid out into the pad frame in square formation (Figure 7). Each pad is labeled as an export with a corresponding pin.

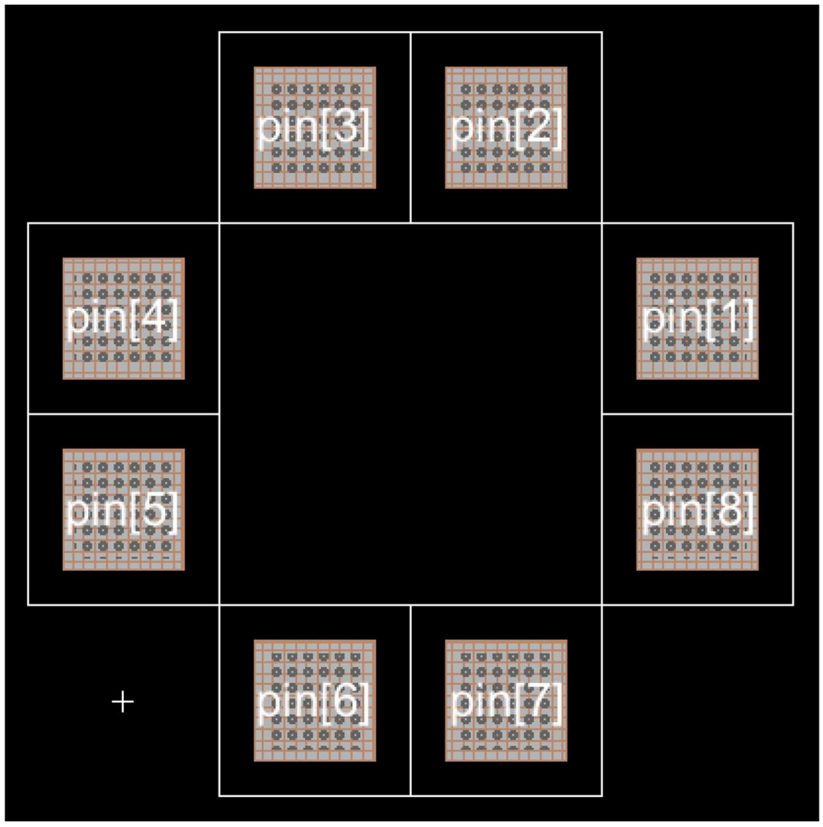

Figure 7: Padframe Layout

Now that the pad frame is complete, it is time to incorporate the 5-Bit DAC from Lab 1 (Figure 8) into the pad frame.

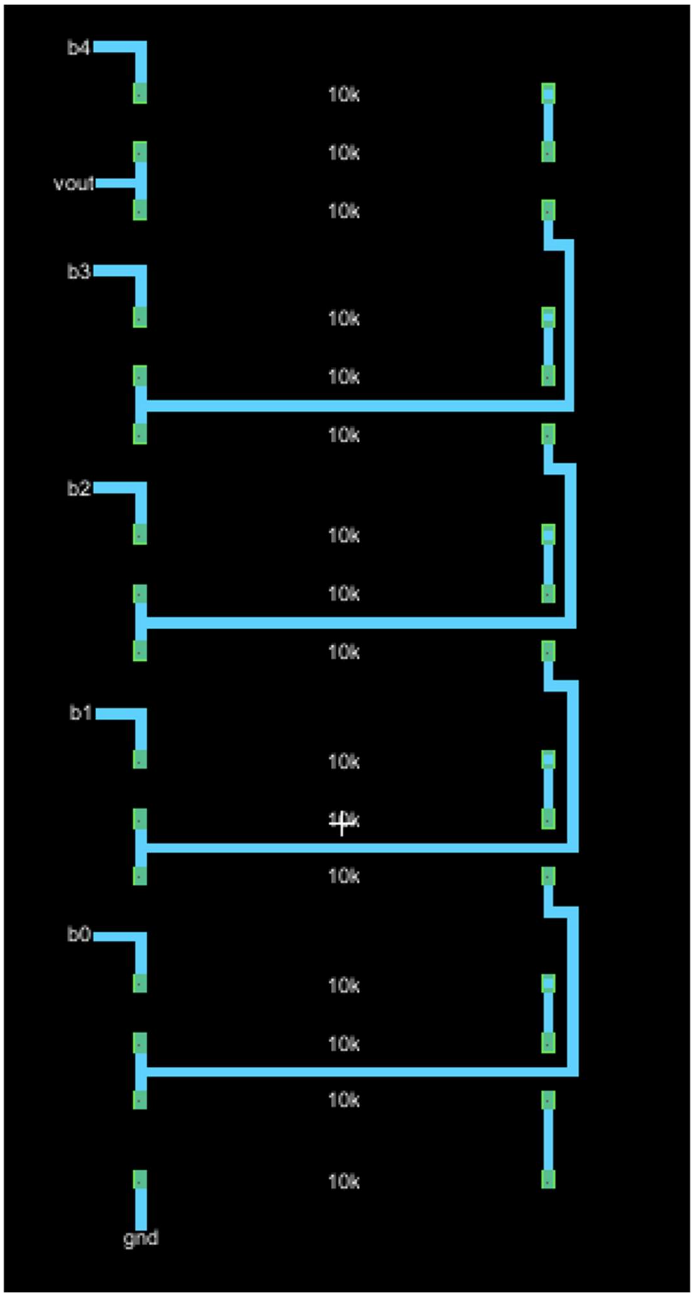

Figure 8: 5-Bit DAC Layout

The 5-Bit DAC Layout is put in the center of the pad frame and each of the pinouts from the DAC are connected to a pad on the pad frame (Figure 9). Vias are required to connect the wires from the DAC to the pads since they are on different metal layers.

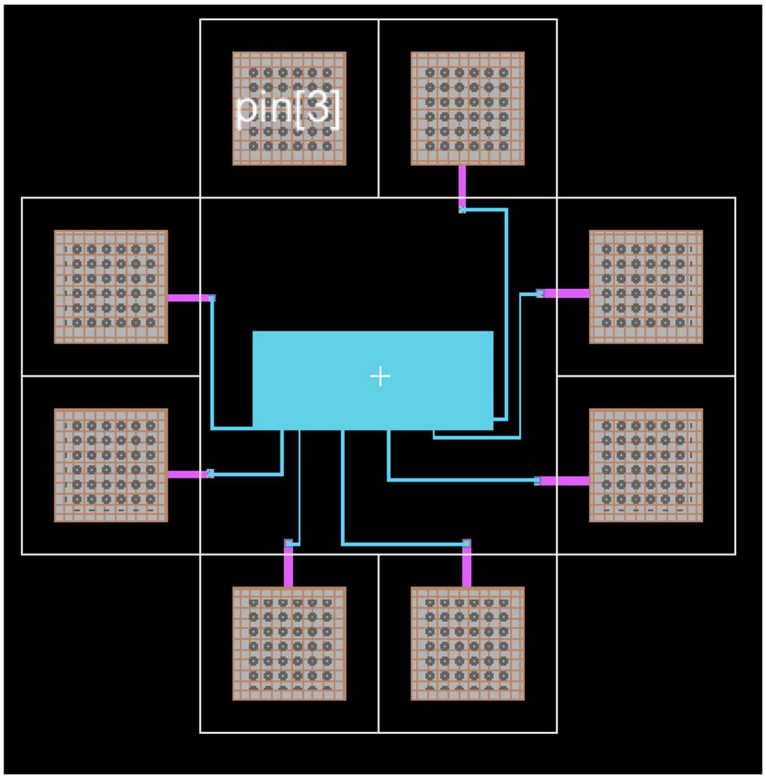

Figure 9: Padframe with DAC Layout (Final IC)

At this point, the die has been assembled.

Conclusion:

In conclusion, students first created a bonding pad which fits the design constraints. With the pad, a pad frame was assembled that supports up to 8 pins. Lastly, a 5-Bit DAC was connected to the pad frame, and a simple die was successfully designed.