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Lab 5

Electric VLSI Full Adder

Introduction:

In this lab, students created schematics and layouts of a 2-input NAND and a 2-input XOR gate which were put together to create a full adder. The full adder circuit is seen in Figure 1.

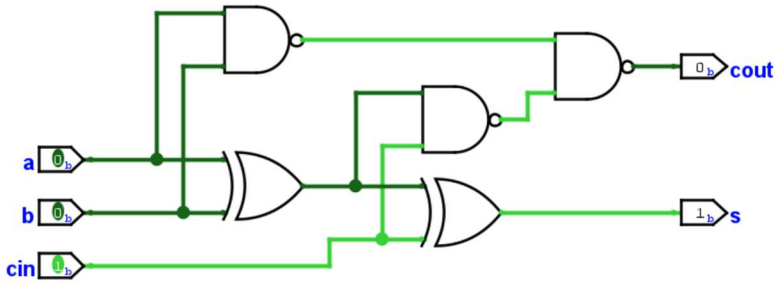

Figure 1: Full Adder Circuit

Methods and Materials:

The lab was completed by following the steps outlined by the "ENCE_3501_Lab_5.pdf" and "Lab_5_Full_Adder.pdf" handouts on the course Canvas page. The software used for this lab was Electric VLSI and LTSpice.

Schematics:

The first component to create a schematic for is the 2-input NAND gate as seen in Figure 2. The dimensions for the CMOS were given in the lab handout.

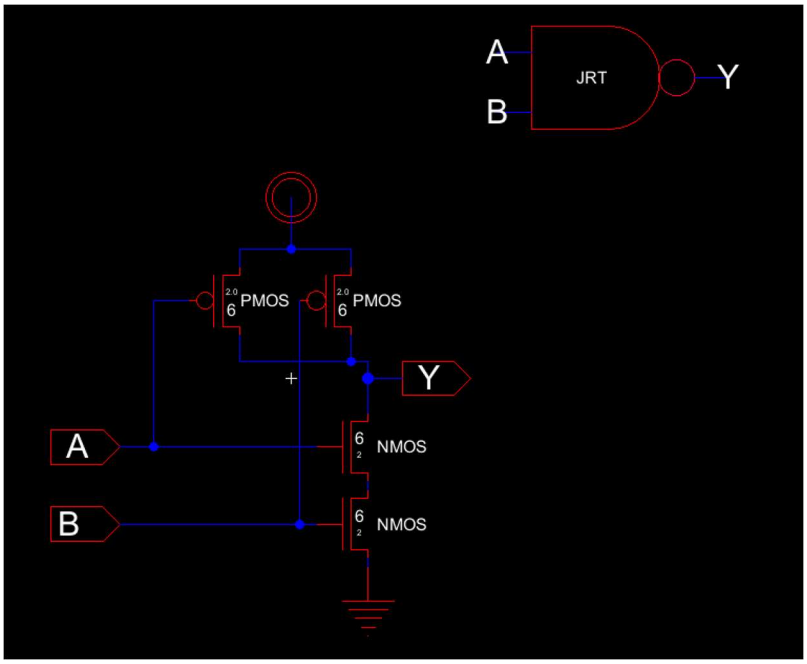

Figure 2: NAND2 Schematic

Once the schematic had been created, the NAND gate was simulated to ensure it matched the expected truth table. In Figure 3, the NAND gate is simulated such that all 4 possible input combinations can be observed.

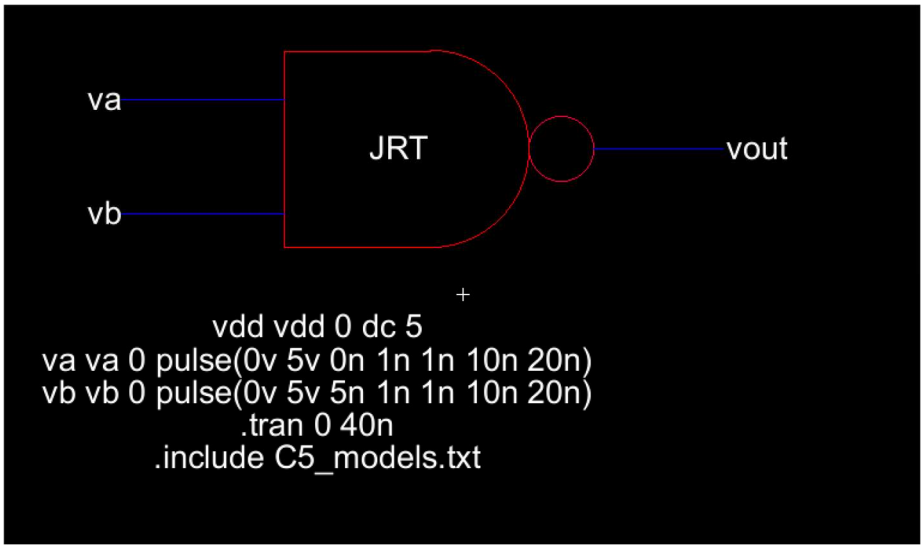

Figure 3: NAND2 Simulation Schematic

The results of the simulation are seen in Figure 4.

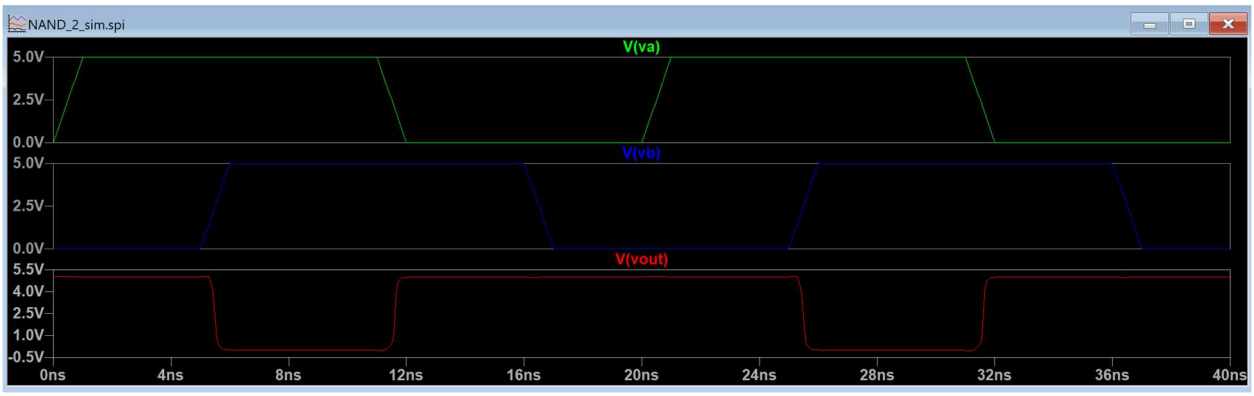

Figure 4: NAND2 Simulation Results

The NOT gate behaves accordingly, the output is only zero when both inputs are Vdd. The next gate to design is a NOT gate. This is crucial to create the XOR later. The schematic for the NOT gate is seen in Figure 5.

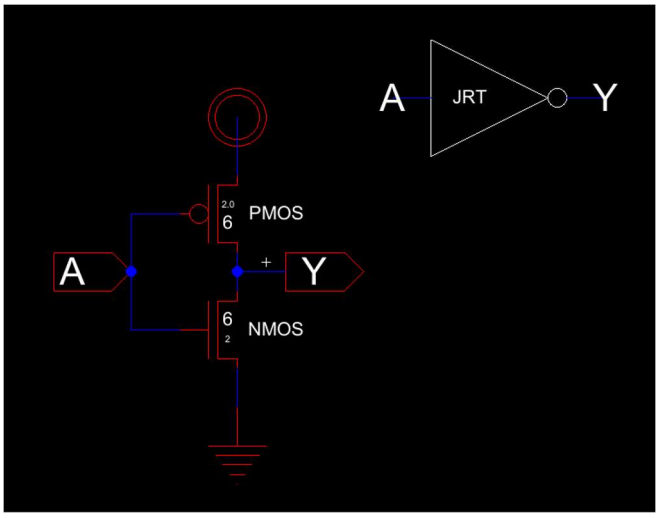

Figure 5: NOT Schematic

The NOT gate is simulated using the schematic in Figure 6 to ensure its functionality and switching point are sufficient.

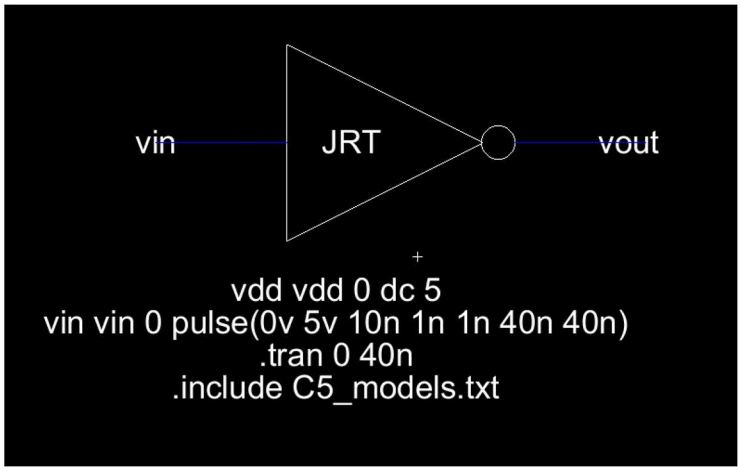

Figure 6: NOT Simulation Schematic

The results of the simulation are seen in Figure 7.

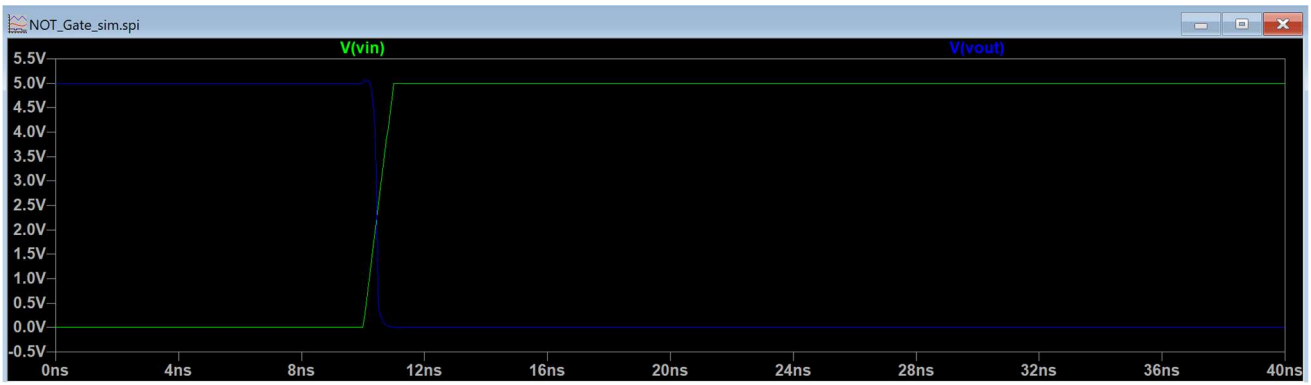

Figure 7: NOT Simulation Result

The NOT gate behaves accordingly, input of 0 is output of Vdd and vice versa. The switching point is acceptable since it crosses Vin near Vdd/2. Using the NOT gate, an XOR is created as seen in Figure 8.

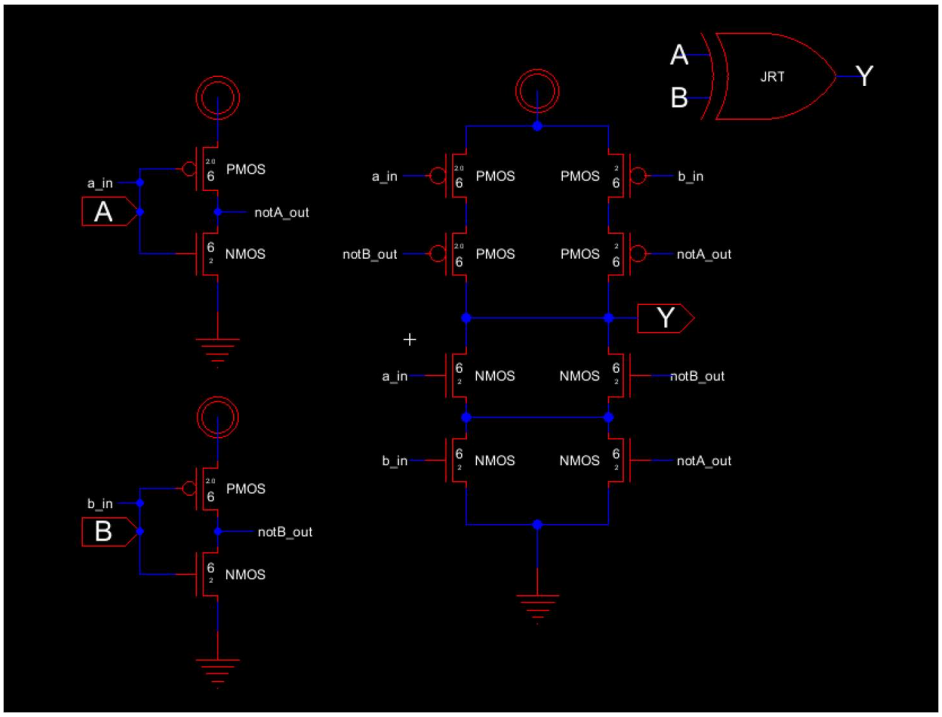

Figure 8: XOR Schematic

Once the schematic had been created, the XOR gate was simulated to ensure it matched the expected truth table. In Figure 9, the XOR gate is simulated such that all 4 possible input combinations can be observed.

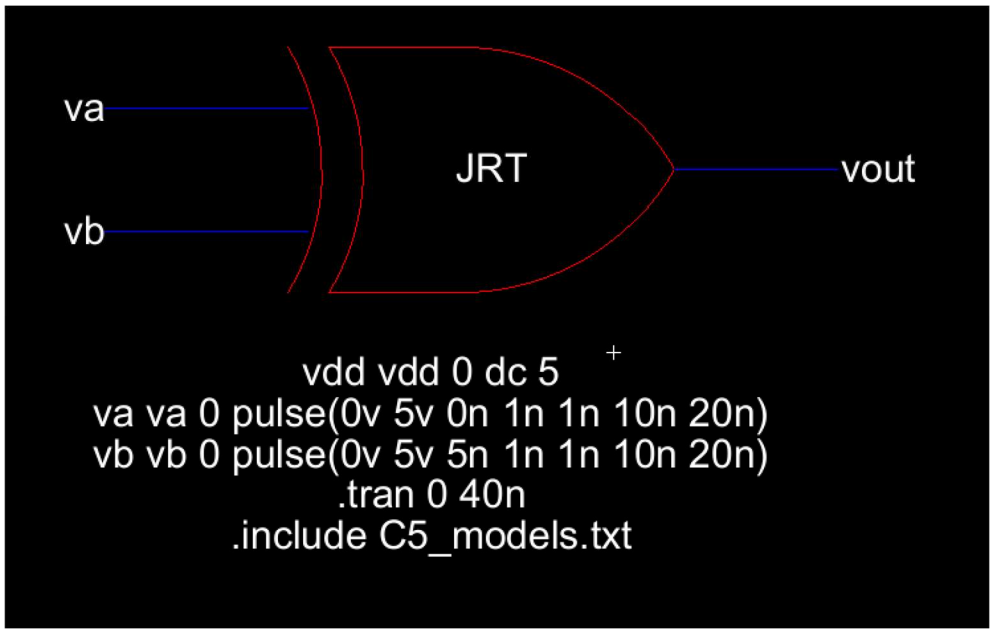

Figure 9: XOR Simulation Schematic

The results of the XOR gate are seen in Figure 10. The XOR gate behaves accordingly.

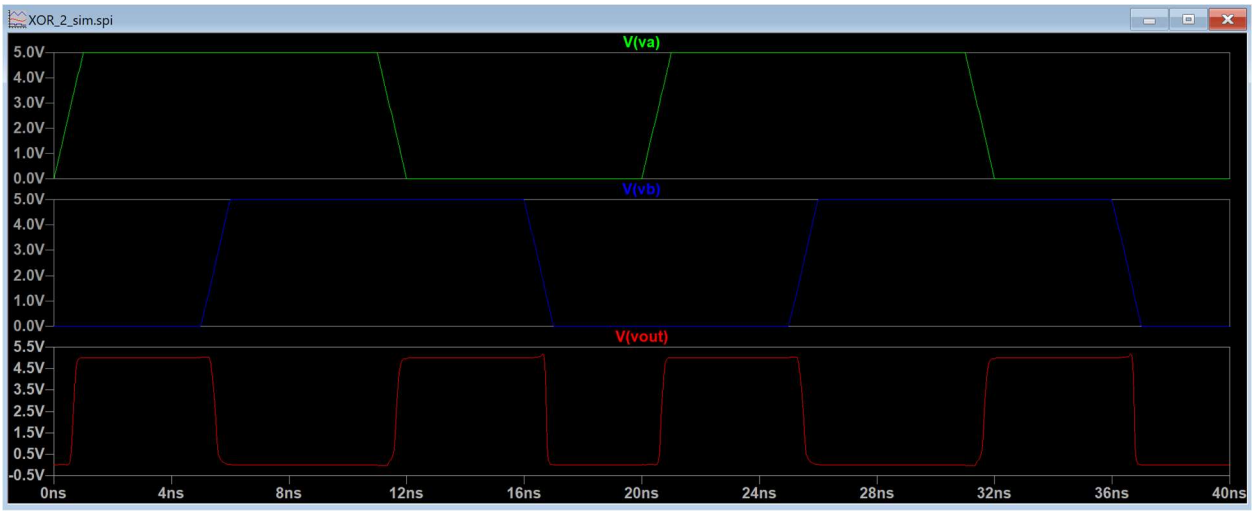

Figure 10: XOR Simulation Result

Now that all the fundamental components are created, the Full Adder schematic is assembled. The schematic is seen in Figure 11.

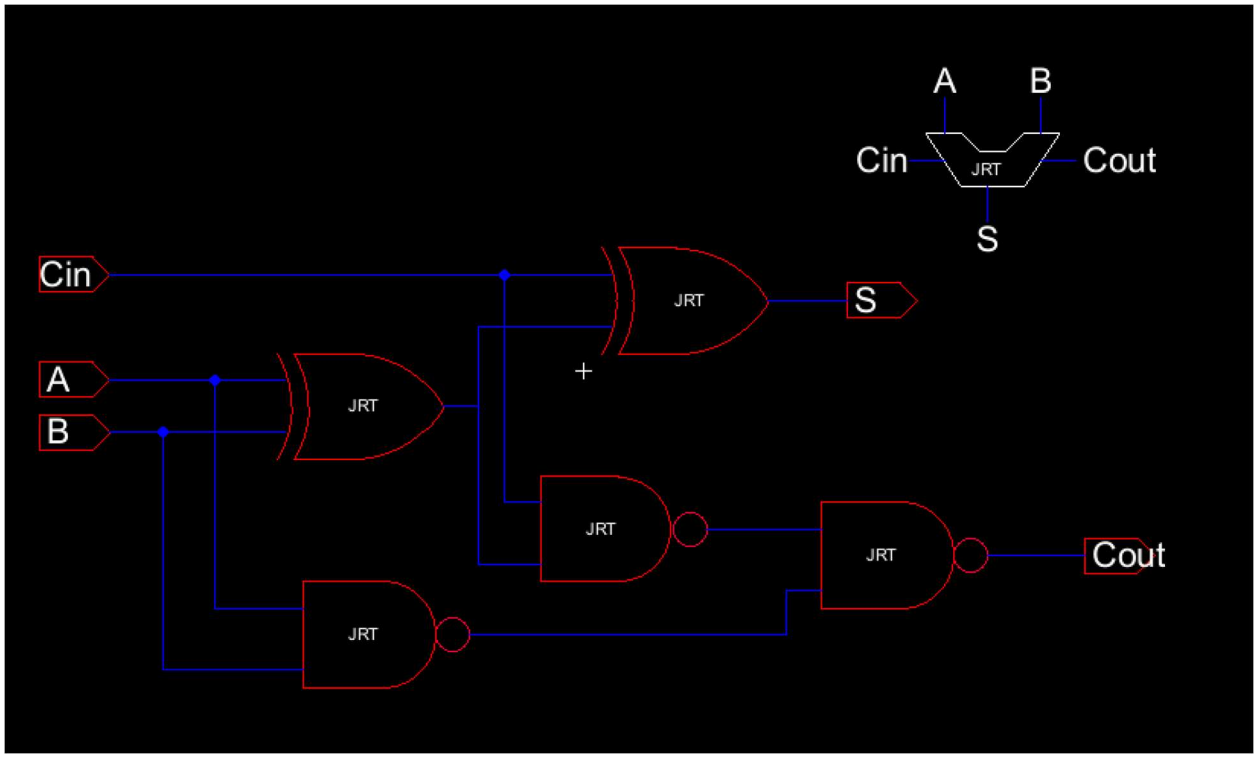

Figure 11: Full Adder Schematic

To ensure functionality of the Full Adder, a simulation is done as seen in Figure 12.

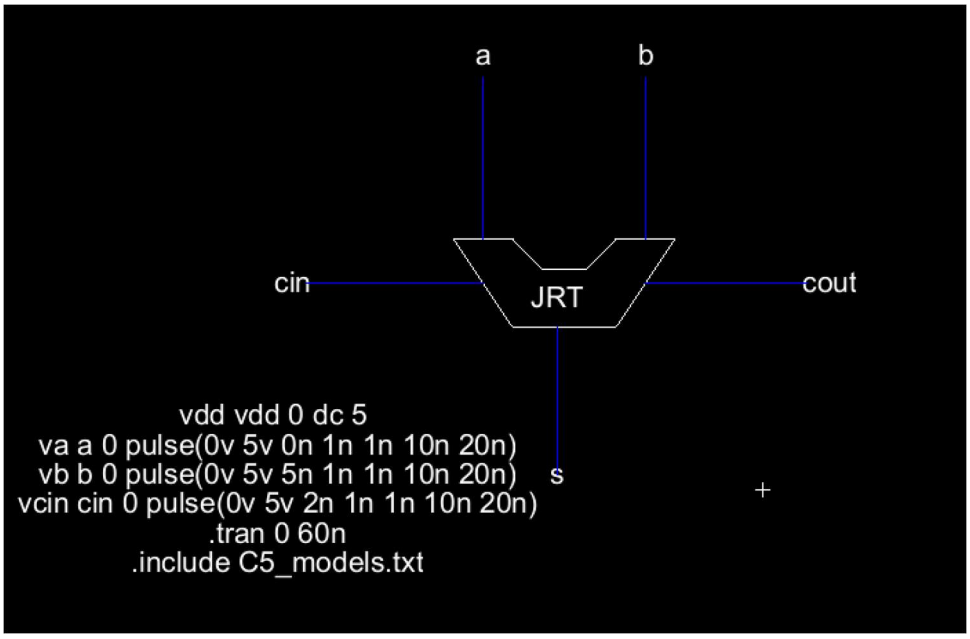

Figure 12: Full Adder Simulation Schematic

Simulation results are seen in Figure 13.

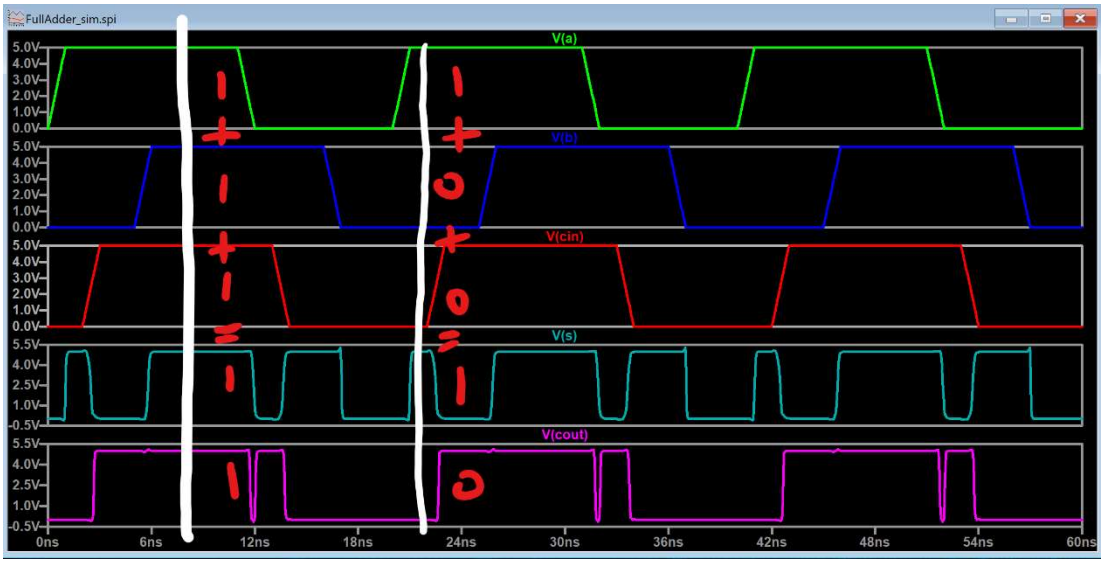

Figure 13: Full Adder Simulation Results

It can be observed that the simulation results match the expectations of a fuller adder's truth table. Along the first white line, the 3 inputs are all 1. This results in a sum of 1 with a carry out with 1. Along the second white line, there is only an input of 1 and the sum is 1 with a carry out of 0. These two white lines verify that the full adder is functional, therefore, all predecessor gates are functional. Timing of the input pulses matter as delays can propagate through a circuit and cause unexpected outputs.

Layouts:

The first layout to be made is the 2-input NAND gate which is seen in Figure 14.

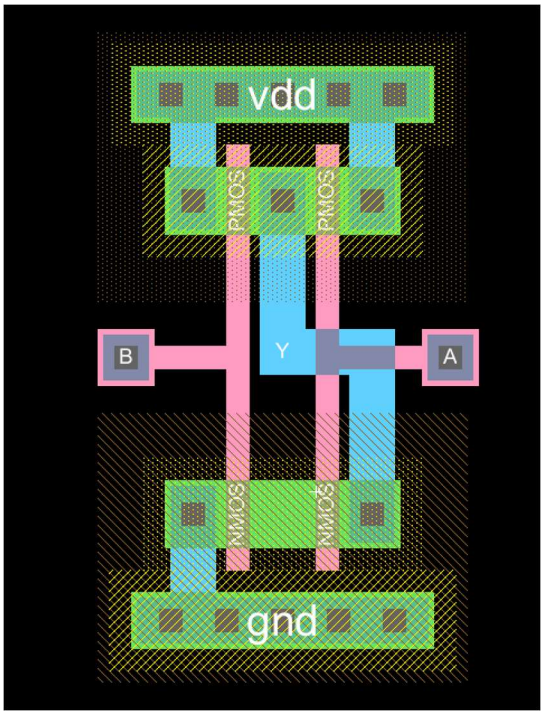

Figure 14: NAND2 Layout

The next layout is the NOT gate seen in Figure 15.

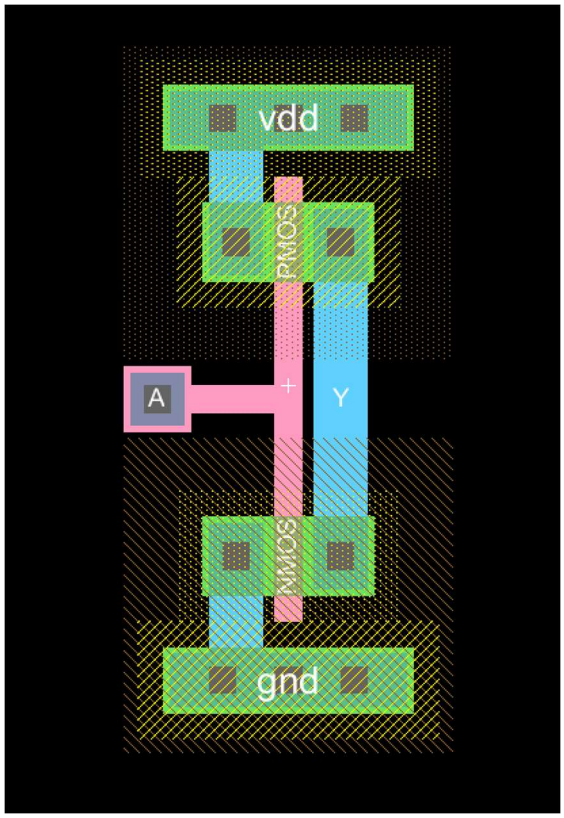

Figure 15: NOT Layout

The last gate to layout is the XOR as seen in Figure 16.

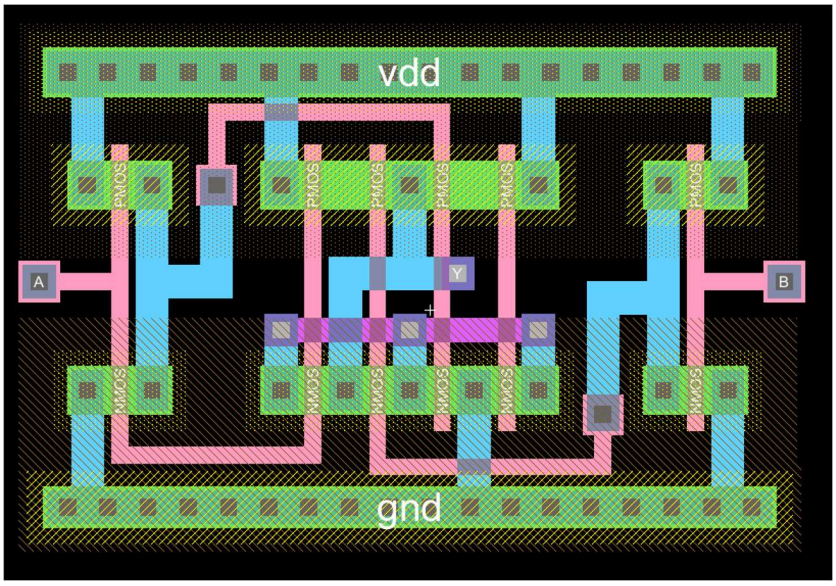

Figure 16: XOR Layout

Now, the Full Adder is laid out using 2 XOR and 3 NAND gates. The layout is seen in Figure 17. The gates are connected to match Figure 11.

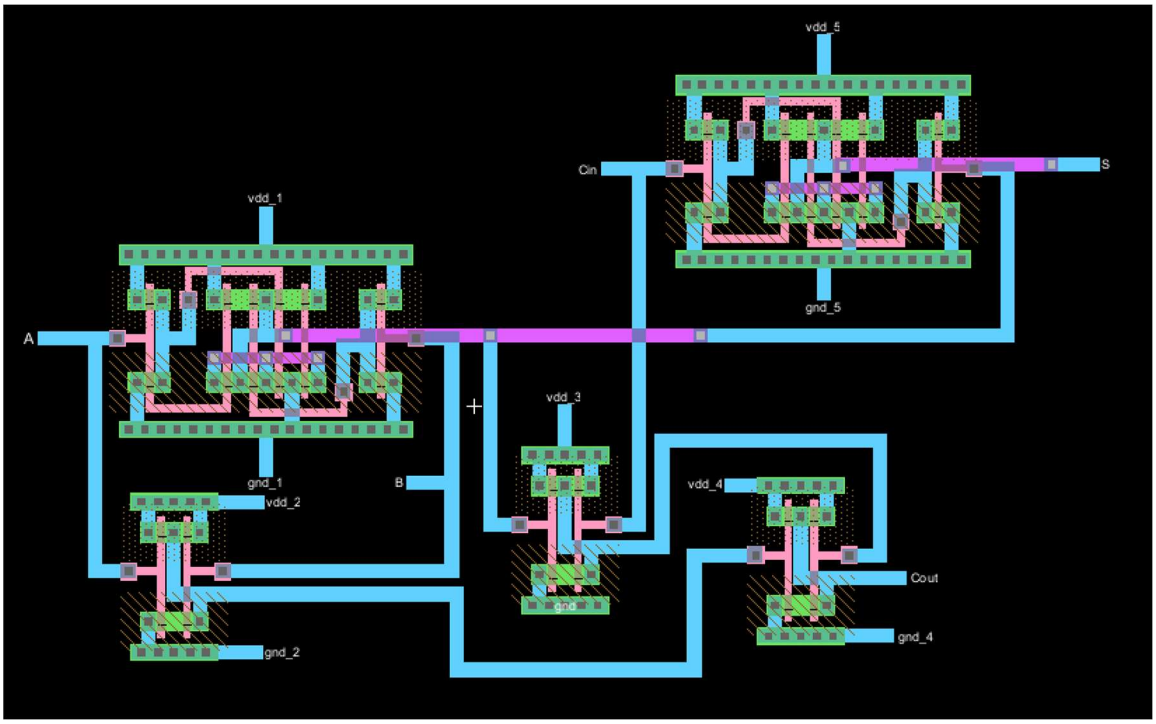

Figure 17: Full Adder Layout

Conclusion:

All in all, students created schematics and layouts for NOT, NAND, and XOR gate. These gates were laid out together to create a full adder.