Jianming Zheng

Irvine, CA

(669) 269-3928 | jianmiz1@uci.edu | https://www.linkedin.com/in/jeremy-zheng-a207aa278

EDUCATION

University of California, Irvine March 2026

B.S. in Computer Science & Engineering **GPA: 3.92**

- **Awards**: Dean's Honors List (9x), Hackathon Winner (1x)
- **Relevant Coursework**: Embedded Software, Internet of Things (IoT), Computer Architecture, Machine Learning, Computer Vision, Operating Systems, Computer Networks, Data Structures

SKILLS

- Programming: C/C++, Embedded C, Python, SQL (PostgreSQL, MySQL), JavaScript, Node.js, Express.js, HTML/CSS, VHDL, System Verilog
- Hardware Tools: Oscilloscope, Logic Analyzer, Multimeter
- Tools & Platforms: AWS, GitHub, Git, Linux, PlatformIO, Arduino
- Frameworks & Libraries: NumPy, Scikit-learn, TensorFlow, PyTorch, EJS, jQuery
- Development Methodologies: Agile
- Languages: Mandarin (Fluent), Spanish (Elementary)

CERTIFICATES

AWS Certified AI Practitioner – Amazon Web Service July 2025
MySQL Implementation Certified Associate – Oracle Jun. 2025
AWS Certified Cloud Practitioner – Amazon Web Service Apr. 2025
PostgreSQL for Everybody Specialization – University of Michigan | Coursera Apr. 2025

EXPERIENCE

UCI Embedded & Cyber-Physical Systems Lab Jan. 2025 - Present

Undergraduate Researcher

- Implemented LLM-based motion planning on **DJI Tello** drone to reproduce results from "*TypeFly*" research.
- Developed UI controls (**Python Gradio**) to simulate visual security attacks (blur, distortion) in drone perception.
- Integrated **YOLOv8** computer vision model for real-time object detection on embedded drone platform.

PROJECTS

Pipelined Processor and ALU FPGA Implementation Jan. 2025 - Mar. 2025

- Designed and synthesized a **pipelined MISP-32** processor and counter in **System Verilog**.
- Verified 15 ALU operations with 100% accuracy and deployed on **Basys 3 FPGA**.
- Diagnosed and optimized -76.065ns timing slack in pipeline using **Vivado**.

Smart-Sit Guardian Sep. 2024 - Dec. 2024

GitHub Repo

- Programmed **C++** firmware on **LILYGO ESP32** to interface heart rate, motion, and SpO_2 sensors via **I²C** to ensure reliable data sampling every 3 seconds.
- Configured **AWS IoT Core**, **DynamoDB**, and **S3** to transmit health data via **MQTT** and retain100 latest record in the AWS cloud.
- Built a web dashboard (**JavaScript, HTML/CSS**) to visualize sensor data and promote healthier user routines

Custom Alarm Clock Mar. 2024 - June. 2024

- Programmed firmware for ATMEGA32 microcontroller in **Embedded C** to implement a multi-feature alarm clock.
- Configured Timer1 (CTC mode, external crystal) for precise timekeeping.
- Integrated keypad and LCD via **GPIO** and **polling** to enhance UI responsiveness and reduce latency by 40%.