SAMA7D6 Series System-in-Package (SiP) MPUs with up to 4-Gbit DDR SDRAM

SAMA7D6 Series SiP Data Sheet

Product Page Links

Scope

This document provides an overview of the main features of the SAMA7D6 Series SiP microprocessors.

Reference documents for product information on the SAMA7D6 Series microprocessors and DDR2/DDR3L SDRAM memories are listed in the Reference Documents section.

Introduction

The SAMA7D6 Series SiP integrates the Arm® Cortex®-A7 processor-based SAMA7D6 Series MPU with up to 4-Gbit DDR SDRAM. By combining the SAMA7D6 with DDR SDRAM in a single package, PCB routing complexity, area and number of layers are reduced in most cases. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

The SAMA7D6 Series SiP is available in the following pin-to-pin compatible SDRAM memory types and densities:

- 512-Mbit DDR2 SDRAM
- 1-Gbit DDR3L SDRAM
- 2-Gbit DDR3L SDRAM
- 4-Gbit DDR3L SDRAM

Reference Documents

Type	Title	Available	Literature No.
Data sheet	SAMA7D6 Series	www.microchip.com	DS60001851
Errata sheet	SAMA7D6 Series Silicon Errata and Data Sheet Clarification	www.microchip.com	DS80001131
Application note	SAMA7D65 Hardware Design Considerations	www.microchip.com	AN5822
Data sheet	512-Mbit 8M × 4 BANKS × 16 BIT DDR2 SDRAM	www.winbond.com	W9751G6NB25I
Data sheet	1-Gbit 8M x 8 BANKS x 16 BIT DDR3L SDRAM	www.winbond.com	W631GU6NB12I
Data sheet	2-Gbit 16M x 8 BANKS x 16 BIT DDR3L SDRAM	www.winbond.com	W632GU6NB12I
Data sheet	4-Gbit 32M x 8 BANKS x 16 BIT DDR3L SDRAM	www.winbond.com	W634GU6NB12I

1. Features

- Arm Cortex-A7 Core
  - Arm TrustZone®
  - Arm® Neon™ multimedia architecture
  - Floating-Point Unit
  - Embedded Trace module with instruction trace stream, including 16 Kbytes of CoreSight™ Embedded Trace buffer
  - 32 Kbytes of L1 data cache, 32 Kbytes of L1 instruction cache
  - 256 Kbytes of L2 cache
  - Up to 1 GHz operational frequency
  - Voltage and frequency scaling support
  - 64-bit generic timers
- Memories
  - Internal memory architecture
    - 128 Kbytes of SRAM
    - 80 Kbytes of ROM, embedding a secure boot loader (boot on QSPI NOR, SLC/MLC NAND, SD card, e.MMC)
    - 96 Kbytes ROM for NAND Flash ECC tables
    - 40 Kbytes ROM for crypto libraries (RSA, ECC, etc.)
    - 11 Kbytes of internal OTP
    - 16-bit high-bandwidth DDR2 or DDR3L SDRAM up to 533 MHz and up to 4 Gbits
  - External memory support
    - 16-bit static memory controller, FPGA and memory-mapped peripheral support with synchronous clock
- System
  - Power-on reset cells, reset controller, shutdown controller, Watchdog and secure Watchdog Timers running on internal slow RC oscillator (32 kHz typical) and real-time clock running on slow crystal oscillator (32.768 kHz)
  - Two internal trimmed RC oscillators with typical values: 32 kHz and 12 MHz
  - Two crystal oscillators: 32.768 kHz and 20 to 50 MHz
  - Nine PLLs for core, system bus and peripherals, serial interfaces, DDR I/Os, pixel clock, audio, USB and Ethernet
  - Two 32-channel DMAs with per-channel security configuration
  - One 8-channel DMA dedicated to memory-to-memory transactions
  - Eight programmable clock output signals
- Power Considerations
  - Different power domains and power modes to reduce power consumption
  - Low-power consumption in Backup mode with 5 Kbytes of secure backup SRAM and DDR SDRAM in Self-Refresh mode
  - Low-power with SRAM and register retention, wake-up from various events (USB, CAN, Ethernet WOL, FLEXCOMs), internal events (RTC, timer) and I/O activity
  - Embedded LDOs for analog and PLLs to enable low-cost power management solutions

  - Optimum connection to Microchip MCP16501/2 PMICs to enter and exit various power modes of the application

- Multimedia Peripherals
  - Audio
    - Two synchronous serial controllers, each with up to eight channels of up to 32-bit TDM data
    - Two inter-IC sound multi-channel controllers with TDM256 support
    - Up to two 4-channel pulse density microphone controllers; support for eight microphones in parallel
    - One Sony/Philips digital interface transmitter and receiver
    - Audio sample rate converter including four stereo channels
- Display Subsystem Supporting One Display Up to WXGA/720p (1366x768p60/1280x720p60)
  - One 4-lane MIPI D-PHY interface and one DSI controller
  - One single-channel LVDS interface, and one LVDS controller
  - 8-bit databus serial RGB interface
  - One LCD controller with one base layer, one overlay and one high-end overlay
  - One 2D GPU controller with up to WXGA/720p target display resolution and support for RGB and YUV
- Connectivity
  - USB Subsystem:
    - Two high-speed USB devices and three high-speed USB hosts sharing three on-chip transceivers
    - Two USB Type-C™ controllers (TCPC)
  - Two 10/100/1000 Gigabit Ethernet MACs supporting:
    - RGMII and RMII interfaces
    - Energy efficiency as per IEEE 802.3az
    - Ethernet AVB support with IEEE802.1AS timestamping
    - IEEE802.1Qav credit-based traffic shaping hardware support
    - IEEE1588 Precision Time Protocol
    - IEEE1588 Timestamp Unit with TSU timer comparison signal triggering a timer counter and available on a PIO line
    - Support for traffic scheduling and Time-Sensitive Networking (TSN/AVB)
    - Packet buffer support
  - Five flexible data rate CAN-FD controllers with SRAM-based mailboxes with time- and event-triggered transmission, flexible data rate, and a 32-bit timestamp unit
  - Eleven FLEXCOMs supporting U(S)ART, SPI, TWI/I2C with FIFOs
  - I3C controller interface supporting FM, FM+, SDR and HDR-DDR modes
- Mass Storage
  - One 8-bit high-speed memory card host with e.MMC 5.1 (HS400), SD3.0, SDR104 mode support
  - One 4-bit high-speed memory card host with e.MMC 5.1 (HS200), SD3.0, SDR104 mode support
  - One 4-bit high-speed memory card host with SD3.0, SDR104 mode support

  - One octal serial peripheral interface supporting high-speed DDR mode
  - One quad serial peripheral interface
  - 8-bit SLC and MLC NAND controller with up to 32-bit Error Correcting Code (ECC)
- General-Purpose Analog and Digital Peripherals
  - Six 64-bit periodic interval timers
  - Two three-channel 32-bit timer counters with PWM generation
  - One four-channel 16-bit PWM controller
  - One 19-channel, 12-bit, 1 Msps analog-to-digital converter
  - One analog comparator with four differential inputs
- Safety
  - Zero-power power-on reset cells
  - Main crystal monitor and clock failure detector with failsafe switchover to main RC oscillator
  - 32 kHz crystal monitor and clock failure detector with switch to internal 32 kHz RC
  - Integrity check monitor based on SHA256
  - One Watchdog Timer running on RC oscillator
  - Register write protection
- Security
  - TrustZone support
  - One secure TrustZone Watchdog Timer running on RC oscillator, providing protection against TrustZone starvation
  - Temperature, voltage and frequency monitoring (also applicable for safety purposes)
  - Secure backup SRAM
    - 5 Kbytes scrambled with non-imprinting support powered with VBAT or VDDIN33:
      - 1 Kbyte non-erasable on tamper detection
      - 4 Kbytes erasable on tamper detection
  - Four tamper pins for static or dynamic detection
    - Can be used as regular wake-up lines
  - 256-bit backup register, erasable on tamper detection (tamper pins or monitor outputs); time stamping of tamper events
  - Programmable OTP with bits available for user purposes
  - Configurable JTAG/SWD security (full debug, non-secure-only debug, no debug)
  - Two independent 128-bit AES on-the-fly encryption/decryption on DDR memory, SMC, QSPI0 and QSPI1, including automatic key load at start-up; separate key for secure and non-secure accesses (TZAESB)
  - Secure RTC
- Cryptography
  - Physically Unclonable Function with automatic key load to hardware encryption engines
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512) compliant with FIPS Publications 180-2
  - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197 specifications
  - TDES: Two-key or three-key algorithms, compliant with FIPS PUB 46-3 specifications
  - True random number generator with health tests compliant with NIST Special Publication 800-22 Tests Suite and FIPS PUB 140-2 and 140-3

  - Public Key Coprocessor (CPKCC) and associated Classical Public Key Cryptography Library (CPKCL) for RSA, DSA, ECC GF(2n), ECC GF(p) and associated library for RSA4096, ECC521

- I/O Ports
  - Up to 142 general-purpose I/Os
  - Fully programmable through Set/Clear registers
  - Multiplexing of up to eight peripheral functions per I/O line
  - Each I/O line can be assigned to a peripheral or used as a general-purpose I/O
  - Synchronous output, possibility to set or clear up to 32 I/O lines simultaneously in a single write
  - General-purpose analog and digital inputs are tolerant to positive and negative current injection
- Design for Low Electromagnetic Interference (EMI)
  - Slew rate controlled I/Os
  - DDR Phy with impedance-calibrated drivers
  - Programmable spread spectrum PLLs
  - Careful BGA power/ground ball assignment to provide optimum decoupling capacitors placement
- Microchip Recommended Power Management Integrated Circuits (PMICs)
  - MCP16502, 6-channel PMIC with I²C control interface; supports dynamic voltage scaling and processor Low-Power modes (BSR)
  - MCP16501, 4-channel PMIC optimized for compact PCB layout; supports processor Low-Power mode (BSR)
- Operating Conditions
  - Junction temperature range (T_J): -40°C to +105°C
- Package
  - 427-ball TFBGA 21x18 mm, 0.8 mm pitch

2. Ordering Information

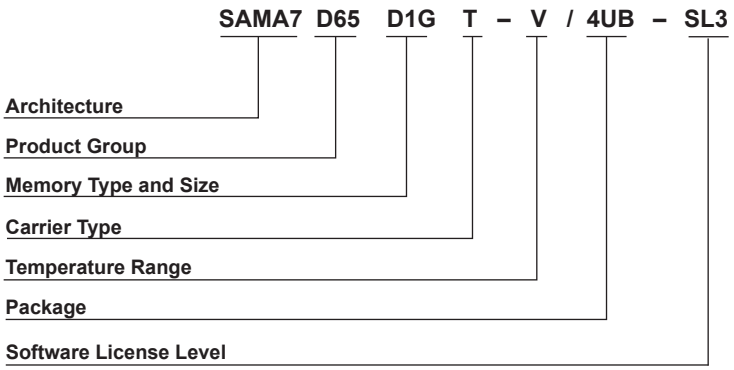
Ordering Code[1][2]	Memory Type	Tier	Max CPU Speed	Package	Junction Temperature Range[3]
SAMA7D65D5M(T)-V/4UB(-SLx)	DDR2 SDRAM	Industrial	1 GHz	TFBGA427	-40°C to +105°C
SAMA7D65D1G(T)-V/4UB(-SLx)	DDR3L SDRAM				
SAMA7D65D2G(T)-V/4UB(-SLx)					
SAMA7D65D4G(T)-V/4UB(-SLx)					

Notes:

1. For details on ordering codes, see Product Identification System.
2. For SL1, SL2 and SL3 device availability, contact a Microchip Sales representative.
3. Applies to both the MPU and the DDR memory junction temperatures.

3. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Architecture:	SAMA7	= Arm Cortex-A7 CPU
Product Group:	D65	= General-purpose microprocessors with graphic features
Memory Type and Size:	D5M	= 512-Mbit DDR2 SDRAM
	D1G	= 1-Gbit DDR3L SDRAM
	D2G	= 2-Gbit DDR3L SDRAM
	D4G	= 4-Gbit DDR3L SDRAM
Carrier Type:	Blank	= Standard packaging (tray)
	T	= Tape and Reel
Temperature Range (Junction):	V	= –40°C to +105°C (industrial)
Package:	4UB	= TFBGA427
Software License Level:	Blank	= Standard
	SL1	= Level 1
	SL2	= Level 2
	SL3	= Level 3

Example:

- SAMA7D65D1GT–V/4UB-SL3 = Arm Cortex-A7 general-purpose microprocessor, 1-Gbit DDR3L SDRAM, tape and reel packaging, industrial temperature, 427-ball TFBGA, software license level 3

Note: The Tape and Reel identifier and the Software License Level identifier only appear in the catalog part number description. These identifiers are used for ordering purposes and are not printed on the device package. Check with your Microchip Sales Office for package availability.

4. DDR2 SDRAM Features

The SAMA7D6 Series SiP is available with a 512-Mbit DDR2 SDRAM memory option.

For power consumption, electrical characteristics and memory timings, refer to the manufacturer's documentation listed in the Reference Documents section.

- Power supply: DDRM_VDD = 1.8V ±0.1V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS latency: 3
- Burst length: 8
- Bidirectional, differential data strobes (DQS and DQSN) are transmitted/received with data
- Edge-aligned with read data and center-aligned with write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLKN)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge; data and data mask referenced to both edges of DQS
- Auto-Refresh and Self-Refresh modes
- Precharged power-down and active power-down
- Write data mask
- Write latency = read latency - 1 (WL = RL - 1)

5. DDR3L SDRAM Features

The SAMA7D6 Series SiP is available with 1-Gbit, 2-Gbit or 4-Gbit DDR3L SDRAM memory options. For power consumption, electrical characteristics and timings of these memories, refer to the manufacturers' data sheets listed in the Reference Documents section.

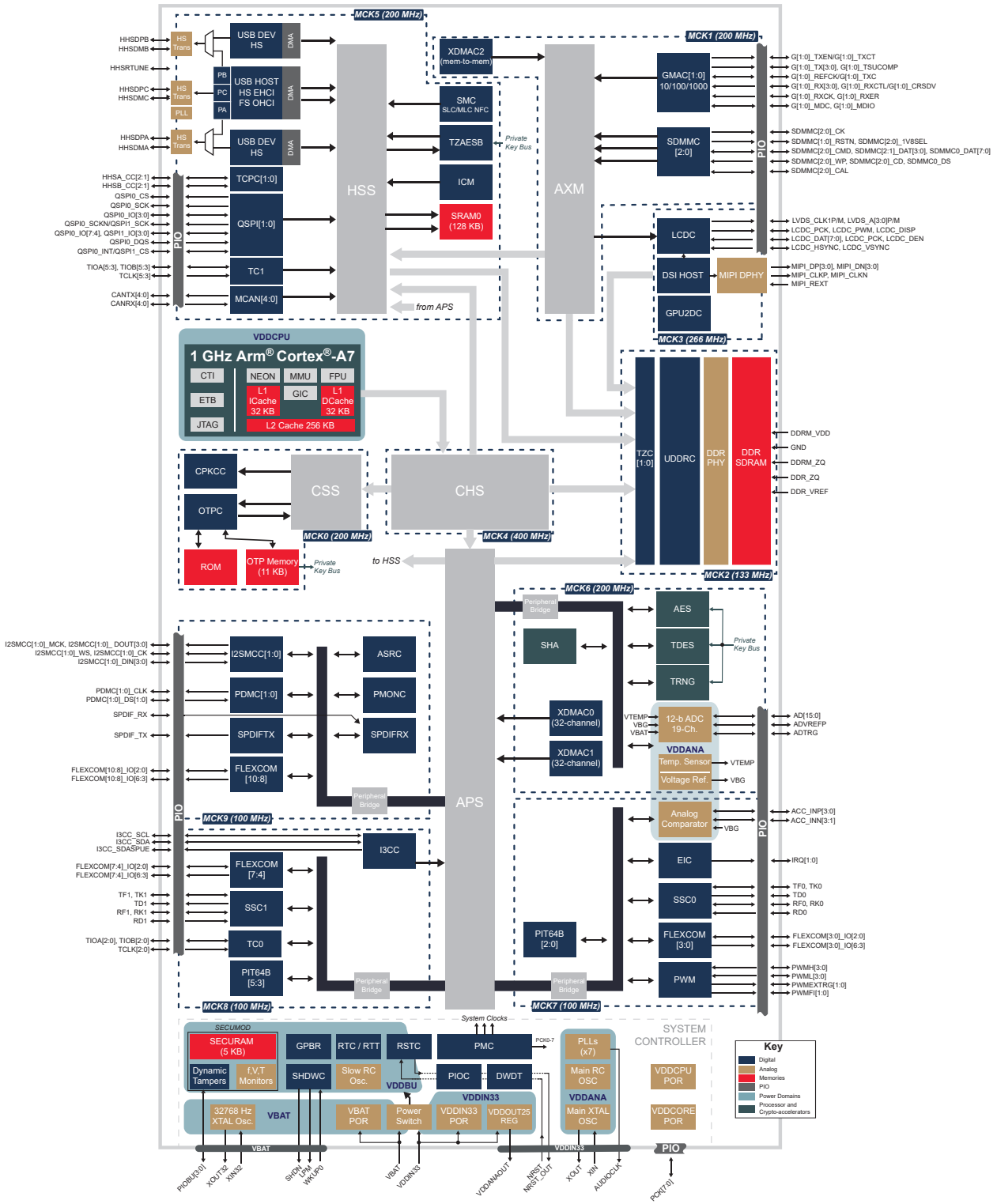
- Power supply: DDR3L DDRM_VDD = 1.283V to 1.45V
- 2-Kbyte page size (x16)
- 8-bank operation controlled by BA0, BA1 and BA2
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Precharge: auto-precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Average refresh period:
  - 7.8 µs at -40°C ≤ T_J ≤ +85°C
  - 3.9 µs at +85°C < T_J ≤ +95°C
  - 1.95 µs at +95°C < T_J ≤ +105°C
- High-speed data transfer realized by the 8-bit prefetch pipelined architecture
- Double Data Rate architecture: two data transfers per clock cycle
- Bidirectional differential data strobe (DQS and /DQS) transmitted/received with data for capturing data at the receiver
- DQS edge-aligned with data for reads and center-aligned with data for writes
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for improved command and databus efficiency
- MultiPurpose Register (MPR) for predefined pattern readout
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- Reset pin for power-up sequence and reset function
- Self-Refresh Temperature (SRT) range: normal/extended
- Automatic Self-Refresh (ASR)
- Programmable output driver impedance control

6. Configuration Summary

Feature	SAMA7D65D5M	SAMA7D65D1G	SAMA7D65D2G	SAMA7D65D4G
CPU	Cortex-A7 up to 1 GHz			
Package	427-ball TFBGA, 0.8mm pitch, 21 x 18 x 1.2 mm			
Internal SDRAM (16-bit, 533 MHz)	512-Mbit DDR2 SDRAM	1-Gbit DDR3L SDRAM	2-Gbit DDR3L SDRAM	4-Gbit DDR3L SDRAM
NAND Flash Controller	8-bit			
Ethernet MAC with TSN support	2x 10/100/1000 with RMII/RGMII I/F			
USB Device/Host	3 USB interfaces: 2 host/device with Type-C interface and 1 host			
2D GPU	One controller to accelerate 2D graphic display			
LCD	1 up to WXGA/720p resolution, single-channel LVDS, 4-lane MIPI DSI® Support of 8-bit serial RGB interface			
Number of PIOs	142			
Quad/Octal SPI	2 quad SPI or 1 octal SPI			
SDIO/SD/e.MMC	3			
SMC	16-bit data/15-bit address/2 CS			
CAN-FD	5			
FLEXCOM (USART/UART/I²C/SPI)	11			
I3C	1 controller			
ADC Inputs	16 external + 3 internal			
ACC Inputs	4 external			
64-bit Periodic Interval Timer	6			
Timer Counter	6 channels			
PWM	4 channels			
ASRC	4x stereo channels with independent conversion rates			
I2SMCC	2 (up to 8 TX and 8 RX channels each)			
SSC	2 (up to 16 TX and 16 RX channels each)			
PDMC	2 (up to 8 digital microphones)			
Cryptography	Asymmetric cryptography (CPKCC+CPKCL), AES, SHA, TRNG, TDES, PUF			

7. Block Diagram

Figure 7-1. SAMA7D6 Series SiP Block Diagram



8. Chip Identifier

Table 8-1. Chip ID and Extended ID Definition

Chip Name	CHIPID_CIDR	CHIPID_EXID(1)
SAMA7D65D5M	0x8026211x	0x00000010 0x000000C8 (SL1) 0x000000C9 (SL2) 0x000000CA (SL3)
SAMA7D65D1G		0x00000018 0x000000CC (SL1) 0x000000CD (SL2) 0x000000CE (SL3)
SAMA7D65D2G		0x00000020 0x000000D0 (SL1) 0x000000D1 (SL2) 0x000000D2 (SL3)
SAMA7D65D4G		0x00000028 0x000000D4 (SL1) 0x000000D5 (SL2) 0x000000D6 (SL3)

Note:

1. For more information, refer to Product Identification System.

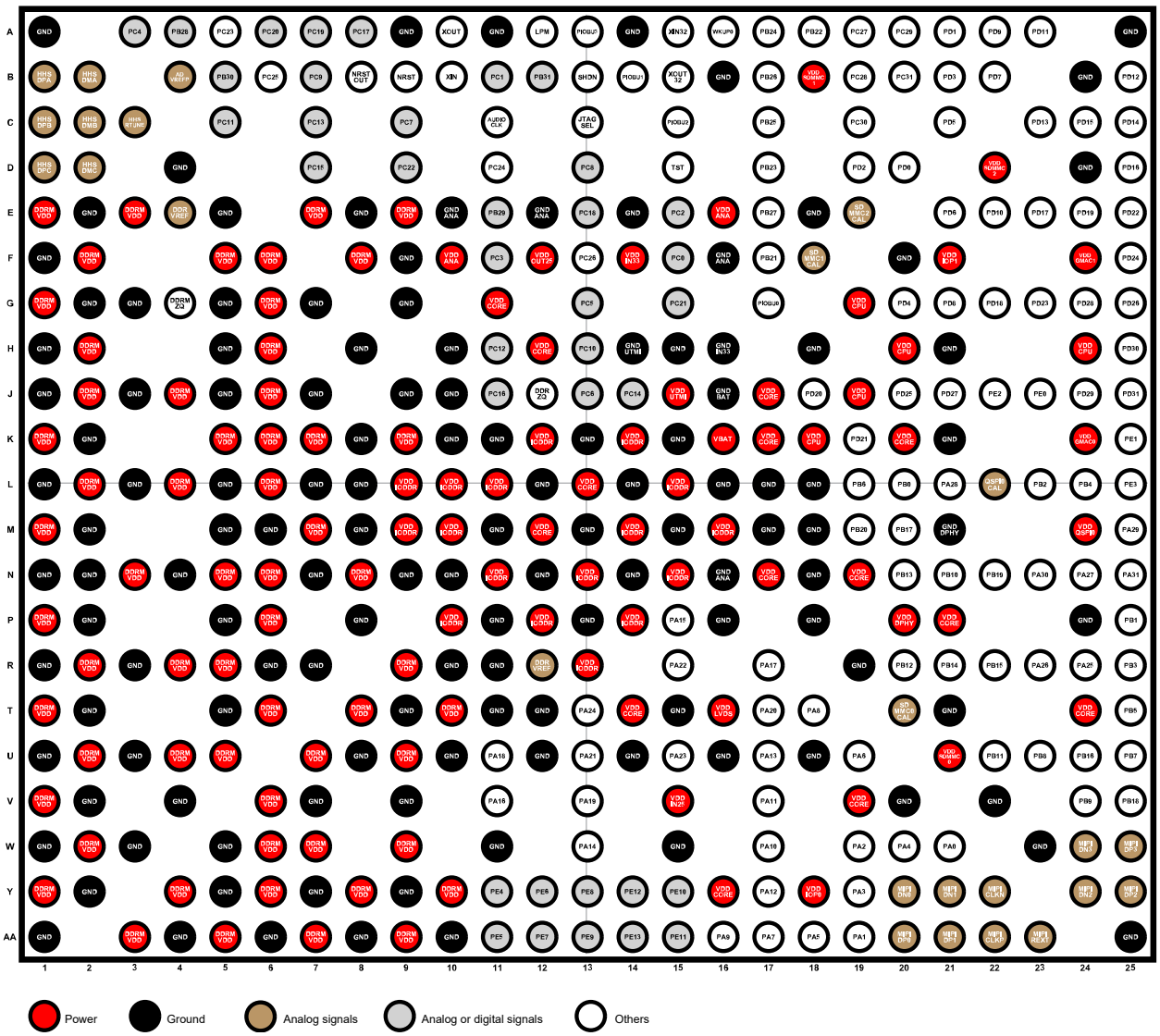
9. Package and Pinout

All SAMA7D6 Series SiP devices are pin-to-pin compatible.

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA427	427	0.8 mm	21 x 18 x 1.2 mm

9.1. TFBGA427 Package

Figure 9-1. 427-Ball TFBGA Pinout



9.2. Pin Description

The device features several PIO controllers that multiplex the I/O lines of the peripheral set. Table 9-1 defines how the I/O lines are multiplexed on the different PIO controllers. The "Reset State" column shows whether the PIO line resets in I/O mode or in Peripheral mode. If I/O is shown, the PIO line resets with the characteristics (input, output, pull-up or pull-down) indicated in this same column, so that the device is configured in a known state as soon as the reset is released. As a result, PIO_CFGR.FUNC resets to '0'. If a signal name is shown in the "Reset State" column, the PIO line is assigned to this function and PIO_CFGR.FUNC is not set to '0'. That is the case for pins controlling memories, in particular address lines, which require the pin to be driven as soon as the reset is released.

Table 9-1. Pin Description[1][2]

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
W21	VDDSDMMC0	HSIO	PA0	I/O	–	–	A	SDMMC0_CK	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	1	
							C	NWE/NWR0/ NANDWE	O	1	
AA19	VDDSDMMC0	HSIO	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	1	
							C	A21/NANDALE	O	1,2	
W19	VDDSDMMC0	HSIO	PA2	I/O	–	–	A	SDMMC0_RSTN	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	1	
							C	A22/NANDCLE	O	1,2	
Y19	VDDSDMMC0	HSIO	PA3	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO3	I/O	1	
							C	D0	I/O	1	
W20	VDDSDMMC0	HSIO	PA4	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO4	O	1	
							C	D1	I/O	1	
AA18	VDDSDMMC0	HSIO	PA5	I/O	–	–	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO0	I/O	3	
							C	D4	I/O	1	
							F	TCLK4	I	3	
U19	VDDSDMMC0	HSIO	PA6	I/O	–	–	A	SDMMC0_DAT5	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO1	I/O	3	
							C	D5	I/O	1	
							F	TIOB4	I/O	3	
AA17	VDDSDMMC0	HSIO	PA7	I/O	–	–	A	SDMMC0_DAT6	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO2	I/O	3	
							C	D6	I/O	1	
							F	TIOA4	I/O	3	
T18	VDDSDMMC0	HSIO	PA8	I/O	–	–	A	SDMMC0_DAT7	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO3	I/O	3	
							C	D7	I/O	1	
							F	TIOA5	I/O	3	
AA16	VDDSDMMC0	HSIO	PA9	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO2	I/O	1	
							C	D2	I/O	1	
							F	TIOB5	I/O	3	
W17	VDDSDMMC0	HSIO	PA10	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO3	I/O	1	
							C	D3	I/O	1	
							F	TCLK5	I	3	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
V17	VDDSDMMC0	HSIO	PA11	I/O	–	–	A	SDMMC0_DS	I	1	PIO, I, PU, ST
							B	FLEXCOM0_IO4	O	1	
							C	NANDRDY	I	1,2	
							F	TIOB3	I/O	3	
Y17	VDDSDMMC0	HSIO	PA12	I/O	–	–	B	FLEXCOM0_IO0	I/O	1	PIO, I, PU, ST
							C	NRD/NANDOE	O	1,2	
							D	PCK0	O	1	
							E	EXT_IRQ0	I	1	
							F	TIOA3	I/O	3	
U17	VDDSDMMC0	HSIO	PA13	I/O	–	–	B	FLEXCOM0_IO1	I/O	1	PIO, I, PU, ST
							C	NCS0/NANDCS0	O	1,2	
							D	PCK1	O	1	
							F	TCLK3	I	3	
W13	VDDIOP0	GPIO	PA14	I/O	–	–	A	FLEXCOM4_IO4	O	1	PIO, I, PU, ST
							B	SDMMC0_WP	I	1	
							C	FLEXCOM3_IO0	I/O	4	
P15	VDDIOP0	GPIO	PA15	I/O	–	–	A	FLEXCOM4_IO3	I/O	1	PIO, I, PU, ST
							B	SDMMC0_1V8SEL	O	1	
							C	FLEXCOM3_IO1	I/O	4	
V11	VDDIOP0	GPIO	PA16	I/O	–	–	A	FLEXCOM4_IO2	I/O	1	PIO, I, PU, ST
							B	SDMMC0_CD	I	1	
							D	PCK2	O	1	
							E	EXT_IRQ1	I	1	
R17	VDDIOP0	GPIO	PA17	I/O	–	–	A	FLEXCOM4_IO1	I/O	1	PIO, I, PU, ST
U11	VDDIOP0	GPIO	PA18	I/O	–	–	A	FLEXCOM4_IO0	I/O	1	PIO, I, PU, ST
V13	VDDIOP0	GPIO	PA19	I/O	–	–	A	TK0	I/O	1	PIO, I, PU, ST
							C	FLEXCOM4_IO5	O	1	
							D	PWML0	O	3	
T17	VDDIOP0	GPIO	PA20	I/O	–	–	A	TD0	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO4	O	2	
							C	FLEXCOM4_IO6	O	1	
							D	PWMH0	O	3	
U13	VDDIOP0	GPIO	PA21	I/O	–	–	A	TF0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO3	I/O	2	
							D	PWML1	O	3	
R15	VDDIOP0	GPIO	PA22	I/O	–	–	A	RD0	I	1	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	2	
							C	PDMC0_DS1	I	1	
							D	PWMH1	O	3	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
U15	VDDIOP0	GPIO	PA23	I/O	–	–	A	RK0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	2	
							C	PDMC0_CLK	O	1	
							D	PWML2	O	3	
T13	VDDIOP0	GPIO	PA24	I/O	–	–	A	RF0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	2	
							C	PDMC0_DS0	I	1	
							D	PWMH2	O	3	
R24	VDDGMAC0	GPIO	PA25	I/O	–	–	A	G0_TXCTL/ G0_TXEN	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO2	I/O	1	
R23	VDDGMAC0	GPIO	PA26	I/O	–	–	A	G0_TX0	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO3	I/O	1	
N24	VDDGMAC0	GPIO	PA27	I/O	–	–	A	G0_TX1	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO4	O	1	
L21	VDDGMAC0	GPIO	PA28	I/O	–	–	A	G0_RXCTL/ G0_CRSDV	I	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO0	I/O	1	
M25	VDDGMAC0	GPIO	PA29	I/O	–	–	A	G0_RX0	I	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO1	I/O	1	
N23	VDDGMAC0	GPIO	PA30	I/O	–	–	A	G0_RX1	I	1,2	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	1	
N25	VDDGMAC0	GPIO	PA31	I/O	–	–	A	G0_MDC	O	1,2	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	1	
L20	VDDGMAC0	GPIO	PB0	I/O	–	–	A	G0_MDIO	I/O	1,2	PIO, I, PU, ST
							B	FLEXCOM8_IO3	I/O	1	
P25	VDDGMAC0	GPIO	PB1	I/O	–	–	A	G0_REFCK/ G0_TXCK	I/O	2,1	PIO, I, PU, ST
							B	FLEXCOM8_IO2	I/O	1	
L23	VDDGMAC0	GPIO	PB2	I/O	–	–	A	G0_RX2	I	1	PIO, I, PU, ST
							B	FLEXCOM8_IO4	O	1	
							C	G0_RXER	I	2	
							D	RK0	I/O	2	
R25	VDDGMAC0	GPIO	PB3	I/O	–	–	A	G0_RXCK	I	1	PIO, I, PU, ST
							B	FLEXCOM10_IO2	I/O	2	
							D	TK0	I/O	2	
L24	VDDGMAC0	GPIO	PB4	I/O	–	–	A	G0_TX2	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO3	I/O	2	
							D	TF0	I/O	2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
T25	VDDGMAC0	GPIO	PB5	I/O	–	–	A	G0_TX3	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO4	O	2	
							D	TD0	O	2	
L19	VDDGMAC0	GPIO	PB6	I/O	–	–	A	G0_RX3	I	1	PIO, I, PU, ST
							B	FLEXCOM10_IO0	I/O	2	
							D	RD0	I	2	
U25	VDDGMAC0	GPIO	PB7	I/O	–	–	A	G0_TSUCOMP	O	1,2	PIO, I, PU, ST
							B	FLEXCOM10_IO1	I/O	2	
							C	ADTRG	I	1	
							D	RF0	I/O	2	
U23	VDDQSPI0	HSIO	PB8	I/O	–	–	A	QSPI0_IO3	I/O	1	PIO, I, PU, ST
							B	PCK3	O	1	
							D	FLEXCOM2_IO1	I/O	2	
V24	VDDQSPI0	HSIO	PB9	I/O	–	–	A	QSPI0_IO2	I/O	1	PIO, I, PU, ST
							D	FLEXCOM2_IO0	I/O	2	
							E	PWMEXTRG0	I	1	
N21	VDDQSPI0	HSIO	PB10	I/O	–	–	A	QSPI0_IO1	I/O	1	PIO, I, PU, ST
							D	FLEXCOM2_IO4	O	2	
							E	PWMEXTRG1	I	1	
U22	VDDQSPI0	HSIO	PB11	I/O	–	–	A	QSPI0_IO0	I/O	1	PIO, I, PU, ST
							D	FLEXCOM2_IO5	O	2	
							E	PWML3	O	1	
							F	TIOB3	I/O	2	
R20	VDDQSPI0	HSIO	PB12	I/O	–	–	A	QSPI0_CS	O	1	PIO, I, PU, ST
							D	FLEXCOM2_IO3	I/O	2	
							E	PWMFI1	I	1	
							F	TIOA3	I/O	2	
N20	VDDQSPI0	HSIO	PB13	I/O	–	–	A	QSPI0_SCK	O	1	PIO, I, PU, ST
							D	FLEXCOM2_IO2	I/O	2	
							E	PWMFI0	I	1	
							F	TCLK3	I	2	
R21	VDDQSPI0	HSIO	PB14	I/O	–	–	A	QSPI0_SCKN	O	1	PIO, I, PU, ST
							B	QSPI1_SCK	O	1	
							C	I2SMCC0_CK	I/O	3	
							D	FLEXCOM10_IO5	O	1	
							E	PWMH3	O	1	
							G	FLEXCOM2_IO1	I/O	4	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
R22	VDDQSPI0	HSIO	PB15	I/O	–	–	A	QSPI0_IO4	I/O	1	PIO, I, PU, ST
							B	QSPI1_IO0	I/O	1	
							C	I2SMCC0_WS	I/O	3	
							D	FLEXCOM10_IO6	O	1	
							E	PWML0	O	1	
							F	TCLK4	I	2	
							G	FLEXCOM2_IO0	I/O	4	
U24	VDDQSPI0	HSIO	PB16	I/O	–	–	A	QSPI0_IO5	I/O	1	PIO, I, PU, ST
							B	QSPI1_IO1	I/O	1	
							C	I2SMCC0_DIN0	I	3	
							D	FLEXCOM10_IO4	O	1	
							E	PWMH0	O	1	
							F	TIOB4	I/O	2	
M20	VDDQSPI0	HSIO	PB17	I/O	–	–	A	QSPI0_IO6	I/O	1	PIO, I, PU, ST
							B	QSPI1_IO2	I/O	1	
							C	I2SMCC0_DOUT0	O	3	
							D	FLEXCOM10_IO3	I/O	1	
							E	PWML1	O	1	
							F	TIOA4	I/O	2	
V25	VDDQSPI0	HSIO	PB18	I/O	–	–	A	QSPI0_IO7	I/O	1	PIO, I, PU, ST
							B	QSPI1_IO3	I/O	1	
							C	I2SMCC0_MCK	O	3	
							D	FLEXCOM10_IO2	I/O	1	
							E	PWMH1	O	1	
							F	TIOA5	I/O	2	
N22	VDDQSPI0	HSIO	PB19	I/O	–	–	A	QSPI0_DQS	I	1	PIO, I, PU, ST
							B	EXT_IRQ1	I	2	
							C	PCK4	O	1	
							D	FLEXCOM10_IO1	I/O	1	
							E	PWML2	O	1	
							F	TIOB5	I/O	2	
M19	VDDQSPI0	HSIO	PB20	I/O	–	–	A	QSPI0_INT	I	1	PIO, I, PU, ST
							B	QSPI1_CS	O	1	
							D	FLEXCOM10_IO0	I/O	1	
							E	PWMH2	O	1	
							F	TCLK5	I	2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
F17	VDDSDMMC1	HSIO	PB21	I/O	–	–	A	SDMMC1_RSTN	O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO4	O	2	
							C	TIOB2	I/O	2	
							D	ADTRG	I	2	
							E	EXT_IRQ0	I	2	
A18	VDDSDMMC1	HSIO	PB22	I/O	–	–	A	SDMMC1_CMD	I/O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO3	I/O	2	
							C	TCLK2	I	2	
D17	VDDSDMMC1	HSIO	PB23	I/O	–	–	A	SDMMC1_CK	O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO2	I/O	2	
							C	TIOA2	I/O	2	
A17	VDDSDMMC1	HSIO	PB24	I/O	–	–	A	SDMMC1_DAT0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO0	I/O	2	
C17	VDDSDMMC1	HSIO	PB25	I/O	–	–	A	SDMMC1_DAT1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO1	I/O	2	
							C	TIOB2	I/O	1	
B17	VDDSDMMC1	HSIO	PB26	I/O	–	–	A	SDMMC1_DAT2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	3	
							C	TCLK2	I	1	
E17	VDDSDMMC1	HSIO	PB27	I/O	–	–	A	SDMMC1_DAT3	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	3	
							C	TIOA2	I/O	1	
A4	VDDIN33	GPIO	PB28	I/O	AD12	I	A	SDMMC1_WP	I	1	PIO, I, PU, ST
							C	FLEXCOM1_IO0	I/O	3	
							E	D15	I/O	1,2	
E11	VDDIN33	GPIO	PB29	I/O	AD13	I	A	SDMMC1_CD	I	1	PIO, I, PU, ST
							B	I2SMCC0_MCK	O	1	
							C	FLEXCOM1_IO1	I/O	3	
							E	D14	I/O	1,2	
B5	VDDIN33	GPIO	PB30	I/O	AD14	I	A	SDMMC1_1V8SEL	O	1	PIO, I, PU, ST
							B	I2SMCC1_MCK	O	1	
							C	FLEXCOM1_IO2	I/O	3	
							D	TIOA1	I/O	1	
							E	NCS1/NANDCS1	O	1,2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
B12	VDDIN33	GPIO	PB31	I/O	HHSA_CC1	I/O	A	PCK7	O	2	PIO, I, PU, ST
							B	I2SMCC1_DIN1	I	1	
							C	FLEXCOM1_IO3	I/O	3	
							D	TCLK1	I	1	
							E	NWE/NWR0/ NANDWE	O	2	
F15	VDDIN33	GPIO	PC0	I/O	HHSA_CC2	I/O	A	PCK6	O	2	PIO, I, PU, ST
							B	I2SMCC1_DIN2	I	1	
							C	FLEXCOM9_IO4	O	2	
							D	TIOB1	I/O	1	
							E	NWR1/NBS1	O	1,2	
B11	VDDIN33	GPIO	PC1	I/O	HHSB_CC1	I/O	A	PCK5	O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO2	I/O	2	
							E	SMCK	O	1,2	
E15	VDDIN33	GPIO	PC2	I/O	HHSB_CC2	I/O	A	EXT_IRQ0	I	3	PIO, I, PU, ST
							C	FLEXCOM9_IO3	I/O	2	
							E	A11	O	1,2	
F11	VDDIN33	GPIO	PC3	I/O	AD0	I	A	SPDIF_RX	I	2	PIO, I, PU, ST
							C	FLEXCOM9_IO0	I/O	2	
							D	FLEXCOM0_IO4	O	2	
							E	A10	O	1,2	
A3	VDDIN33	GPIO	PC4	I/O	AD1	I	A	SPDIF_TX	O	2	PIO, I, PU, ST
							C	FLEXCOM9_IO1	I/O	2	
							D	FLEXCOM0_IO3	I/O	2	
							E	D0	I/O	2	
G13	VDDIN33	GPIO	PC5	I/O	AD2	I	A	I3CC_SDASPUE	O	1	PIO, I, PU, ST
							B	I2SMCC1_DIN3	I	1	
							D	FLEXCOM0_IO2	I/O	2	
							E	D1	I/O	2	
J13	VDDIN33	GPIO	PC6	I/O	AD3	I	A	I3CC_SCL	I/O	1	PIO, I, PU, ST
							D	FLEXCOM0_IO1	I/O	2	
							E	D4	I/O	2	
C9	VDDIN33	GPIO	PC7	I/O	AD4	I/O	A	I3CC_SDA	I/O	1	PIO, I, PU, ST
							D	FLEXCOM0_IO0	I/O	2	
							E	D5	I/O	2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
D13	VDDIN33	GPIO	PC8	I/O	ACC_INP1	I	A	I2SMCC0_DIN1	I	1	PIO, I, PU, ST
							B	PDMC0_DS1	I	2	
							C	I2SMCC1_DOUT1	O	1	
							D	FLEXCOM9_IO0	I/O	1	
							E	D6	I/O	2	
B7	VDDIN33	GPIO	PC9	I/O	ACC_INN1	I	A	I2SMCC0_DIN2	I	1	PIO, I, PU, ST
							B	PDMC0_CLK	O	2	
							C	I2SMCC1_DOUT2	O	1	
							D	FLEXCOM9_IO1	I/O	1	
							E	D7	I/O	2	
H13	VDDIN33	GPIO	PC10	I/O	AD5	I/O	A	I2SMCC0_DIN3	I	1	PIO, I, PU, ST
							B	PDMC0_DS0	I	2	
							C	I2SMCC1_DOUT3	O	1	
							D	FLEXCOM9_IO2	I/O	1	
							E	D2	I/O	2	
C5	VDDIN33	GPIO	PC11	I/O	AD6	I	A	I2SMCC0_DOUT1	O	1	PIO, I, PU, ST
							B	PDMC1_DS0	I	1	
							D	FLEXCOM9_IO3	I/O	1	
							E	D3	I/O	2	
H11	VDDIN33	GPIO	PC12	I/O	AD7	I	A	I2SMCC0_DOUT2	O	1	PIO, I, PU, ST
							B	PDMC1_CLK	O	1	
							D	FLEXCOM9_IO4	O	1	
							E	A9	O	1,2	
C7	VDDIN33	GPIO	PC13	I/O	AD8	I	A	I2SMCC0_DOUT3	O	1	PIO, I, PD, ST
							B	PDMC1_DS1	I	1	
							E	A8	O	1,2	
J14	VDDIN33	GPIO	PC14	I/O	AD9	I	A	I2SMCC1_DIN0	I	1	PIO, I, PD, ST
							B	SPDIF_RX	I	3	
							C	FLEXCOM1_IO0	I/O	2	
							E	A7	O	1,2	
D7	VDDIN33	GPIO	PC15	I/O	AD10	I	A	I2SMCC1_WS	I/O	1	PIO, I, PD, ST
							B	PDMC1_DS1	I	2	
							C	FLEXCOM1_IO1	I/O	2	
							E	A6	O	1,2	
J11	VDDIN33	GPIO	PC16	I/O	AD11	I	A	I2SMCC1_CK	I/O	1	PIO, I, PD, ST
							B	PDMC1_CLK	O	2	
							C	FLEXCOM1_IO2	I/O	2	
							D	TIOA1	I/O	2	
							E	A5	O	1,2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
A8	VDDIN33	GPIO	PC17	I/O	ACC_INP0	I	A	I2SMCC1_DOUT0	O	1	PIO, I, PU, ST
							B	PDMC1_DS0	I	2	
							C	FLEXCOM1_IO3	I/O	2	
							D	TCLK1	I	2	
							E	A4	O	1,2	
E13	VDDIN33	GPIO	PC18	I/O	ACC_INN2	I	A	I2SMCC0_DIN0	I	1	PIO, I, PU, ST
							B	SPDIF_TX	O	3	
							C	FLEXCOM1_IO4	O	2	
							D	TIOB1	I/O	2	
							E	A3	O	1,2	
A7	VDDIN33	GPIO	PC19	I/O	ACC_INP2	I	A	I2SMCC0_WS	I/O	1	PIO, I, PU, ST
							B	PCK6	O	1	
							E	A2	O	1,2	
A6	VDDIN33	GPIO	PC20	I/O	ACC_INN3	–	A	I2SMCC0_DOUT0	O	1	PIO, I, PU, ST
							E	A1	O	1,2	
G15	VDDIN33	GPIO	PC21	I/O	ACC_INP3	–	A	I2SMCC0_CK	I/O	1	PIO, I, PU, ST
							B	PCK7	O	1	
							E	A0/NBS0	O	1,2	
D9	VDDIN33	GPIO	PC22	I/O	AD15	–	A	NTRST	I	1	NTRST, PU, ST
							E	NWAIT	I	1,2	
A5	VDDIN33	GPIO	PC23	I/O	–	–	A	TCK_SWCLK	I	1	TCK_SWCLK, ST
D11	VDDIN33	GPIO	PC24	I/O	–	–	A	TMS_SWDIO	I/O	1	TMS_SWDIO, PU, ST
B6	VDDIN33	GPIO	PC25	I/O	–	–	A	TDI	I	1	TDI, PU, ST
F13	VDDIN33	GPIO	PC26	I/O	–	–	A	TDO	O	1	TDO, ST
							E	A12	O	1,2	
A19	VDDSDMMC2	HSIO	PC27	I/O	–	–	A	SDMMC2_CMD	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	2	
							D	TD1	O	2	
							E	D8	I/O	1,2	
B19	VDDSDMMC2	HSIO	PC28	I/O	–	–	A	SDMMC2_CK	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	2	
							D	TF1	I/O	2	
							E	D9	I/O	1,2	
A20	VDDSDMMC2	HSIO	PC29	I/O	–	–	A	SDMMC2_DAT0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO2	I/O	2	
							D	TK1	I/O	2	
							E	D10	I/O	1,2	
							F	TCLK0	I	1	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
C19	VDDSDMMC2	HSIO	PC30	I/O	–	–	A	SDMMC2_DAT1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO3	I/O	2	
							D	RD1	I	2	
							E	D11	I/O	1,2	
							F	TIOA0	I/O	1	
B20	VDDSDMMC2	HSIO	PC31	I/O	–	–	A	SDMMC2_DAT2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO4	O	2	
							C	PCK0	O	2	
							D	RK1	I/O	2	
							E	D12	I/O	1,2	
							F	TIOB0	I/O	1	
D20	VDDSDMMC2	HSIO	PD0	I/O	–	–	A	SDMMC2_DAT3	I/O	1	PIO, I, PU, ST
							C	PCK1	O	2	
							D	RF1	I/O	2	
							E	D13	I/O	1,2	
A21	VDDIOP1	GPIO	PD1	I/O	–	–	A	SDMMC2_WP	I	1	PIO, I, PU, ST
							B	FLEXCOM1_IO5	O	1	
							C	LCDC_HSYNC	O	2	
							D	FLEXCOM3_IO0	I/O	3	
D19	VDDIOP1	GPIO	PD2	I/O	–	–	A	SDMMC2_CD	I	1	PIO, I, PU, ST
							B	FLEXCOM1_IO6	O	1	
							C	LCDC_VSYNC	O	2	
							D	FLEXCOM3_IO1	I/O	3	
B21	VDDIOP1	GPIO	PD3	I/O	–	–	A	SDMMC2_1V8SEL	O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO4	O	1	
							C	TIOA0	I/O	2	
							D	FLEXCOM3_IO2	I/O	3	
							E	EXT_IRQ1	I	3	
G20	VDDIOP1	GPIO	PD4	I/O	–	–	A	LCDC_HSYNC	O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO2	I/O	1	
							C	TIOB0	I/O	2	
							D	FLEXCOM7_IO1	I/O	3	
C21	VDDIOP1	GPIO	PD5	I/O	–	–	A	LCDC_VSYNC	O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO3	I/O	1	
							C	TCLK0	I	2	
							D	FLEXCOM7_IO0	I/O	3	
E21	VDDIOP1	GPIO	PD6	I/O	–	–	A	LCDC_PWM	O	1,2	PIO, I, PU, ST
							B	FLEXCOM1_IO1	I/O	1	
							D	FLEXCOM7_IO2	I/O	3	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
B22	VDDIOP1	GPIO	PD7	I/O	–	–	A	LCDC_DISP	O	1,2	PIO, I, PU, ST
							B	FLEXCOM1_IO0	I/O	1	
							D	FLEXCOM7_IO3	I/O	3	
G21	VDDIOP1	GPIO	PD8	I/O	–	–	A	CANTX0	O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO0	I/O	1	
A22	VDDIOP1	GPIO	PD9	I/O	–	–	A	CANRX0	I	1	PIO, I, PU, ST
							B	FLEXCOM7_IO1	I/O	1	
E22	VDDIOP1	GPIO	PD10	I/O	–	–	A	CANTX1	O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO2	I/O	1	
							C	TIOA1	I/O	3	
A23	VDDIOP1	GPIO	PD11	I/O	–	–	A	CANRX1	I	1	PIO, I, PU, ST
							B	FLEXCOM7_IO3	I/O	1	
							C	TCLK1	I	3	
B25	VDDIOP1	GPIO	PD12	I/O	–	–	A	CANTX2	O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO4	O	1	
							C	TIOB1	I/O	3	
							D	PCK2	O	2	
							E	FLEXCOM3_IO3	I/O	3	
C23	VDDIOP1	GPIO	PD13	I/O	–	–	A	CANRX2	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO4	O	1	
							C	TIOA2	I/O	3	
							D	PCK3	O	2	
C25	VDDIOP1	GPIO	PD14	I/O	–	–	A	CANTX3	O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO2	I/O	1	
							C	TIOB2	I/O	3	
C24	VDDIOP1	GPIO	PD15	I/O	–	–	A	CANRX3	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO3	I/O	1	
							C	TCLK2	I	3	
D25	VDDIOP1	GPIO	PD16	I/O	–	–	A	CANTX4	O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO0	I/O	1	
E23	VDDIOP1	GPIO	PD17	I/O	–	–	A	CANRX4	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO1	I/O	1	
G22	VDDGMAC1	GPIO	PD18	I/O	–	–	B	FLEXCOM6_IO0	I/O	4	PIO, I, PU, ST
							C	CANTX1	O	2	
							D	PCK4	O	2	
E24	VDDGMAC1	GPIO	PD19	I/O	–	–	B	FLEXCOM6_IO1	I/O	4	PIO, I, PU, ST
							C	CANRX1	I	2	
							D	PCK2	O	3	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
J18	VDDGMAC1	GPIO	PD20	I/O	–	–	B	FLEXCOM6_IO2	I/O	4	PIO, I, PU, ST
							C	I2SMCC1_MCK	O	2	
							D	PCK3	O	3	
K19	VDDGMAC1	GPIO	PD21	I/O	–	–	A	G1_TXCTL/ G1_TXEN	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO2	I/O	3	
							C	TK1	I/O	1	
E25	VDDGMAC1	GPIO	PD22	I/O	–	–	A	G1_TX0	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO3	I/O	3,4	
							C	TF1	I/O	1	
G23	VDDGMAC1	GPIO	PD23	I/O	–	–	A	G1_TX1	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO4	O	3,4	
							C	TD1	O	1	
F25	VDDGMAC1	GPIO	PD24	I/O	–	–	A	G1_RXCTL/ G1_CRSDV	I	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO0	I/O	3	
							C	RD1	I	1	
							E	PDMC0_DS1	I	3	
J20	VDDGMAC1	GPIO	PD25	I/O	–	–	A	G1_MDC	O	1,2	PIO, I, PU, ST
							B	FLEXCOM6_IO1	I/O	3	
							C	RK1	I/O	1	
							E	PDMC0_CLK	O	3	
G25	VDDGMAC1	GPIO	PD26	I/O	–	–	A	G1_MDIO	I/O	1,2	PIO, I, PU, ST
							B	FLEXCOM7_IO4	O	2	
							C	RF1	I/O	1	
							D	I2SMCC1_DIN2	I	2	
							E	PDMC0_DS0	I	3	
J21	VDDGMAC1	GPIO	PD27	I/O	–	–	A	G1_RX0	I	1,2	PIO, I, PU, ST
							B	FLEXCOM7_IO0	I/O	2	
							C	SPDIF_RX	I	1	
							D	I2SMCC1_DIN3	I	2	
G24	VDDGMAC1	GPIO	PD28	I/O	–	–	A	G1_RX1	I	1,2	PIO, I, PU, ST
							B	FLEXCOM7_IO1	I/O	2	
							C	SPDIF_TX	O	1	
							D	I2SMCC1_DIN1	I	2	
J24	VDDGMAC1	GPIO	PD29	I/O	–	–	A	G1_REFCK/ G1_TXCK	I/O	2,1	PIO, I, PU, ST
							B	FLEXCOM7_IO2	I/O	2	
							C	I2SMCC1_DOUT3	O	2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
H25	VDDGMAC1	GPIO	PD30	I/O	–	–	A	G1_RX2	I	1	PIO, I, PU, ST
							B	FLEXCOM7_IO3	I/O	2	
							C	I2SMCC1_DOUT1	O	2	
							D	PDMC1_DS1	I	3	
							E	G1_RXER	I	2	
J25	VDDGMAC1	GPIO	PD31	I/O	–	–	A	G1_RX3	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO4	O	2	
							C	I2SMCC1_DOUT2	O	2	
							D	PDMC1_DS0	I	3	
J23	VDDGMAC1	GPIO	PE0	I/O	–	–	A	G1_TX2	O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO2	I/O	2	
							C	I2SMCC1_DIN0	I	2	
							D	PDMC1_CLK	O	3	
K25	VDDGMAC1	GPIO	PE1	I/O	–	–	A	G1_TX3	O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO3	I/O	2	
							C	I2SMCC1_WS	I/O	2	
							D	PDMC0_DS1	I	4	
J22	VDDGMAC1	GPIO	PE2	I/O	–	–	A	G1_RXCK	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO1	I/O	2	
							C	I2SMCC1_CK	I/O	2	
							D	PDMC0_CLK	O	4	
L25	VDDGMAC1	GPIO	PE3	I/O	–	–	A	G1_TSUCOMP	O	1,2	PIO, I, PU, ST
							B	FLEXCOM5_IO0	I/O	2	
							C	I2SMCC1_DOUT0	O	2	
							D	PDMC0_DS0	I	4	
Y11	VDDLVDS	GPIO	PE4	I/O	LVDS_A0M	O	A	LCDC_DAT0	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO2	I/O	1	
							C	PWML0	O	2	
							D	TIOA3	I/O	1	
							E	I2SMCC0_DIN1	I	2	
AA11	VDDLVDS	GPIO	PE5	I/O	LVDS_A0P	O	A	LCDC_DAT1	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO3	I/O	1	
							C	PWMH0	O	2	
							D	TIOB3	I/O	1	
							E	I2SMCC0_DIN2	I	2	

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
Y12	VDDLVDS	GPIO	PE6	I/O	LVDS_A1M	O	A	LCDC_DAT2	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO4	O	1	
							C	PWML1	O	2	
							D	TCLK3	I	1	
							E	I2SMCC0_DIN3	I	2	
AA12	VDDLVDS	GPIO	PE7	I/O	LVDS_A1P	O	A	LCDC_DAT3	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO5	O	1	
							C	PWMH1	O	2	
							D	TIOA4	I/O	1	
							E	I2SMCC0_DOUT1	O	2	
Y13	VDDLVDS	GPIO	PE8	I/O	LVDS_A2M	O	A	LCDC_DAT4	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO0	I/O	1	
							C	PWML2	O	2	
							D	TIOB4	I/O	1	
							E	I2SMCC0_CK	I/O	2	
AA13	VDDLVDS	GPIO	PE9	I/O	LVDS_A2P	O	A	LCDC_DAT5	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO1	I/O	1	
							C	PWMH2	O	2	
							D	TCLK4	I	1	
							E	I2SMCC0_WS	I/O	2	
Y15	VDDLVDS	GPIO	PE10	I/O	LVDS_A3M	O	A	LCDC_DAT6	O	1,2	PIO, I, PU, ST
							B	FLEXCOM2_IO6	O	1	
							C	PWML3	O	2	
							D	TIOA5	I/O	1	
							E	I2SMCC0_DOUT2	O	2	
AA15	VDDLVDS	GPIO	PE11	I/O	LVDS_A3P	O	A	LCDC_DAT7	O	1,2	PIO, I, PU, ST
							C	PWMH3	O	2	
							D	TIOB5	I/O	1	
							E	I2SMCC0_DOUT3	O	2	
Y14	VDDLVDS	GPIO	PE12	I/O	LVDS_CLK1M	O	A	LCDC_DEN	O	1,2	PIO, I, PU, ST
							B	PCK3	O	4	
							C	PWMEXTRG0	I	2	
							D	TCLK5	I	1	
							E	I2SMCC0_DIN0	I	2	
AA14	VDDLVDS	GPIO	PE13	I/O	LVDS_CLK1P	O	A	LCDC_PCK	O	1,2	PIO, I, PU, ST
							B	PCK4	O	3	
							C	PWMEXTRG1	I	2	
							E	I2SMCC0_DOUT0	O	2	
B4	VDDIN33	Analog input	ADVREFP	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
F14	VDDIN33	Power	VDDIN33	I	–	–	–	–	–	–	–
H16	GNDIN33	Ground	GNDIN33	I	–	–	–	–	–	–	–
F16	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–
E10	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–
E12	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–
N16	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–
Y18	VDDIOP0	Power	VDDIOP0	I	–	–	–	–	–	–	–
K24	VDDGMAC0	Power	VDDGMAC0	I	–	–	–	–	–	–	–
F21	VDDIOP1	Power	VDDIOP1	I	–	–	–	–	–	–	–
F24	VDDGMAC1	Power	VDDGMAC1	I	–	–	–	–	–	–	–
A1	GND	Ground	GND	I	–	–	–	–	–	–	–
A25	GND	Ground	GND	I	–	–	–	–	–	–	–
AA1	GND	Ground	GND	I	–	–	–	–	–	–	–
AA4	GND	Ground	GND	I	–	–	–	–	–	–	–
AA6	GND	Ground	GND	I	–	–	–	–	–	–	–
D4	GND	Ground	GND	I	–	–	–	–	–	–	–
D24	GND	Ground	GND	I	–	–	–	–	–	–	–
E2	GND	Ground	GND	I	–	–	–	–	–	–	–
E5	GND	Ground	GND	I	–	–	–	–	–	–	–
E8	GND	Ground	GND	I	–	–	–	–	–	–	–
E14	GND	Ground	GND	I	–	–	–	–	–	–	–
E18	GND	Ground	GND	I	–	–	–	–	–	–	–
E16	VDDANA	Power	VDDANA	I	–	–	–	–	–	–	–
F10	VDDANA	Power	VDDANA	I	–	–	–	–	–	–	–
F12	VDDANA	Power	VDDOUT25	O	–	–	–	–	–	–	–
V15	VDDANA	Power	VDDIN25	I	–	–	–	–	–	–	–
L1	GND	Ground	GND		–	–	–	–	–	–	–
G11	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
N19	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
H12	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
F1	GND	Ground	GND	I	–	–	–	–	–	–	–
K17	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
K20	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
L13	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
M12	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
N17	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
V19	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
P21	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
T14	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
T24	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
Y16	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
G19	VDDCPU	Power	VDDCPU	I	–	–	–	–	–	–	–
H20	VDDCPU	Power	VDDCPU	I	–	–	–	–	–	–	–
H24	VDDCPU	Power	VDDCPU	I	–	–	–	–	–	–	–
J19	VDDCPU	Power	VDDCPU	I	–	–	–	–	–	–	–
K18	VDDCPU	Power	VDDCPU	I	–	–	–	–	–	–	–
J17	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
F9	GND	Ground	GND	I	–	–	–	–	–	–	–
F20	GND	Ground	GND	I	–	–	–	–	–	–	–
G2	GND	Ground	GND	I	–	–	–	–	–	–	–
G3	GND	Ground	GND	I	–	–	–	–	–	–	–
G5	GND	Ground	GND	I	–	–	–	–	–	–	–
G7	GND	Ground	GND	I	–	–	–	–	–	–	–
G9	GND	Ground	GND	I	–	–	–	–	–	–	–
H1	GND	Ground	GND	I	–	–	–	–	–	–	–
H5	GND	Ground	GND	I	–	–	–	–	–	–	–
H8	GND	Ground	GND	I	–	–	–	–	–	–	–
H10	GND	Ground	GND	I	–	–	–	–	–	–	–
H18	GND	Ground	GND	I	–	–	–	–	–	–	–
H21	GND	Ground	GND	I	–	–	–	–	–	–	–
J1	GND	Ground	GND	I	–	–	–	–	–	–	–
J3	GND	Ground	GND	I	–	–	–	–	–	–	–
J5	GND	Ground	GND	I	–	–	–	–	–	–	–
J7	GND	Ground	GND	I	–	–	–	–	–	–	–
P16	GND	Ground	GND	I	–	–	–	–	–	–	–
T16	VDDLVDS	Power	VDDLVDS	I	–	–	–	–	–	–	–
H14	GNDUTMI	Ground	GNDUTMI	I	–	–	–	–	–	–	–
J15	VDDUTMI	Power	VDDUTMI	I	–	–	–	–	–	–	–
B1	VDDUTMI	–	HHSDPA	I/O	–	–	–	–	–	–	–
B2	VDDUTMI	–	HHSDMA	I/O	–	–	–	–	–	–	–
C1	VDDUTMI	–	HHSDPB	I/O	–	–	–	–	–	–	–
C2	VDDUTMI	–	HHSDMB	I/O	–	–	–	–	–	–	–
D1	VDDUTMI	–	HHSDPC	I/O	–	–	–	–	–	–	–
D2	VDDUTMI	–	HHSDMC	I/O	–	–	–	–	–	–	–
C3	VDDUTMI	Analog input	HHSRTUNE	I	–	–	–	–	–	–	–
K12	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
K14	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
L9	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
L10	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
L11	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
L15	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
M9	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
M10	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
M14	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
M16	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
N11	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
N13	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
N15	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
P10	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
P12	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
J9	GND	Ground	GND	I	–	–	–	–	–	–	–
J10	GND	Ground	GND	I	–	–	–	–	–	–	–
K2	GND	Ground	GND	I	–	–	–	–	–	–	–
K8	GND	Ground	GND	I	–	–	–	–	–	–	–
K10	GND	Ground	GND	I	–	–	–	–	–	–	–
K11	GND	Ground	GND	I	–	–	–	–	–	–	–
K13	GND	Ground	GND	I	–	–	–	–	–	–	–
K15	GND	Ground	GND	I	–	–	–	–	–	–	–
K21	GND	Ground	GND	I	–	–	–	–	–	–	–
AA8	GND	Ground	GND	I	–	–	–	–	–	–	–
AA10	GND	Ground	GND	I	–	–	–	–	–	–	–
AA25	GND	Ground	GND	I	–	–	–	–	–	–	–
B16	GND	Ground	GND	I	–	–	–	–	–	–	–
B24	GND	Ground	GND	I	–	–	–	–	–	–	–
E4	VDDIODDR	Analog input	DDR_VREF	I	–	–	–	–	–	–	–
J12	VDDIODDR	Analog input	DDR_ZQ	O	–	–	–	–	–	–	–
P20	VDDDPHY	Power	VDDDPHY	I	–	–	–	–	–	–	–
M21	GNDDPHY	Ground	GNDDPHY	I	–	–	–	–	–	–	–
Y22	VDDDPHY	–	MIPI_CLKN	O	–	–	–	–	–	–	–
AA22	VDDDPHY	–	MIPI_CLKP	O	–	–	–	–	–	–	–
Y20	VDDDPHY	–	MIPI_DN0	O	–	–	–	–	–	–	–
AA20	VDDDPHY	–	MIPI_DP0	O	–	–	–	–	–	–	–
Y21	VDDDPHY	–	MIPI_DN1	O	–	–	–	–	–	–	–
AA21	VDDDPHY	–	MIPI_DP1	O	–	–	–	–	–	–	–
Y24	VDDDPHY	–	MIPI_DN2	O	–	–	–	–	–	–	–
Y25	VDDDPHY	–	MIPI_DP2	O	–	–	–	–	–	–	–
W24	VDDDPHY	–	MIPI_DN3	O	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
W25	VDDDPHY	–	MIPI_DP3	O	–	–	–	–	–	–	–
AA23	VDDDPHY	–	MIPI_REXT	I	–	–	–	–	–	–	–
U21	VDDSDMMC0	Power	VDDSDMMC0	I	–	–	–	–	–	–	–
B18	VDDSDMMC1	Power	VDDSDMMC1	I	–	–	–	–	–	–	–
T20	VDDSDMMC0	Analog input	SDMMC0_CAL	I	–	–	–	–	–	–	–
F18	VDDSDMMC1	Analog input	SDMMC1_CAL	I	–	–	–	–	–	–	–
D22	VDDSDMMC2	Power	VDDSDMMC2	I	–	–	–	–	–	–	–
E19	VDDSDMMC2	Analog input	SDMMC2_CAL	I	–	–	–	–	–	–	–
J16	GNDBAT	Ground	GNDBAT	I	–	–	–	–	–	–	–
K16	VBAT	Power	VBAT	I	–	–	–	–	–	–	–
G17	VBAT	PIOBU	PIOBU0	I	–	–	–	–	–	–	PU[5]
B14	VBAT	PIOBU	PIOBU1	I	–	–	–	–	–	–	PU[5]
C15	VBAT	PIOBU	PIOBU2	I	–	–	–	–	–	–	PU[5]
A13	VBAT	PIOBU	PIOBU3	I	–	–	–	–	–	–	PD[5]
B10	VDDIN33	–	XIN	I	–	–	–	–	–	–	–
A10	VDDIN33	–	XOUT	O	–	–	–	–	–	–	–
A15	VBAT	–	XIN32	I	–	–	–	–	–	–	–
B15	VBAT	–	XOUT32	O	–	–	–	–	–	–	–
D15	VBAT	–	TST	I	–	–	–	–	–	–	PD
C13	VBAT	–	JTAGSEL	I	–	–	–	–	–	–	PD
A16	VBAT	–	WKUP0	I	–	–	–	–	–	–	–
B13	VBAT	–	SHDN	O	–	–	–	–	–	–	–
B9	VDDIN33	–	NRST	I	–	–	–	–	–	–	PU
B8	VDDIN33	–	NRST_OUT	O	–	–	–	–	–	–	OD[6]
C11	VDDIN33	GPIO	AUDIOCLK	O	–	–	–	–	–	–	–
A12	VBAT	Backup I/O	LPM	O	–	–	–	–	–	–	–
M24	VDDQSPI0	Power	VDDQSPI0	I	–	–	–	–	–	–	–
L22	VDDQSPI0	Analog input	QSPI0_CAL	I	–	–	–	–	–	–	–
A14	GND	Ground	GND	I	–	–	–	–	–	–	–
H15	GND	Ground	GND	I	–	–	–	–	–	–	–
A11	GND	Ground	GND	I	–	–	–	–	–	–	–
A9	GND	Ground	GND	I	–	–	–	–	–	–	–
AA3	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
AA5	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
AA7	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
AA9	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
E1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
E3	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
E7	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
E9	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F5	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F8	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
G1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
G4	DDRM_ZQ	Analog input	DDRM_ZQ	I	–	–	–	–	–	–	–
G6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
H2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
H6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
J2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
J4	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
J6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
K1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
K5	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
K6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
K7	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
K9	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
L2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
L3	GND	Ground	GND	I	–	–	–	–	–	–	–
L4	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
L5	GND	Ground	GND	I	–	–	–	–	–	–	–
L6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
L7	GND	Ground	GND	I	–	–	–	–	–	–	–
L8	GND	Ground	GND	I	–	–	–	–	–	–	–
L12	GND	Ground	GND	I	–	–	–	–	–	–	–
L14	GND	Ground	GND	I	–	–	–	–	–	–	–
L16	GND	Ground	GND	I	–	–	–	–	–	–	–
L17	GND	Ground	GND	I	–	–	–	–	–	–	–
L18	GND	Ground	GND	I	–	–	–	–	–	–	–
M1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
M2	GND	Ground	GND	I	–	–	–	–	–	–	–
M5	GND	Ground	GND	I	–	–	–	–	–	–	–
M6	GND	Ground	GND	I	–	–	–	–	–	–	–
M7	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
M8	GND	Ground	GND	I	–	–	–	–	–	–	–
M11	GND	Ground	GND	I	–	–	–	–	–	–	–
M13	GND	Ground	GND	I	–	–	–	–	–	–	–
M15	GND	Ground	GND	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
M17	GND	Ground	GND	I	–	–	–	–	–	–	–
M18	GND	Ground	GND	I	–	–	–	–	–	–	–
N1	GND	Ground	GND	I	–	–	–	–	–	–	–
N2	GND	Ground	GND	I	–	–	–	–	–	–	–
N3	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
N4	GND	Ground	GND	I	–	–	–	–	–	–	–
N5	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
N6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
N7	GND	Ground	GND	I	–	–	–	–	–	–	–
N8	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
N9	GND	Ground	GND	I	–	–	–	–	–	–	–
N10	GND	Ground	GND	I	–	–	–	–	–	–	–
N12	GND	Ground	GND	I	–	–	–	–	–	–	–
N14	GND	Ground	GND	I	–	–	–	–	–	–	–
N18	GND	Ground	GND	I	–	–	–	–	–	–	–
P1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
P2	GND	Ground	GND	I	–	–	–	–	–	–	–
P5	GND	Ground	GND	I	–	–	–	–	–	–	–
P6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
P8	GND	Ground	GND	I	–	–	–	–	–	–	–
P11	GND	Ground	GND	I	–	–	–	–	–	–	–
P13	GND	Ground	GND	I	–	–	–	–	–	–	–
P14	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
P18	GND	Ground	GND	I	–	–	–	–	–	–	–
P24	GND	Ground	GND	I	–	–	–	–	–	–	–
R1	GND	Ground	GND	I	–	–	–	–	–	–	–
R2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
R3	GND	Ground	GND	I	–	–	–	–	–	–	–
R4	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
R5	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
R6	GND	Ground	GND	I	–	–	–	–	–	–	–
R7	GND	Ground	GND	I	–	–	–	–	–	–	–
R9	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
R10	GND	Ground	GND	I	–	–	–	–	–	–	–
R11	GND	Ground	GND	I	–	–	–	–	–	–	–
R12	DDR_VREF	Analog input	DDR_VREF	I	–	–	–	–	–	–	–
R13	VDDIODDR	Power	VDDIODDR	I	–	–	–	–	–	–	–
R19	GND	Ground	GND	I	–	–	–	–	–	–	–
T1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
T2	GND	Ground	GND	I	–	–	–	–	–	–	–
T5	GND	Ground	GND	I	–	–	–	–	–	–	–
T6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
T8	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
T9	GND	Ground	GND	I	–	–	–	–	–	–	–
T10	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
T11	GND	Ground	GND	I	–	–	–	–	–	–	–
T12	GND	Ground	GND	I	–	–	–	–	–	–	–
T15	GND	Ground	GND	I	–	–	–	–	–	–	–
T21	GND	Ground	GND	I	–	–	–	–	–	–	–
U1	GND	Ground	GND	I	–	–	–	–	–	–	–
U2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
U3	GND	Ground	GND	I	–	–	–	–	–	–	–
U4	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
U5	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
U7	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
U8	GND	Ground	GND	I	–	–	–	–	–	–	–
U9	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
U10	GND	Ground	GND	I	–	–	–	–	–	–	–
U12	GND	Ground	GND	I	–	–	–	–	–	–	–
U14	GND	Ground	GND	I	–	–	–	–	–	–	–
U16	GND	Ground	GND	I	–	–	–	–	–	–	–
U18	GND	Ground	GND	I	–	–	–	–	–	–	–
V1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
V2	GND	Ground	GND	I	–	–	–	–	–	–	–
V4	GND	Ground	GND	I	–	–	–	–	–	–	–
V6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
V7	GND	Ground	GND	I	–	–	–	–	–	–	–
V9	GND	Ground	GND	I	–	–	–	–	–	–	–
V20	GND	Ground	GND	I	–	–	–	–	–	–	–
V22	GND	Ground	GND	I	–	–	–	–	–	–	–
W1	GND	Ground	GND	I	–	–	–	–	–	–	–
W2	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
W3	GND	Ground	GND	I	–	–	–	–	–	–	–
W5	GND	Ground	GND	I	–	–	–	–	–	–	–
W6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
W7	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
W9	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
W11	GND	Ground	GND	I	–	–	–	–	–	–	–

Table 9-1. Pin Description[1][2] (continued)

427-pin TFBGA	Power Rail	I/O Type[3]	Primary		Alternate		PIO Peripheral				Reset State[4]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
W15	GND	Ground	GND	I	–	–	–	–	–	–	–
W23	GND	Ground	GND	I	–	–	–	–	–	–	–
Y1	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
Y2	GND	Ground	GND	I	–	–	–	–	–	–	–
Y4	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
Y5	GND	Ground	GND	I	–	–	–	–	–	–	–
Y6	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
Y7	GND	Ground	GND	I	–	–	–	–	–	–	–
Y8	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
Y9	GND	Ground	GND	I	–	–	–	–	–	–	–
Y10	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–

Notes:

1. I/Os for each peripheral are grouped into I/O sets, listed in the column "I/O Set". For all peripherals, use I/Os that belong to the same I/O set. Timings can be unpredictable when I/Os from different I/O sets are mixed.
2. When using an I/O line with the Analog-to-Digital Converter (ADC) or with the Analog Comparator Controller (ACC), the PIO line configuration (pull-up, pull-down) programmed before assigning this line to the ADC or ACC peripheral is not modified by this peripheral.
3. Refer to I/O Characteristics in the Electrical Characteristics section of the SAMA7D6 Series data sheet for the definition of I/Os.
4. PU=Pull-Up, PD=Pull-Down, HiZ=High Impedance, ST=Schmitt Trigger
5. This is the PIOBU state after VBAT power-up. If programmed to another value, this value is maintained as long as VBAT is not removed.
6. Open-drain output requires an external resistor.

10. Electrical Characteristics

The Electrical Characteristics sections in the SAMA7D6 Series and DDR SDRAM data sheets (see Reference Documents) apply to this device. Complementary information is provided in the following sections.

The VDDQ, VDD and VDDL power inputs described in the DDR SDRAM data sheets are connected to the SAMA7D6 Series SiP balls called “DDRM_VDD”. Therefore, the requirements placed on the VDDQ, VDD and VDDL power inputs in the “Absolute Maximum Ratings” and “Recommended DC Operating Conditions” sections of these data sheets apply to the DDRM_VDD power inputs.

10.1. Recommended Thermal Operating Conditions

Table 10-1. Recommended Thermal Operating Conditions

Symbol	Parameter	Min	Max	Unit
T_{J_MPU}	Junction temperature range	-40	105	°C
T_{J_DDR}	Junction temperature range	-40	105	°C

Table 10-2. TFBGA427 Package Thermal Characteristics(1)(2)(3)

Symbol	Parameter	Typ	Unit
R_{JA}	Junction-to-ambient thermal resistance	21	°C/W

Notes:

1. $R_{JA} = (T_{J\_MPU} - T_A) / P_{MPU}$, where T_A is the ambient temperature and P_{MPU} is the processor power consumption. The DDR SDRAM junction temperature (T_{J_DDR}) is always lower than the MPU junction temperature.
2. According to the JEDEC JESD51-2 standard, with a 2s2p board and 0 m/s air flow.
3. These values are not directly applicable to the board where the device is mounted. As per JEDEC standards, these parameters do not characterize the package itself but rather the package together with the PCB (4-layer or more) and other environmental factors (still air, etc.). For example, in still-air JEDEC-defined R_{JA} measurements, almost 70% of the power generated by the chip is dissipated from the test board, not from the package surfaces.

10.2. Power Sequences

The DDR SDRAM power rail (DDRM_VDD) must be connected to VDDIODDR on the PCB. Refer to Recommended Power Supply Sequencing in the Electrical Characteristics section of the SAMA7D6 Series data sheet.

10.3. System Power Consumption in Applicative Use Cases

Table 10-4 provides the device power consumption in the following conditions:

- f_{CPU_CLK} = 800 MHz
- f_{MCK1} = 200 MHz
- f_{MCK2} = 533 MHz
- f_{MCK3} = 266 MHz
- f_{MCK4} = 400 MHz
- f_{MCK5} = 200 MHz
- f_{MCK6} = 200 MHz
- f_{MCK7} = 100 MHz
- f_{MCK8} = 100 MHz

- f_{MCK9} = 100 MHz
- I & D caches enabled
- Use cases run on Linux®
- Ambient temperature: 25°C
- Current consumption is measured as shown in Figure 10-1. Note that the external component current consumptions are counted.

The measurements are provided for typical SAMA7D65D5M, SAMA7D65D1G, SAMA7D65D2G and SAMA7D65D4G devices.

Table 10-3. Use Case Definition

Use Case	Description
1	Audio MP3 decoding and playback on I²S; MP3 file on USB mass storage
2	SAMA7D6 running as iPerf server
3	Running Bonnie++ on USB mass storage
4	SAMA7D6 downloads a file from GMAC0 and copies this file to USB mass storage
5	Test pattern display using mode test (720x1280 DSI panel @ 60 Hz)
6	Linux idle

Figure 10-1. Current Measurement for Applicative Use Cases

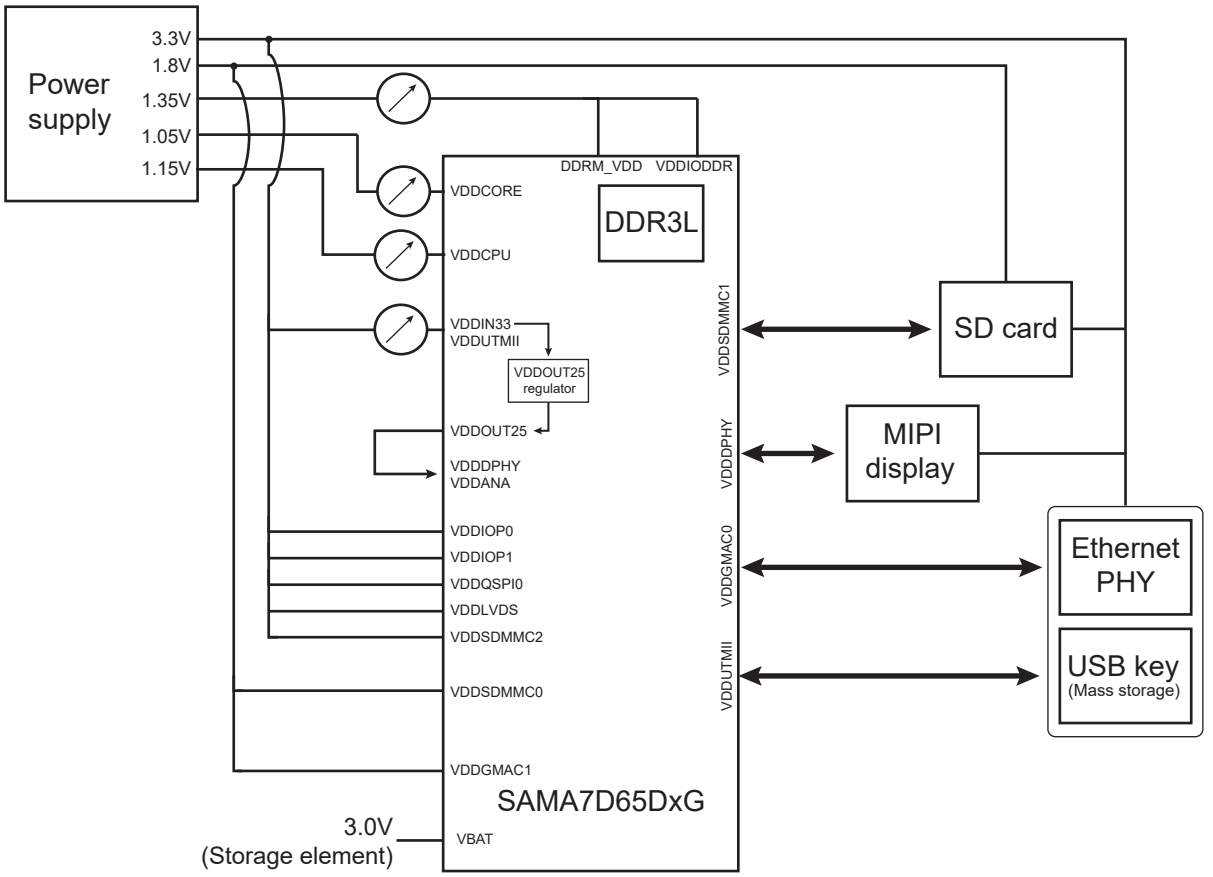


Table 10-4. Power Consumption in Applicative Use Cases

Use Case	Power Consumption (mW)				
	VDDCORE 1.05V	VDDCPU 1.15V	VDDIODDR 1.35V	VDDIN33 VDDUTMII 3.3V	Total
1	181	43	97	181	501
2	204	117	185	224	730
3	195	156	123	176	650
4	183	63	120	173	538
5	206	29	113	197	545
6	189	41	96	164	490

10.4. Power Consumption in Idle and Ultra-Low Power (ULP0, ULP1) Modes with SDRAM in Self-Refresh

For a complete description of how to enter and exit ULP0 or ULP1 mode, refer to the SAMA7D6 Series data sheet (see Reference Documents).

Table 10-5. Typical Power Consumption in Idle, ULP0 or ULP1 Mode on VDDIODDR and DDRM_VDD

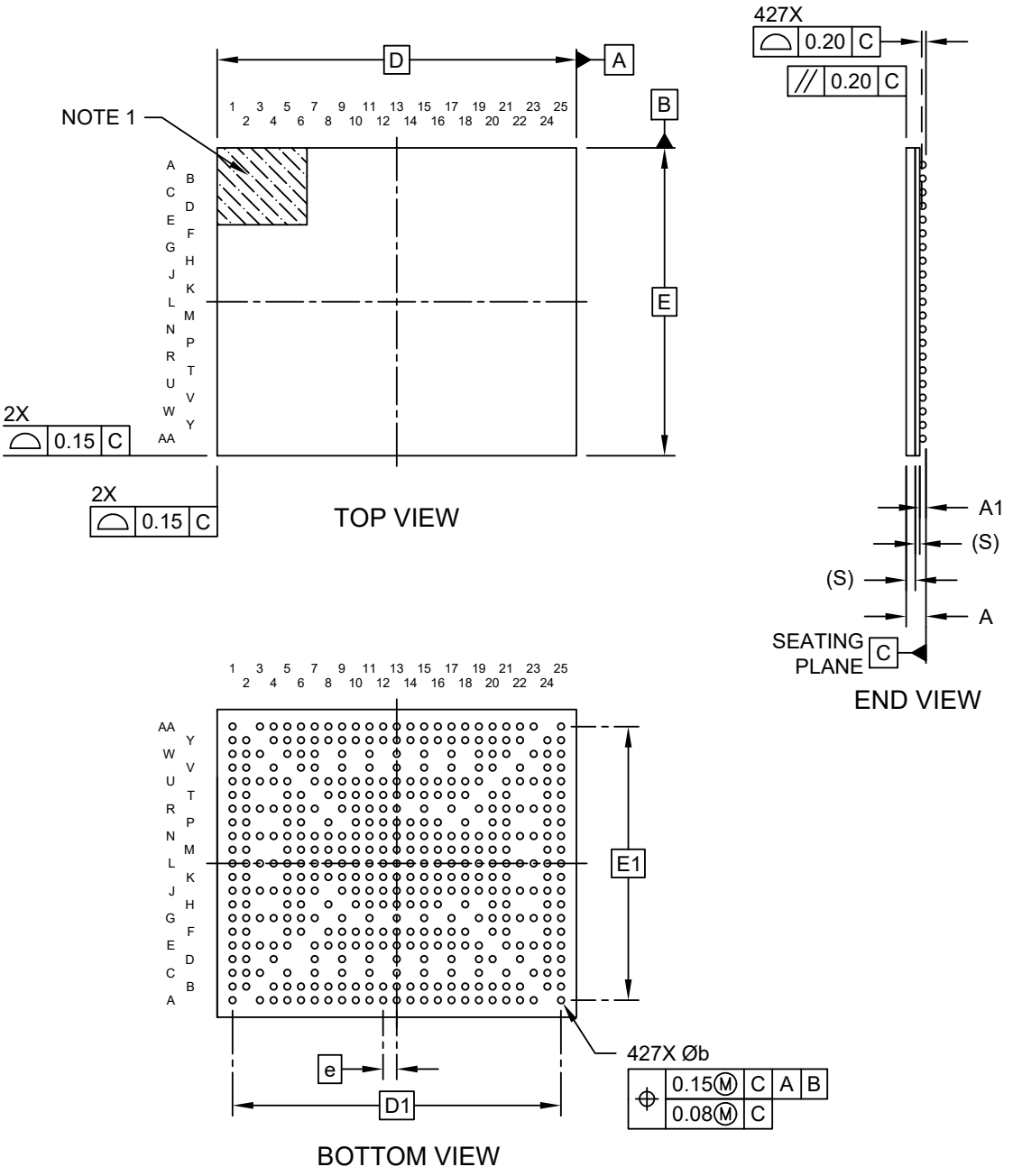
VDDIODDR DDRM_VDD (V)	T_J = -40°C	T_J = 25°C	T_J = 50°C	T_J = 70°C	T_J = 85°C	T_J = 105°C	Unit
1.35	3.7	4.3	5.1	6.3	7.7	10.9	mW

11. Mechanical Characteristics

11.1. 427-Ball TFBGA Mechanical Characteristics

427-Ball Thin Fine-Pitch Ball Grid Array (4UB) - 21x18x1.2 mm Body [TFBGA]

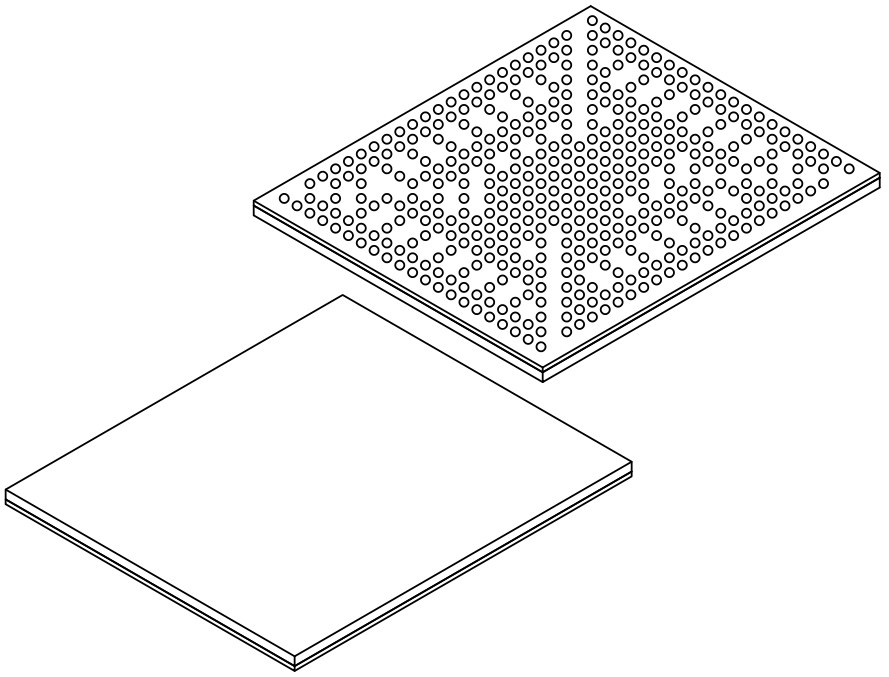
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21537 Rev A Sheet 1 of 2

427-Ball Thin Fine-Pitch Ball Grid Array (4UB) - 21x18x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		427	
Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Ball Height	A1	0.27	–	0.37
Mold Thickness	M		0.53 REF	
Substrate Thickness	S		0.26 REF	
Overall Length	D		21.00 BSC	
Ball Array Length	D2		19.20 BSC	
Overall Width	E		18.00 BSC	
Ball Array Width	E2		16.00 BSC	
Ball Width	b	0.38	–	0.45

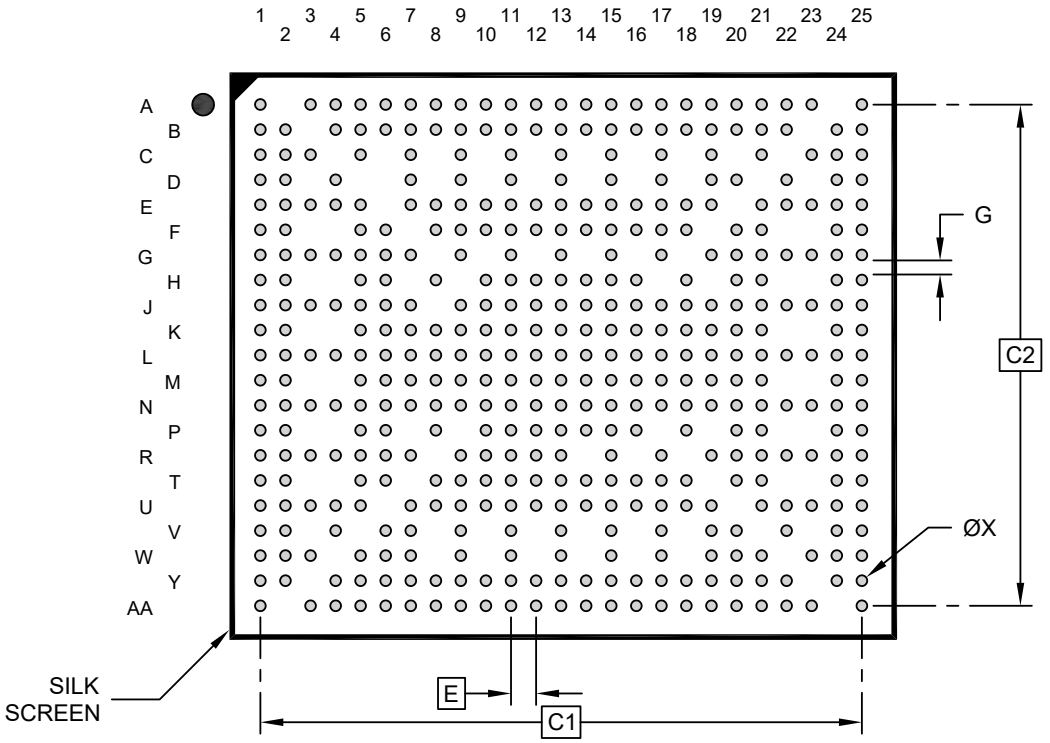
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21537 Rev A Sheet 2 of 2

427-Ball Thin Fine-Pitch Ball Grid Array (4UB) - 21x18x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		19.20 BSC	
Contact Pad Spacing	C2		16.00 BSC	
Contact Pad Width (Xnn)	X			0.35
Contact Pad to Contact Pad (Xnn)	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23537 Rev A

Table 11-1. 427-ball TFBGA Package Characteristics

Moisture sensitivity level	MSL3

Table 11-2. Device and 427-ball TFBGA Package Weight

980	mg

Table 11-3. Package Reference

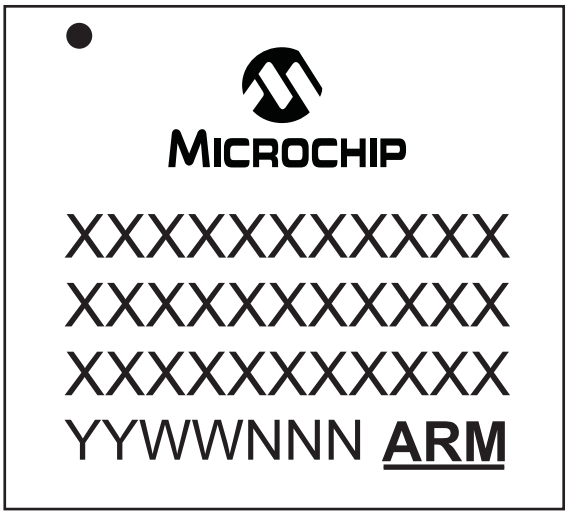
JEDEC drawing reference	N/A
J-STD-609 classification	e8

Table 11-4. 427-ball TFBGA Package Information

Ball land	0.450 mm
Nominal ball diameter	0.400 mm
Solder mask opening	0.350 mm
Solder mask definition	Solder Mask Defined (SMD)
Solder	SAC105

12. Marking

Top marking follows the scheme below:



with possible values:

Line	Description	Values
1	Company logo	Microchip logo
2	Company name	Microchip
3	Device name	SAMA7D65Dxx
4	Temperature code / Packaging code, JEDEC symbol	V/4UB e8
5	Not used	–
6	Lot traceability, Arm logo	YYWWNNN ARM

13. Revision History

13.1. Rev. D - 08/2025

Throughout: added content related to the 4-Gbit device (SAMA7D65D4G) Updated Reference Documents

13.2. Rev. C - 07/2025

Throughout: added content related to the 512-Mbit device (SAMA7D65D5M)

13.3. Rev. B - 12/2024

Complete data sheet

13.4. Rev. A - 06/2024

Preliminary issue

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Product Page Links

SAMA7D65D1G, SAMA7D65D2G, SAMA7D65D4G, SAMA7D65D5M