SAMA7D6 Series Silicon Errata and Data Sheet Clarifications

SAMA7D6 Series

Product Page Links

Scope

The SAMA7D6 Series device that you have received conforms functionally to the current SAMA7D6 Series device data sheet (DS60001851) or SAMA7D6 Series SiP data sheet (DS60001853), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the device revision and device identification listed in the following table. The silicon issues are summarized in Silicon Issue Summary.

Data sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications.

The silicon device revisions and device IDs are shown in the following table.

Table 1. SAMA7D6 Series Device Identification

Ordering Code	Device Revision	Device Identification
		CHIPID_CIDR[31:0]
SAMA7D65(T)-V/4HB	A0	0x80262110
SAMA7D65D1G(T)-V/4UB	A0-D1G	
SAMA7D65D2G(T)-V/4UB	A0-D2G	
SAMA7D65(T)-V/4HB	A1	0x80262111
SAMA7D65(T)-E/4HB(VAO)		
SAMA7D65D5M(T)-V/4UB	A1-D5M	
SAMA7D65D1G(T)-V/4UB	A1-D1G	
SAMA7D65D2G(T)-V/4UB	A1-D2G	

Note: Refer to the “Chip Identifier (CHIPID)” and “Product Identification System” sections in the current device data sheet for detailed information on chip identification for your specific device.

1. Silicon Issue Summary

In this table and in subsequent sections, the following applies:

- "X" means the device revision is affected by the erratum.
- "–" means the device revision is not affected by the erratum.

Table 1-1. Silicon Issue Summary

Module	Erratum	Affected Device Revisions	
		A0 **A0-D1G** **A0-D2G**	**A1** **A1-D5M** **A1-D1G** **A1-D2G**
ROM Code	Watchdog not disabled	X	X
	Boot failure on e.MMC memories	X	X
SHDWC	Wake-up events are not deactivated	X	X
RTC	RTC_TSTR0 timestamping error	X	X
PMC	Delay to first establish PCK	X	X
	Programmable Clock Output (PCKx) Ready status issue	X	X
PIO	Open drain management limitation	X	X
ADC	Temperature sensor still enabled when stopped without conversion	X	X
	Temperature sensor spurious activation with CH30	X	X
I2SMCC	Time Division Multiplexed Left Justified (TDMLJ) is not functional in Client mode	X	X
SSC	Inverted left/right channels	X	X
	TD output delay	X	X
SECUMOD	Tamper timestamping polarity error	X	X
GMAC	GMAC0 not functional with multiple queues in 10/100 Half Duplex mode	X	X
SDMMC	SDMMC failure when changing speed mode or performing ALL soft reset on the fly	X	X
	GCLK cannot be stopped	X	X
	EXTUN (Execute Tuning) status issue	X	X
	HS400 and HS400-ES modes are not functional	X	X
MCAN	Debug message handling state machine not reset to Idle when CCCR.INIT is set	X	X
TCPC	Signal level detection not functional	X	–

2. ROM Code

2.1. Watchdog not disabled

When entering SAM-BA monitor, even after a USB enumeration by a host or reception of a character on the UART ROM code console, the Dual Watchdog Timer is not disabled.

As a consequence, the chip resets after the watchdog timeout elapses. A typical value is 16 seconds.

Work Around

Before the timeout elapses, write the WDDIS bit in PS_WDT_MR to disable the Dual Watchdog Timer.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

2.2. Boot failure on e.MMC memories

The device fails to load a bootstrap program (boot.bin) from an e.MMC **USER** partition.

Work Around

Always use the e.MMC **BOOT** partition to store the boot.bin file and enable the e.MMC **BOOT** partition feature.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

3. Shutdown Controller (SHDWC)

3.1. Wake-up events are not deactivated

When SHDW_MR.WKUPDBC is set to 0, wake-up events wake up the system even if they are deactivated (SHDW_WUIR.WKUPENx set to 0).

Work Around

To deactivate wake-up events, set SHDW_MR.WKUPDBC to a non-null value.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

4. Real-time Clock (RTC)

4.1. RTC_TSTR0 timestamping error

RTC_TSTR0.TEVCNT fails to report the correct number of tamper event occurrences.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

5. Power Management Controller (PMC)

5.1. Delay to first establish PCK

When enabling a PCK after a reset, the delay before establishing the PCK with the correct frequency is 255 cycles of the PCK source clock. Once this delay has elapsed, and as long as the core reset is not asserted, there is no more additional delay when disabling/enabling the PCK.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

5.2. Programmable Clock Output (PCKx) Ready status issue

The Programmable Clock Output (PCKx) Ready status bit (PMC_SR.PCKRDYx) remains unexpectedly high when the PCKx source clock (PMC_PCKx.CSS) is changed on the fly while PCKx is already running.

Work Around

To change a PCKx source clock:

1. Disable PCKx (PMC_SCDR.PCKx).
2. Change the source clock (PMC_PCKx.CSS).
3. Re-enable PCKx (PMC_SCER.PCKx).
4. Wait for PCKRDYx to rise (PMC_SR.PCKRDYx).

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

6. Parallel Input/Output Controller (PIO)

6.1. Open drain management limitation

PIOC does not allow open drain configuration (PIO_CFGRx.OPD=1) when a peripheral is selected (PIO_CFGRx.FUNC different from 0).

TWI/TWIHS peripherals are not affected.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

7. Analog-to-Digital Converter (ADC) Controller

7.1. Temperature sensor still enabled when stopped without conversion

The temperature sensor remains active even when ADC_TEMPMR.TEMPON is set to 0.

Work Around

To stop the temperature sensor and save its power consumption, perform a conversion prior to writing ADC_TEMPMR.TEMPON=0.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

7.2. Temperature sensor spurious activation with CH30

Enabling ADC channel 30 enables the temperature sensor.

Work Around

To stop the temperature sensor and save its power consumption, perform a conversion prior to writing ADC_TEMPMR.TEMPON=0.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

8. Inter-IC Sound Multi-Channel Controller (I2SMCC)

8.1. Time Division Multiplexed Left Justified (TDMLJ) is not functional in Client mode

When the clock is enabled during a high level of the frame synchro signal (I2SMCC_WS) by writing I2SMCC_CR.CKEN = 1, the data alignment is incorrect.

Work Around

None.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

9. Synchronous Serial Controller (SSC)

9.1. Inverted left/right channels

When the SSC is in Client mode, the TF signal is derived from the codec and not controlled by the SSC. The SSC transmits the data when detecting the falling edge on the TF signal after the SSC transmission is enabled. In some overflow cases, a left/right channel inversion may occur and may require SSC reinitializing.

Work Around

Use the SSC in Host mode so that TF is controlled by the SSC. If the SSC must be used in TF Client mode, start the SSC by writing TXEN and RXEN synchronously with the TXSYN flag rising.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

9.2. TD output delay

The TD output is delayed by two or three extra system clock cycles when SSC is configured with the following conditions:

- RCMR.START = Start on falling edge/Start on rising edge/Start on any edge
- RFMR.FSOS = None (input)
- TCMR.START = Receive Start

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

10. Security Module (SECUMOD)

10.1. Tamper timestamping polarity error

The tamper detection signal polarity is inverted, with the following consequences:

- Key erasing in TZAEB, AES and TDES if the respective Clear On Tamper features are enabled, with TZAESB_MR.TAMPCLR = 1, AES_MR.TAMPCLR = 1 and TDES_MR.TAMPCLR = 1.
- Scrambling key erasing in QSPI0 or QSPI1 if Clear On Tamper is enabled with QSPI0_MR.TAMPCLR = 1 or QSPI1_MR.TAMPCLR = 1.
- SHA locking if Tamper Lock is enabled with SHA_MR.TMPLCK = 1. SHA is locked until SHA_CR.UNLOCK is written to 1.

Work Around

Do not enable the following bits:

- TZAESB_MR.TAMPCLR
- AES_MR.TAMPCLR
- TDES_MR.TAMPCLR
- QSPI0_MR.TAMPCLR
- QSPI1_MR.TAMPCLR
- SHA_MR.TMPLCK

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

11. Gigabit Ethernet MAC (GMAC)

11.1. GMAC0 not functional with multiple queues in 10/100 Half Duplex mode

When operating in 10/100 Half Duplex mode, GMAC0 does not work with multiple queues.

Work Around

Configure the controller for transmission over a single queue.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

12. Secure Digital MultiMedia Card Controller (SDMMC)

12.1. SDMMC failure when changing speed mode or performing ALL soft reset on the fly

Changing speed mode or performing an ALL soft reset while SDCK is active may lead to block the SDMMC.

Work Around

Stop SDCLK before changing speed mode or performing an ALL soft reset, then re-enable SDCLK by writing SDMMC_CCR.SDCLKEN to 0 before writing SDMMC_MC1R/SDMMC_HC1R/SDMMC_HC2R.

Example:

```
//FIX : stop SDCLK
pSDMMC->SDMMC_CCR = pSDMMC->SDMMC_CCR & ~SDMMC_CCR_SDCLKEN;
switch (speed_mode) {
case DS : pSDMMC->SDMMC_HC1R = pSDMMC->SDMMC_HC1R & ~SDMMC_HC1R_HSEN;
break;
case HS : pSDMMC->SDMMC_HC1R = pSDMMC->SDMMC_HC1R | SDMMC_HC1R_HSEN;
break;
case SDR12 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR12;
break;
case SDR25 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR25;
break;
case SDR50 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR50;
break;
case SDR104 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR104;
break;
case DDR50 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_DDR50;
break;
}
//FIX : re-start SDCLK
pSDMMC->SDMMC_CCR = pSDMMC->SDMMC_CCR | SDMMC_CCR_SDCLKEN;
```

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

12.2. GCLK cannot be stopped

If a speed mode other than Default Speed or SDR12 is used, GCLK cannot be stopped, leading to unpredictable behavior.

Work Around

Perform an ALL soft reset before any operation to ensure the internal clock DLL can be stopped properly.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										

X	X										

12.3. EXTUN (Execute Tuning) status issue

After starting a tuning procedure by setting the SDMMC_HC2R.EXTUN bit, this bit is not automatically cleared when the tuning procedure is completed.

Work Around

Do not wait for SDMMC_HC2R.EXTUN to be cleared. Launching 17 iterations of the tuning command always finalizes the tuning procedure.

Example:

```
//FIX: Tuning procedure

enum tuning_status {TUNING_SUCCEED, TUNING_FAIL};
enum tuning_status st;

// Start the tuning procedure
#ifdef EMMC_MODE
// e.MMC Mode
pSDMMC->SDMMC_HC2R |= SDMMC_HC2R_EMMC_EXTUN_1;
#else
// SD/SDIO mode
pSDMMC->SDMMC_HC2R |= SDMMC_HC2R_SD_SDIO_EXTUN_1;
#endif

// Tuning procedure is always completed after 17 executions of the tuning command
for (ix = 0; ix < 17; ix++) {

#ifdef EMMC_MODE
   // e.MMC Mode : command SEND_TUNING_BLOCK (CMD21)
   send_cmd21();
#else
   // SD/SDIO mode : command SEND_TUNING_PATTERN (CMD19)
   send_cmd19();
#endif
   // Wait for BRDRDY status to be set
   while (!(pSDMMC->SDMMC_NISTR & SDMMC_NISTR_BRDRDY_Msk));
   // Clear BRDRDY status bit
   pSDMMC->SDMMC_NISTR = SDMMC_NISTR_BWRRDY_0;
}

// Check if tuning failed
if (!(pSDMMC->SDMMC_HC2R & SDMMC_HC2R_SCLKSEL_1))
   // Tuning failed
   st = TUNING_FAIL;
else
   // Tuning successful
   st = TUNING_SUCCEED;

// Clear residual interrupts, if any
if (pSDMMC->SDMMC_NISTR & SDMMC_NISTR_ERRINT_1)
    pSDMMC->SDMMC_EISTR = pSDMMC->SDMMC_EISTR;

// Clear residual status, if any
pSDMMC->SDMMC_NISTR = pSDMMC->SDMMC_NISTR;
```

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

12.4. HS400 and HS400-ES modes are not functional

Using modes HS400 and HS400-ES may lead to data read error failures.

Work Around

None.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

13. Controller Area Network (MCAN)

13.1. Debug message handling state machine not reset to Idle when CCCR.INIT is set

When the host sets the MCAN_CCCR.INIT bit through the MCAN_CCCRn register, or when the CAN enters Bus Off state, the debug message handling state machine stays in its current state instead of resetting to Idle state. Setting MCAN_CCCR.CCE does not change MCAN_RXF1S.DMS.

Work Around

If the debug message handling state machine stopped while MCAN_RXF1S.DMS="01" or MCAN_RXF1S.DMS="10", it can be reset to Idle state by hardware reset or by reception of debug messages after MCAN_CCCR.INIT is reset to zero.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	X										

14. USB Type-C™ Port Controller (TCPC)

14.1. Signal level detection not functional

Signal level detection on CC1/CC2 signals and D+/D- signals is not functional. USB Type-C features (cable detection, cable inversion, etc.) and battery charging features (Battery Charging Source Type Detection and Accessory Charger Adapter Detection) are not supported.

USB ports A and B, which include TCPC, are both affected.

Work Around

None. Do not use Type-C Port Controller (CC1/CC2 signal) or battery charging features on USB ports A and B.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G										
X	–										

15. Data Sheet Clarifications

There are no known data sheet clarifications as of this publication date.

16. Revision History

16.1. DS80001131F - 07/2025

Extended scope to the SAMA7D65D5M(T)-V/4UB devices

16.2. DS80001131E - 07/2025

Added:

- EXTUN (Execute Tuning) status issue
- HS400 and HS400-ES modes are not functional

16.3. DS80001131D - 05/2025

Extended scope to the SAMA7D65(T)-E/4HB(VAO) devices

16.4. DS80001131C - 02/2025

- Added:
  - Boot failure on e.MMC memories
  - Programmable Clock Output (PCKx) Ready status issue
- Throughout: changed terminology from “silicon revision” to “device revision”
- Removed “PCK and GCLK Ready status issue” erratum

16.5. DS80001131B - 11/2024

First issue.

16.6. DS80001131A - 06/2024

Preliminary issue.

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