

FINAL PROGRAM

FOURTH IEEE SYMPOSIUM ON COMPUTER ARITHMETIC

October 25-27, 1978
Santa Monica, California, U. S. A.
sponsored by
IEEE Computer Society in cooperation
with the UCLA Computer Science Department

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California, Los Angeles, U. S. A.

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Wednesday, October 25, 1978

8:00 AM Registration

9:00 Opening Remarks

- Miloš D. Ercegovic, Symposium Chairman
- Algirdas Avižienis, Program Chairman

Welcome

- Walter J. Karplus, UCLA Computer Science Department Chairman

9:15 SESSION 1

Chairman: R. T. Gregory

- 1.1 *Basic Digit Sets for Radix Representation of the Integers*
D. W. Matula
- 1.2 *Exact Arithmetic Using a Variable-Length p-adic Representation*
R. N. Horspool and E. C. R. Hehner
- 1.3 *An Interleaved Rational/Radix Arithmetic System for High-Precision Computations*
K. Hwang and T. P. Chang

10:30 Coffee

10:50 SESSION 2

Chairman: W. J. Cody

- 2.1 *A Unified Approach to a Class of Number Systems*
I. Koren and Y. Maliniak
- 2.2 *A Feasibility Analysis of Binary Fixed-Slash and Floating-Slash Number Systems*
D. W. Matula and P. Kornerup *Sacrifices Integer*
- 2.3 *A Feasibility Analysis of Fixed-Slash Rational Arithmetic*
P. Kornerup and D. W. Matula
- 2.4 *A Modified Bi-Imaginary Number System*
A. G. Slekyš and A. Avižienis

12:30 Luncheon

2:00 SESSION 3

Chairman: D. W. Matula

- 3.1 *Required Scientific Floating Point Arithmetic*
L. A. Liddiard
- 3.2 *Desirable Floating-Point Arithmetic and Elementary Functions for Numerical Computation*
T. E. Hull
- 3.3 *A Realistic Model for Error Estimates in the Evaluation of Elementary Functions*
K. S. Frankowski
- 3.4 *Some Experiments Using Interval Arithmetic*
E. K. Reuter, J. P. Jeter, J. W. Anderson and B. D. Shriver

3:40 Coffee

4:00 Panel Session I

Chairman: W. J. Cody

Is Floating-Point Arithmetic Standardization Possible?

6:30 No-Host Cocktails

7:30 Symposium Dinner

- Speaker: W. Kahan, UC Berkeley

Thursday, October 26, 1978

9:00 SESSION 4

Chairman: P. Kornerup

- 4.1 *Multivariable Polynomial Processing-Applications to Interpolation*
E. V. Krishnamurthy and H. Venkateswaran
- 4.2 *On Arithmetic Inter-relationships and Hardware Interchangeability of Negabinary and Binary Systems*
D. P. Agrawal
- 4.3 *An Appropriate and Empirical Study of the Distribution of Adder Inputs and Maximum Carry Length Propagation*
O. N. Garcia, H. Glass, and S. C. Haines
- 4.4 *On Modular (2^n+1) Arithmetic Logic*
D. P. Agrawal and T. R. N. Rao

10:40 Coffee

11:00 SESSION 5

Chairman: T. C. Chen

- 5.1 *Logical Design of a Redundant Binary Adder*
C. Y. Chow and J. E. Robertson
- 5.2 *Parallel Adders Using Standard PLAs*
A. Weinberger
- 5.3 *A Comparison of Two Approaches to Multi-Operand Binary Addition*
D. E. Atkins and S. C. Ong

12:15 Luncheon

2:00 SESSION 6

Chairman: J. E. Robertson

- 6.1 *Multiple Addition of Binary Serial Numbers*
L. Dadda
- 6.2 *High-Speed Multiplication and Multiple Summand Addition*
R. S. Lim
- 6.3 *The Theory and Implementation of High-Radix Division*
D. G. Tan
- 6.4 *Higher Radix On-Line Division*
K. S. Trivedi and J. G. Rusnak

3:40 Coffee

4:00

SESSION 7

Chairman: L. Dadda

- 7.1 *Convergence Guarantee and Improvements for a Hardware Exponential and Logarithm Evaluation Scheme*
C. Wrathall and T. C. Chen
- 7.2 *An On-Line Square Rooting Algorithm*
M. D. Ercegovic
- 7.3 *An Arithmetic Module for Efficient Evaluation of Functions*
M. D. Ercegovic and M. M. Takata
- 7.4 *Two Methods for Fast Integer Binary - BCD Conversion*
F. A. Schreiber and R. Stefanelli

Friday, October 27, 1978

9:00

SESSION 8

Chairman: E. V. Krishnamurthy

- 8.1 *Arithmetic Circuit Fault Detection by Modular Encoding*
A. Svoboda
- 8.2 *Application of the Residue Number System to Computer Processing of Digital Signals*
G. A. Jullien and W. C. Miller
- 8.3 *Mathematical Approach to Iterative Computation Networks*
D. Cohen
- 8.4 *Merged Arithmetic for Signal Processing*
E. E. Swartzlander, Jr.

10:40 Coffee

11:00

SESSION 9 to 4?

Chairman: B. D. Shriver

- 9.1 *Design of Arithmetic Elements for Burroughs Scientific Processor*
D. D. Gajski and L. P. Rubinfield
- 9.2 *Survey of Arithmetic Integrated Circuits*
S. Waser
- 9.3 *Computational Design Alternatives with Microprocessor-Based Systems*
S. L. Lillevik and P. D. Fisher

2:00

Panel Session II

Chairman: M. Ercegovic

Research Directions and Projects in Computer Arithmetic

3:30 End of Symposium

SCA-4 Special Events

Wednesday, October 25

4:00 PM-PANEL DISCUSSION

"Is Floating-Point Arithmetic Standardization Possible?"

Chairman: *W. J. Cody, Argonne National Laboratory*

Panelists: *T. E. Hull, University of Toronto*

W. Kahan, University of California, Berkeley

C. Kaman, Digital Equipment Corporation

J. F. Palmer, Intel Corporation

A. Riccomi, Texas Instruments, Inc.

D. Jelp, Signetics

6:30 PM-NO-HOST COCKTAILS

7:30 PM-SYMPOSIUM BANQUET

1) Dinner

2) Recognition of Professor Antonin Svoboda, Guest of Honor

Professor Ray Redheffer, Department of Mathematics, University of California, Los Angeles

3) "Can You Count on Your Calculator?"

Illustrated Lecture, Professor William Kahan, Department of Electrical Engineering and Computer Science, University of California, Berkeley

Banquet Tickets at \$15.00 each are available
at the Registration Desk.

Friday, October 27

2:00 PM-PANEL SESSION

"Research Directions and Projects in Computer Arithmetic"

Chairman: *Milos D. Ercegovic, University of California, Los Angeles*

"Concurrent Error Detection in Parallel Computer Systems"

R. S. Lim, NASA-Ames Research Center

"On-Line Algorithms and Their Implementation"

M. J. Irwin, Pennsylvania State University

"DELTA - A General Purpose Language for Algorithm Development"
with demonstrations

C. Satten, University of California, Los Angeles