- Weitek Business: Solutions To Floating Point Intensive Problems

- 500 Man-years Experience In Floating Point Chip Design & Marketing

Ken Stanley
14 July 88

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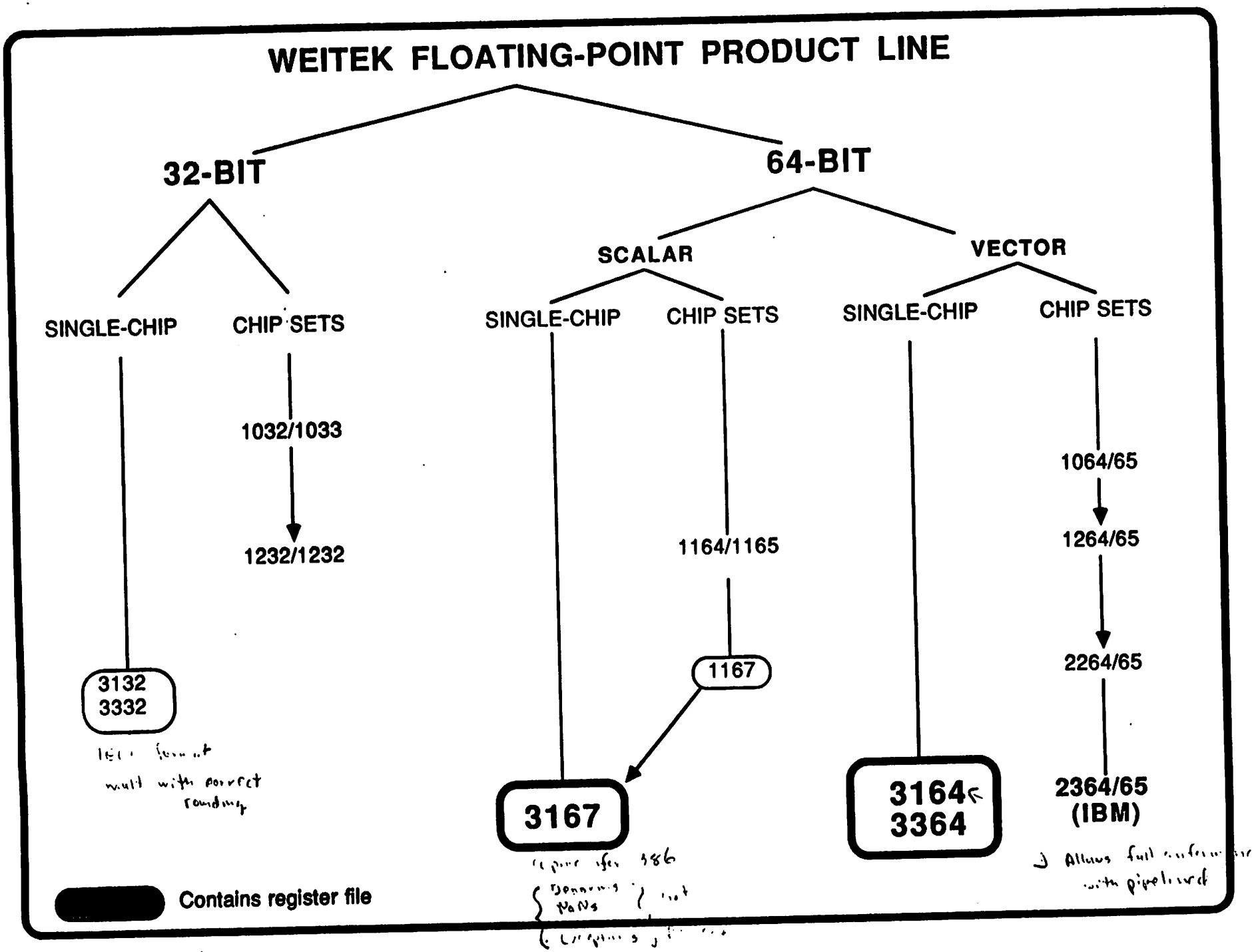
- Weitek Makes Chips (Apples)

- IEEE 754 Is A System Level Spec (Oranges)


WEITEK FLOATING-POINT PRODUCT LINE
32-BIT
64-BIT
SCALAR
VECTOR
SINGLE-CHIP
CHIP SETS
SINGLE-CHIP
CHIP SETS
SINGLE-CHIP
CHIP SETS
1032/1033
1232/1232
1164/1165
1167
1064/65
1264/65
2264/65
2364/65
(IBM)
3132
3332
3167
3164
3364
Contains register file

All Generalizations Are False

# ALL WEITEK CHIPS

- Conform To IEEE Format (Except 2364/2365)
- Allow Control Of Overflow Trap
- Do Not Support 80-bit Arithmetic
- Do Not Support De-Norms In Hardware
- Have Multiplier Arrays

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# WEITEK SINGLE CHIP SOLUTIONS

- Attack System Cost
- Reduce Time To Market
- ansi C
- fortran 77
- CMOS
- 32 Registers
- 3132, 1167/3167, 3164/3364

# 3132

- 32-bits Only
- Graphics/DSP
- No Denorm, NaN or Infinity Support
- MAC Operations Does Not Obey IEEE Rounding
- Ignores Underflow, Invalid, Inexact.
  Divide By Zero Gives Overflow
- Divide, and SQRT In Software (not IEEE)
- No Remainder Operation
- ~~All Four Rounding Modes~~

# 1167/3167

- 32 + 64-bit IEEE Formats
- 386 Coprocessor
- User Controllable Traps On All Five Exceptions
- Cannot Restart After An Exception
- No Denorm Support (Hardware Or Software)
- All Four Rounding Modes
- ADD, SUB, MUL, DIV On Chip
- SQRT On 3167
- Remainder In Software
- Transcendental Library

All chips have 32 registers of (16 double) size

- Can't restart operands may have been modified trap doesn't say where trap occurred

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# WEITEK 3164/3364

- First Single Chip To Make Possible Complete Compliance To The IEEE 754 Spec In A Pipelined Environment.

- Trap Handler Supplied To OEM's.

# WTL 3164 SINGLE-PORT

# AND WTL 3364 THREE-PORT

# 64-BIT FLOATING-POINT

# DATA PATH UNITS

# OUTLINE

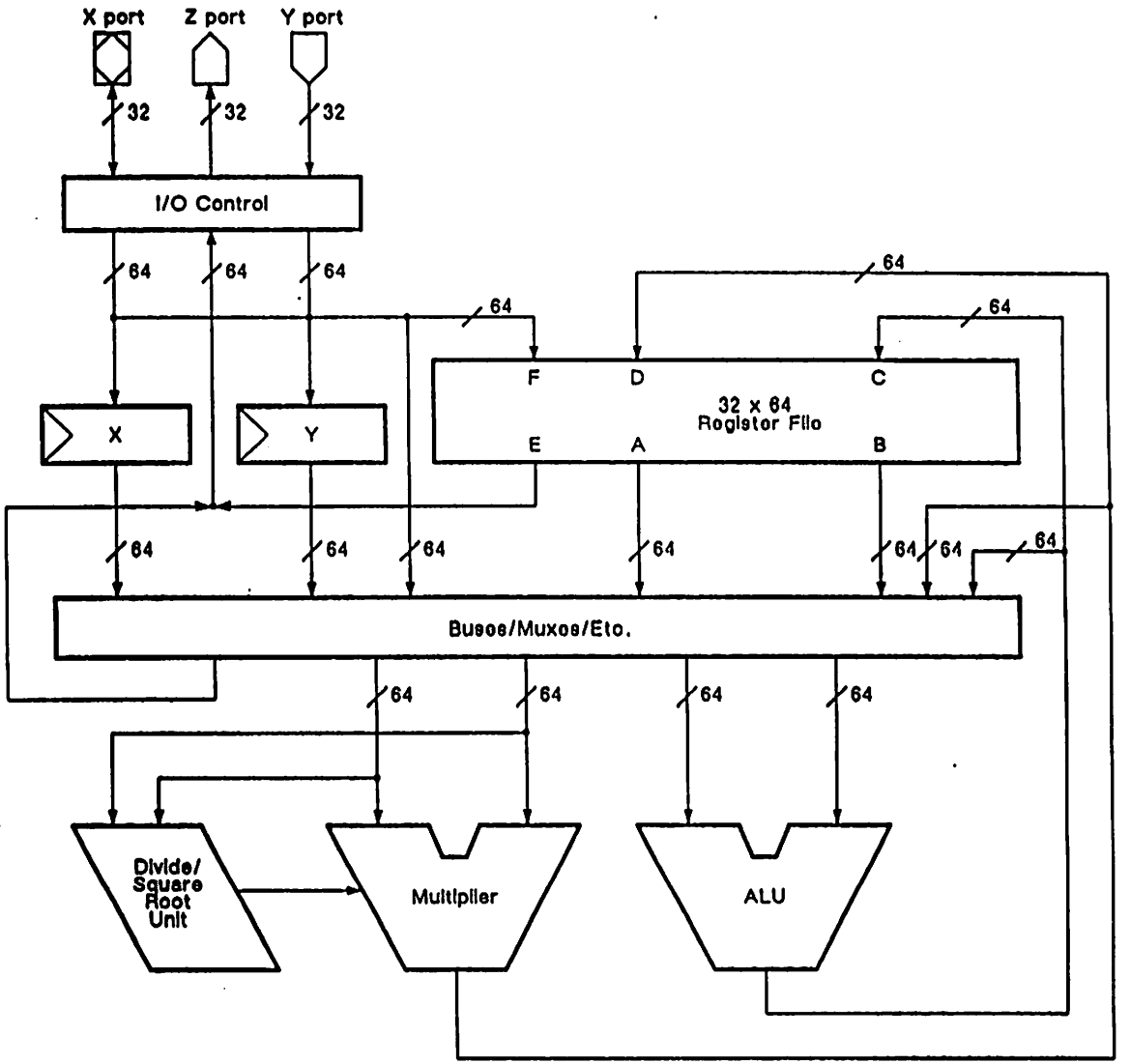
ARCHITECTURE AND FEATURES

IEEE COMPLIANCE

PERFORMANCE

STATUS AND SCHEDULE

FUTURES




## 3X64 PRODUCT UPDATE

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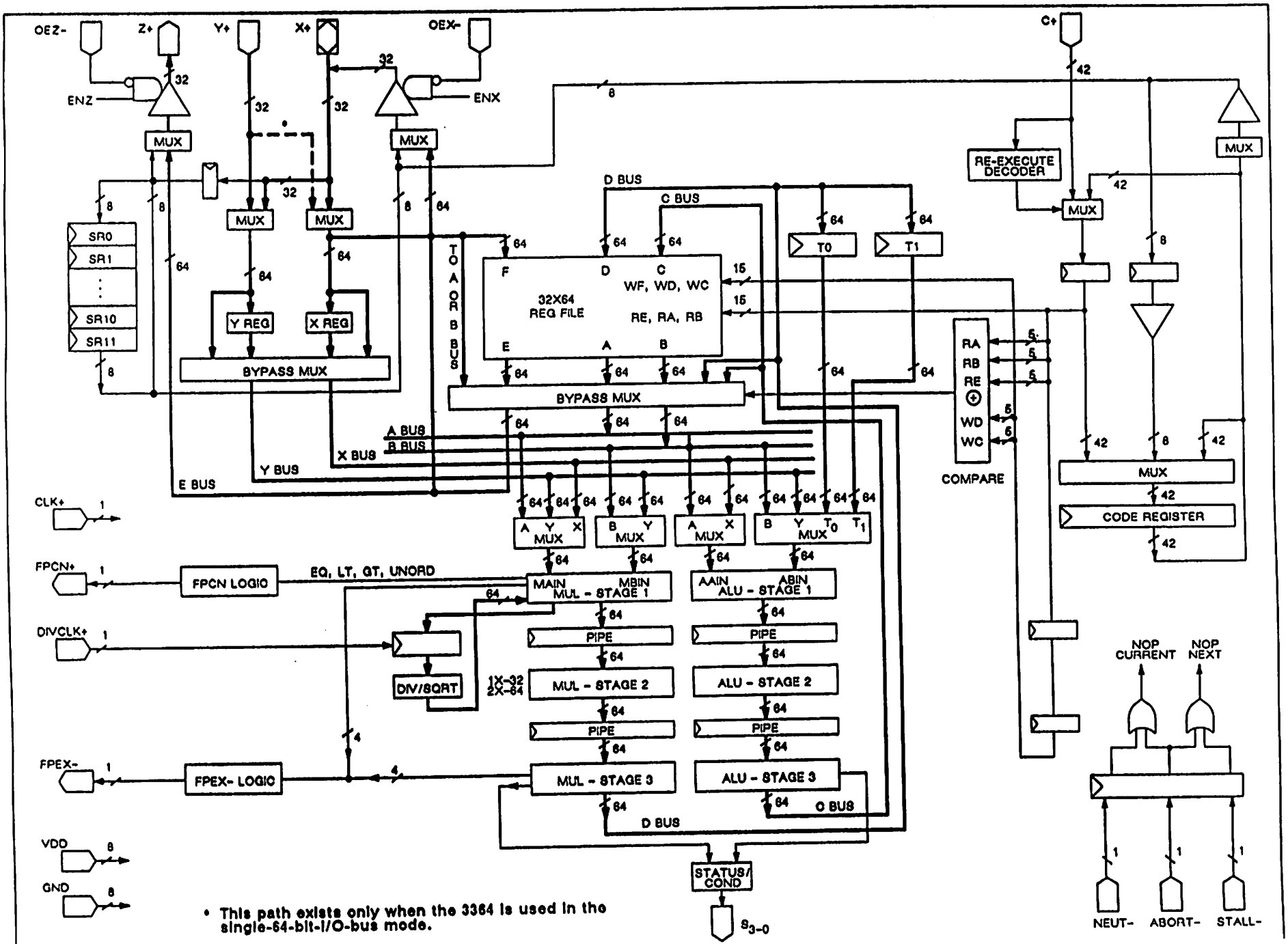
# WTL 3164 / 3364 BLOCK DIAGRAM



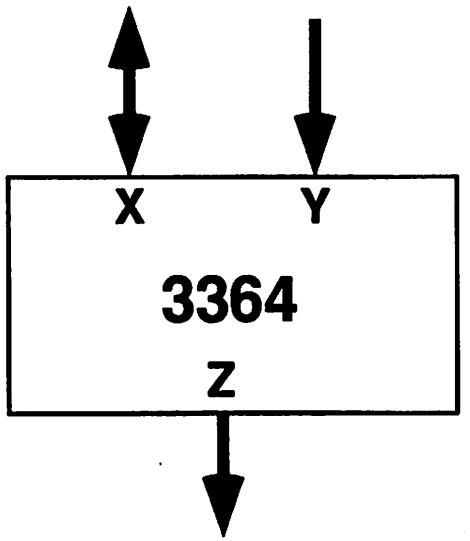

• This path exists only when the 3364 is used in the single-64-bit-I/O-bus mode.

# ARCHITECTURE

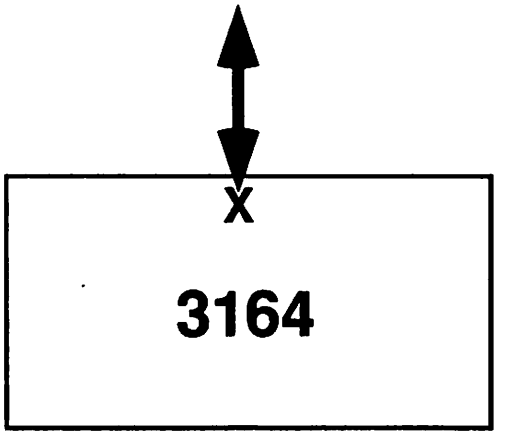
- 64-BIT IEEE FLOATING-POINT DATA PATH
- THREE INDEPENDENT ARITHMETIC UNITS CAN OPERATE IN PARALLEL
  - 64-BIT ALU
  - 64-BIT MULTIPLIER
  - 64-BIT DIVIDE/SQRT UNIT
- REGISTER FILE: SIX-PORT, 32-DEEP BY 64-BIT-WIDE
  - THREE READ PORTS
  - THREE WRITE PORTS
  - CAN BE BYPASSED ON LOADS, STORES, AND REGISTER-TO-REGISTER OPERATIONS
- INDEPENDENT LOAD/STORE
- SIX MAJOR INTERNAL 64-BIT BUSES
- EXTENSIVE STATUS AND CONTROL LOGIC

# ARCHITECTURE CONT'D

- FLEXIBLE I/O STRUCTURE
  - X PORT: I/O
  - Y PORT: INPUT ONLY
  - Z PORT: OUTPUT ONLY




- THREE 32-BIT PORTS
- SINGLE 64-BIT I/O PORT




- SINGLE 32-BIT I/O PORT

# ARCHITECTURE CONT'D

- TWO-CYCLE REGISTER-TO-REGISTER LATENCY
- SINGLE-CYCLE THROUGHPUT FOR
  - Xi * Yi -->Zi and / or Ra + Rb --> Rc
  - Ra * Xi + Yi --> Zi/Rc
  - $\sum$ Xi * Yi (requires 3364)
  - $\sum$ (Xi + Yi) (requires 3364)
- DIVIDE/SQRT LATENCY

| | DIVIDE | SQRT |
|---|---|---|
| 64-BIT | 17 | 30 |
| 32-BIT | 10 | 16 |

- DIV/SQRT CAN OVERLAP WITH MULTIPLIER AND/OR ALU OPERATION

## FULL FUNCTION

- 64- AND 32-BIT FLOATING-POINT AND 32-BIT INTEGER INSTRUCTIONS
  - MULTIPLY, ADD, MULTIPLY-ADD, DIV, SQRT, ETC.
- 64-BIT LOGICAL
- ABSOLUTE VALUE
- COMPARE
- MIN/MAX
- FORMAT CONVERSION

## FULLY INTERRUPTIBLE

- NEUT, STALL, ABORT

# IEEE COMPLIANCE

- FULL IEEE SUPPORT IN PIPELINED ENVIRONMENT
  - INCLUDING DIVIDE AND SQUARE ROOT
- ALL FOUR ROUNDING MODES
- DENORMALIZED NUMBER SUPPORT
  - FAST MODE IF DNRM SUPPORT NOT REQUIRED
- FULL STATUS AND CONDITION SUPPORT
  - FPEX PIN SIGNALS OCCURENCE OF ENABLED EXCEPTION
  - EXCEPTIONS
    - SOURCE: NAN, DNRM, DVZ, INV
    - RESULT: OVF, IOVF, UNF, INX
  - FLOATING-POINT CONDITION PIN REPORTS RESULTS OF COMPARE OPERATIONS: EQ, LT, GT, UNORDERED

# SIMPLE PROGRAMMING MODEL

- REGISTER-BASED PROGRAMMING MODEL
- MATCHED LATENCY FOR ALL OPERATIONS
  - EXCEPT DIVIDE AND SQRT
- BOTH SOURCES AND DESTINATIONS SPECIFIED ONLY ONCE -- WHEN INSTRUCTION IS ISSUED
  - DESTINATION ADDRESSES ARE DELAYED AUTOMATICALLY
- ALL INFORMATION NECESSARY FOR EXCEPTION HANDLING INCLUDED ON-CHIP
  - DEDICATED STATUS REGISTERS STORE THE STATUS AND REG FILE DESTINATION ADDRESSES

# HIGH-LEVEL LANGUAGE SUPPORT

- AVAILABLE FOR BOTH 3164 AND 3364 WHEN USED IN XL SYSTEM
  - HLL COMPILERS (C, FORTRAN)
  - DEVELOPMENT SYSTEM
  - OTHER SUPPORT: DEBUGGERS, SIMULATORS
- PERFORMANCE OF XL-3164 IN XL8164 SYSTEM

| | -100 | -080 |
|---|---|---|
| • LINPACK (MFLOPS) (HAND-CODED BLAS) | | |
| SINGLE OR DOUBLE PRECISION | 4.7 | 5.8 |
| • WHETSTONES (MWHETS) | | |
| SINGLE OR DOUBLE PRECISION | 8.7 | 10.9 |
| • DHRYSTONES | 11,834 | 14,793 |

# WEITEK 3164/3364

pipe is 7 deep
can do mult & ALU
in parallel

- 32 + 64-Bit IEEE Formats
- Denorms Handled In Software
- User Controlled Traps On All Five IEEE Exceptions
- Status Regs Allow Recovery From Exceptions
- ADD, SUB, MUL, DIV, SQRT On Chip
- DREM In Software

# 3164/3364 EXCEPTION HANDLING

- Source Exceptions:
  (Invalid, Divide-By-Zero)
  - Stop Current Operation
  - Denorm
- Destination Exceptions
  (Underflow, Overflow, Inexact)
  - Operation Completes Before Trapping
  - Correctly Rounded Result Supplied To User Trap Handler

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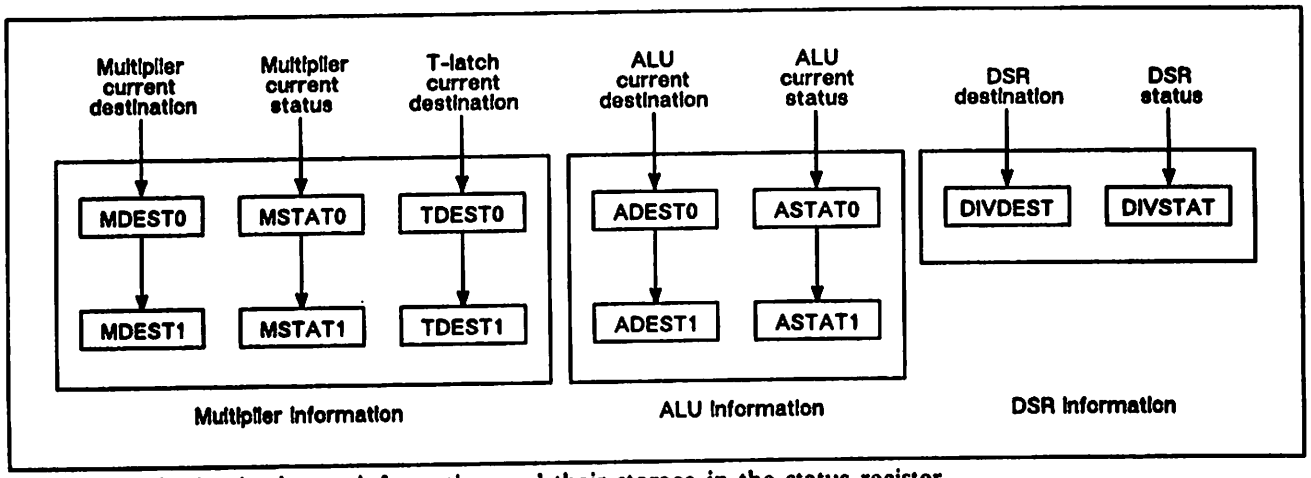
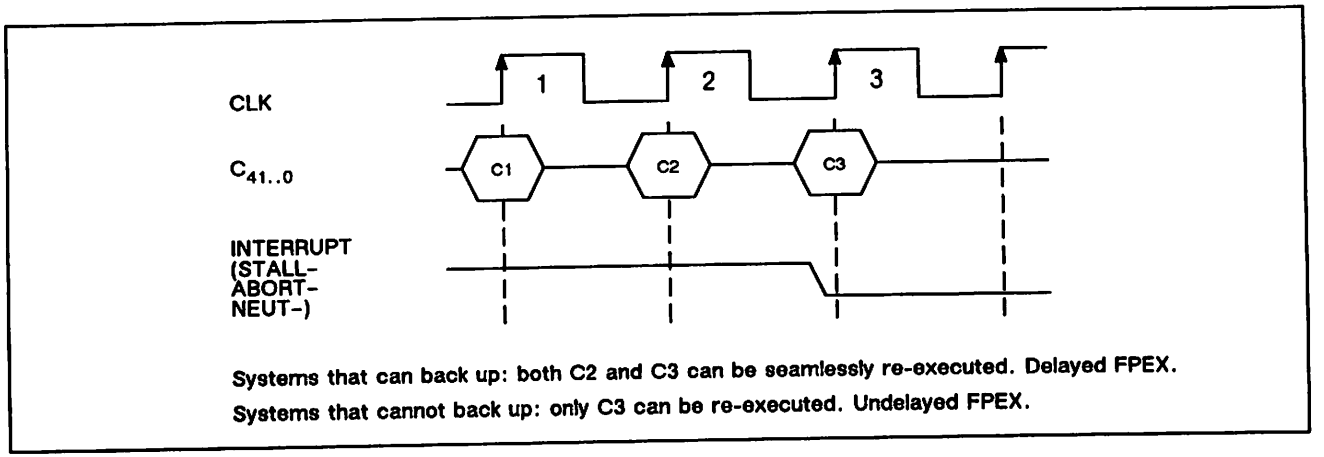


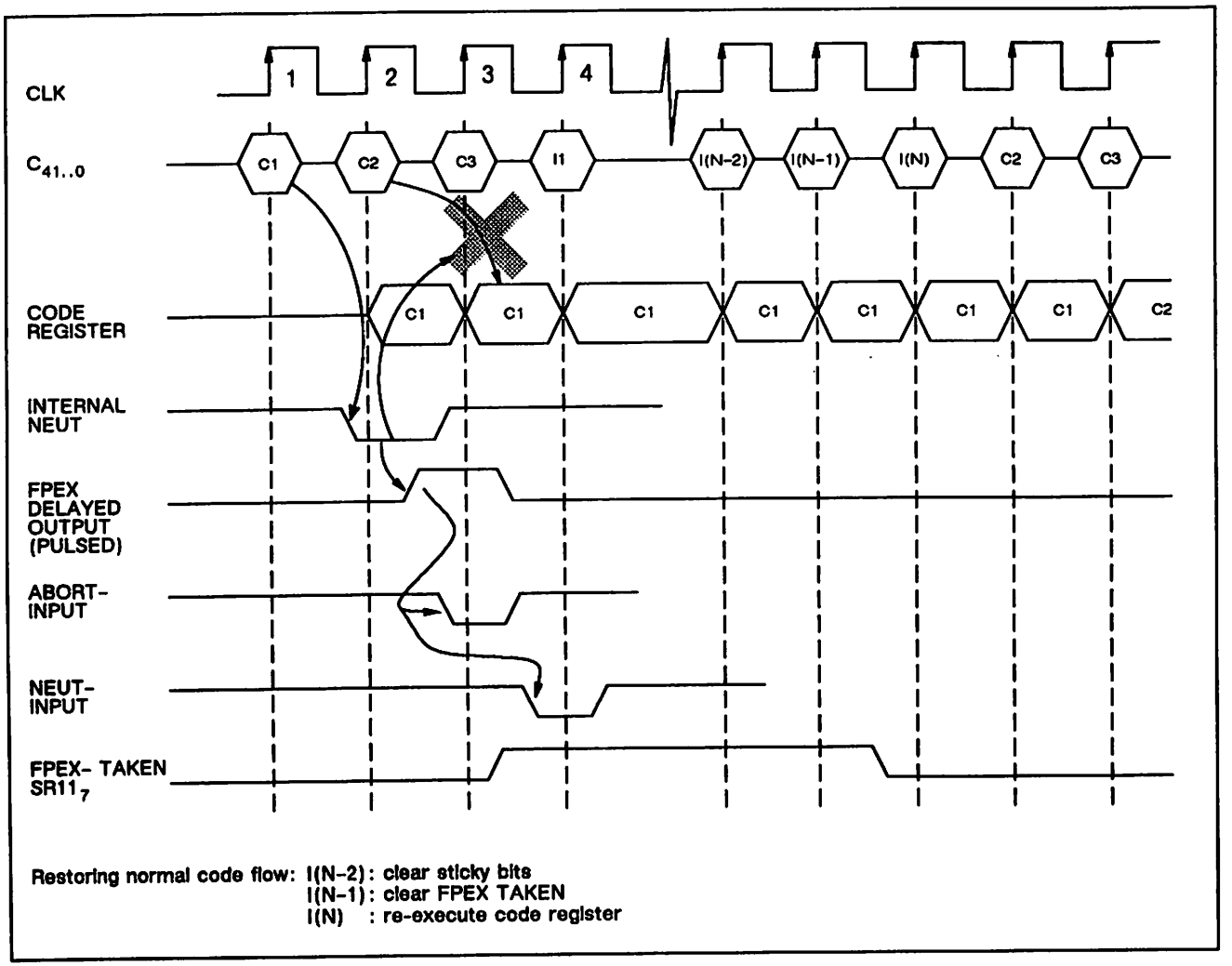

Operations' destination/status information and their storage in the status register

| SR# | BIT# | | | | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| SR0 | Multiplier Latency | FPEX-Sticky | 0 | 0 | Internal NEUT- on | Rounding Mode | | Fast Mode | Modes |
| SR1 | 0 / XL Soft-ware Underflow | Bypass on | FPEX-Delay | I/O Mode | | | | | Modes |
| SR2 | NaN EN | INV EN | DVZ EN | DNRM EN | OVF EN | UNF EN | INX EN | IOVF EN | Trap Enables |
| SR3 | NaN | INV | DVZ | DNRM | OVF | UNF | INX | IOVF | Sticky Bits |
| SR4 | 0 | TDEST0 | | MDEST0 | | | | | Destination |
| SR5 | 0 | 0 | 0 | ADEST0 | | | | | Destination |
| SR6 | ASTAT0 | | | | MSTAT0 | | | | Status |
| SR7 | 0 | 0 | 0 | DIVDEST | | | | | Destination |
| SR8 | 0 | TDEST1 | | MDEST1 | | | | | Destination |
| SR9 | 0 | 0 | 0 | ADEST1 | | | | | Destination |
| SR10 | ASTAT1 | | | | MSTAT1 | | | | Status |
| SR11 | FPEX-Taken | DSR in progress | FPCN | Carry | DIVSTAT | | | | Status |

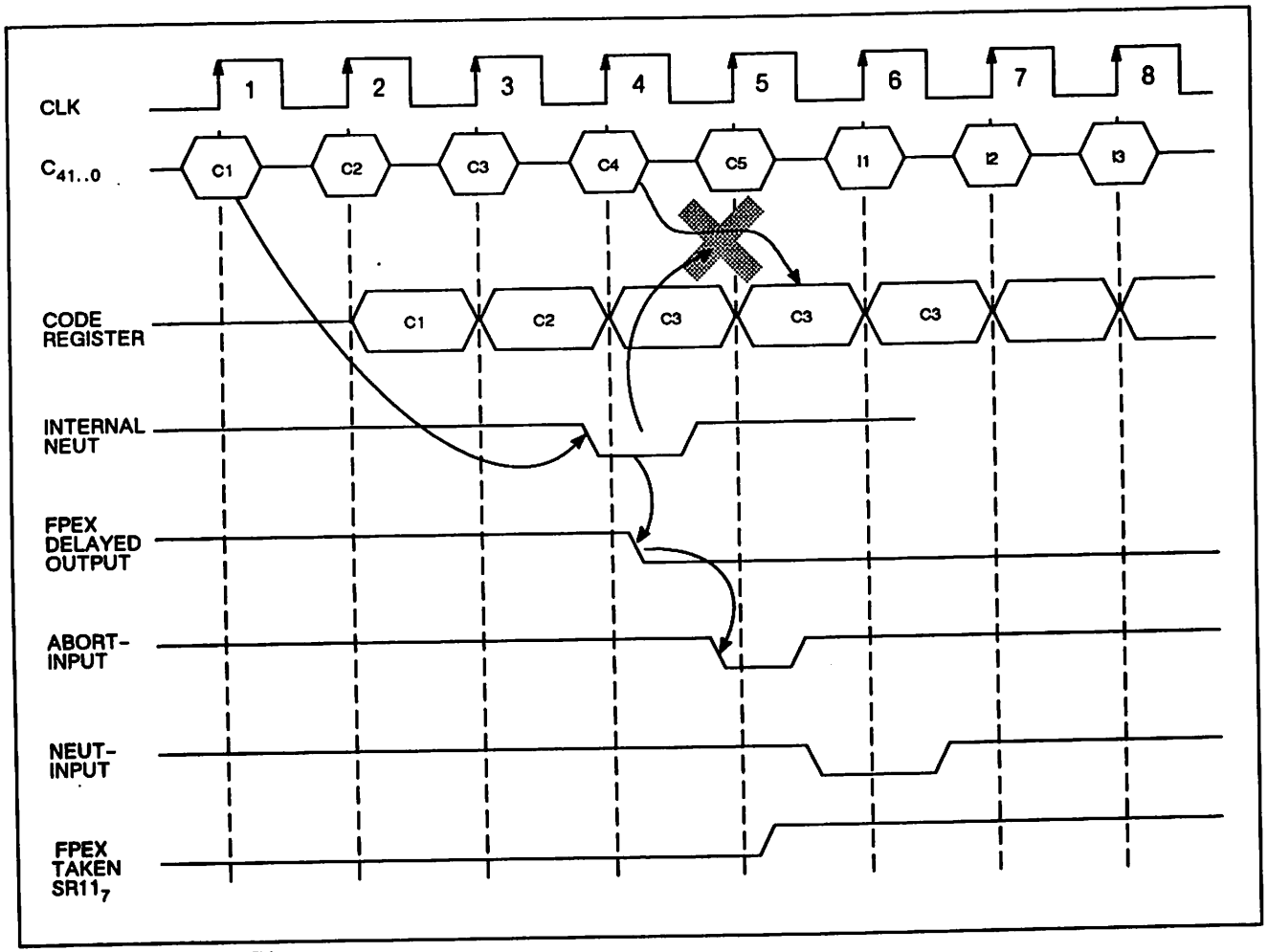
Status register structure



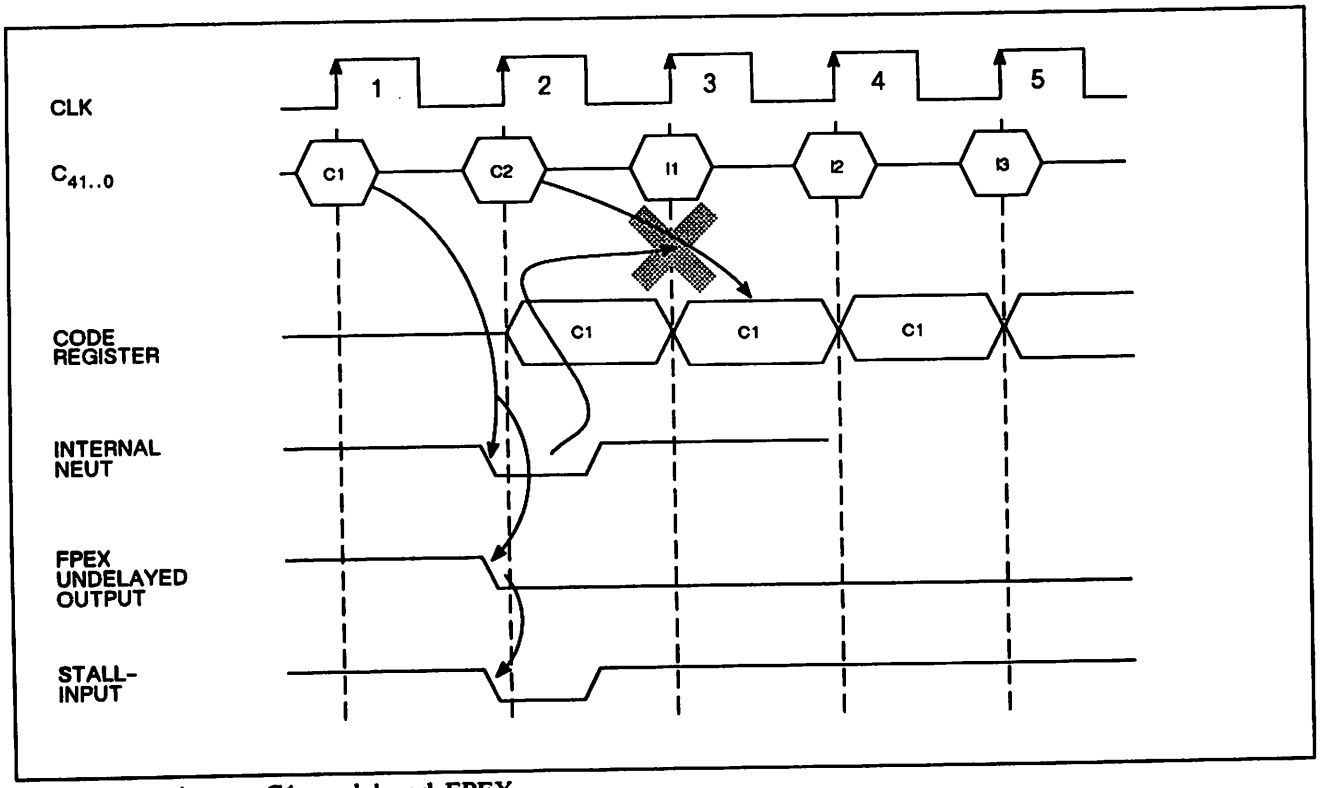

System types



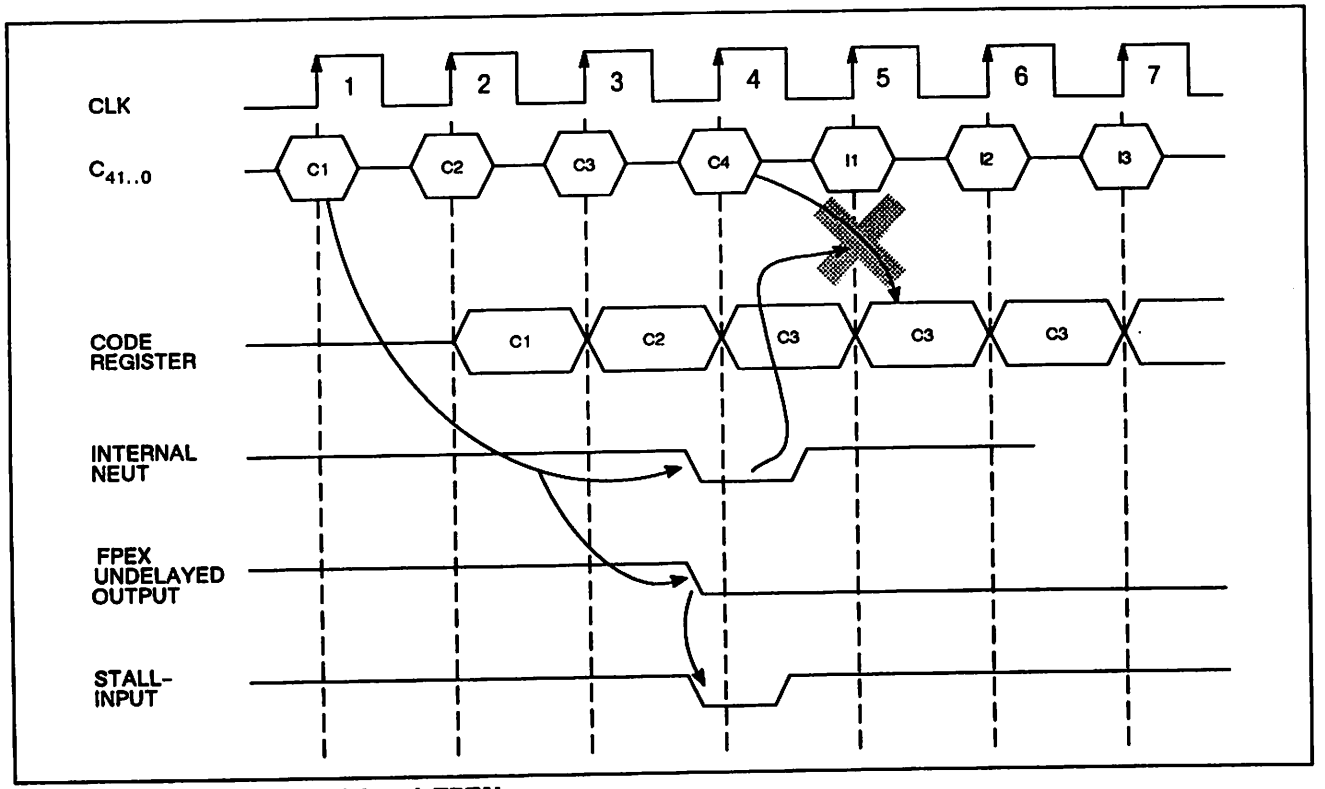

Source exception on C1




Result exception on C1




Source exception on C1, undelayed FPEX




Result exception on C1, undelayed FPEX