Inter-Kernel Communication, Jeronimo Costa Penha, José Vianna, Nusrat Jahan Lisa, UNICAMP and UFV (GitHub link)

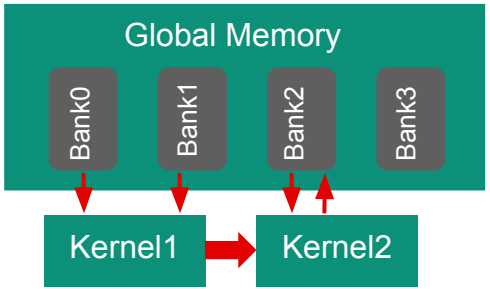
Summary

- Plan - Configure HLS Inter-Kernel streaming dataflow whereby each kernel accesses different DDR banks.
- Final project - Prepared a Vitis GUI-based Application Project having two HLS kernels and each kernel accessing different DDR banks. Emulated it both for SW and HW, build hardware (xclbin), and finally created AFI to execute the application on F1.

What we learned, or what was interesting / difficult

- Understanding how to use the tools.
- Understanding how to visualize the behavior of kernels.
- Understanding how to configure inter-kernel dataflow and different memory banks.
- Difficulty creating AFI and running on AWS.

Block diagram



Results

Name	Kernel	LUT (% Used)	Register (% Used)	BRAM (% Used)	URAM (% Used)	DSP (% Used)	Calls	CU Utilization (%)	Total Time (ms)	Avg Time (ms)
krnl_stream_vadd_1	krnl_stream_vadd	1,157 (0.1 %)	1,400 (N/A)	0 (0.0 %)	0 (N/A)	0 (0.0 %)	1	99.996 %	6543.680	6543.680
krnl_stream_vmult_1	krnl_stream_vmult	2,217 (0.19 %)	2,690 (N/A)	1 (0.05 %)	0 (N/A)	3 (0.04 %)	1	99.995 %	6543.590	6543.590

Compute Units | Kernels | Memories

Name	Type	Used	Size (kB)	Base Address	SLR
DDR[0]	DDR	✓	0x1000000	0x8_0000_0000	SLR1
DDR[1]	DDR	✓	0x1000000	0x0	SLR2
DDR[2]	DDR	✓	0x1000000	0x4_0000_0000	SLR1
DDR[3]	DDR		0x1000000	0xc_0000_0000	SLR0
PLRAM[0]	PLRAM		0x80	0x10_0000_0000	
PLRAM[1]	PLRAM		0x80	0x10_0020_0000	
PLRAM[2]	PLRAM		0x80	0x10_0040_0000	

Compute Units | Kernels | Memories