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== Synthesis Summary Report of 'simulatedAnnealingTop'
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+ General Information:
  * Date:      Wed Mar 13 18:12:06 2024
  * Version:   2022.2 (Build 3670227 on Oct 13 2022)
  * Project:   prj_ob
  * Solution:  simulatedAnnealingTop (Vitis Kernel Flow Target)
  * Product family: virtexuplus
  * Target device: xcu55c-fsvh2892-2L-e
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+ Performance & Resource Estimates:

PS: '+' for module; 'o' for loop; '\*' for dataflow

| Modules<br>& Loops                       | Issue<br>Type | Slack | Latency<br>(cycles) | Latency<br>(ns) | Iteration<br>Latency | Interval  | Trip<br>Count | Pipelined | BRAM    | DSP | FF          | LUT        | URAM |
|--|---------------|-------|---------------------|-----------------|----------------------|-----------|---------------|-----------|---------|-----|-------------|------------|------|
| + simulatedAnnealingTop                  | Timing        | -0.03 | 280003736           | 8.750e+08       | -                    | 280003737 | -             | no        | 3 (~0%) | -   | 32309 (1%)  | 22795 (1%) | -    |
| + simulatedAnnealingTop_Pipeline_1       | -             | 0.01  | 674                 | 2.106e+03       | -                    | 674       | -             | no        | -       | -   | 5277 (~0%)  | 731 (~0%)  | -    |
| o Loop 1                                 | -             | 2.29  | 672                 | 2.100e+03       | 74                   | 1         | 600           | yes       | -       | -   | -           | -          | -    |
| + simulatedAnnealingTop_Pipeline_2       | -             | 0.01  | 674                 | 2.106e+03       | -                    | 674       | -             | no        | -       | -   | 5277 (~0%)  | 731 (~0%)  | -    |
| o Loop 1                                 | -             | 2.29  | 672                 | 2.100e+03       | 74                   | 1         | 600           | yes       | -       | -   | -           | -          | -    |
| + simulatedAnnealingTop_Pipeline_3       | -             | 0.01  | 403                 | 1.259e+03       | -                    | 403       | -             | no        | -       | -   | 284 (~0%)   | 112 (~0%)  | -    |
| o Loop 1                                 | -             | 2.29  | 401                 | 1.253e+03       | 3                    | 1         | 400           | yes       | -       | -   | -           | -          | -    |
| + exec_pipeline                          | -             | 0.08  | 280000088           | 8.750e+08       | -                    | 280000088 | -             | no        | -       | -   | 18257 (~0%) | 15149 (1%) | -    |
| + exec_pipeline_Pipeline_VITIS_LOOP_6_1  | -             | 0.42  | 51                  | 159.375         | -                    | 51        | -             | no        | -       | -   | 539 (~0%)   | 602 (~0%)  | -    |
| o VITIS_LOOP_6_1                         | II            | 2.29  | 49                  | 153.125         | 14                   | 12        | 4             | yes       | -       | -   | -           | -          | -    |
| + exec_pipeline_Pipeline_VITIS_LOOP_28_1 | -             | 0.08  | 280000030           | 8.750e+08       | -                    | 280000030 | -             | no        | -       | -   | 17642 (~0%) | 13829 (1%) | -    |
| o VITIS_LOOP_28_1                        | II            | 2.29  | 280000028           | 8.750e+08       | 44                   | 28        | 10000000      | yes       | -       | -   | -           | -          | -    |
| + compute_3                              | II            | 0.41  | 27                  | 84.375          | -                    | 2         | -             | yes       | -       | -   | 5361 (~0%)  | 2613 (~0%) | -    |
| + compute_2                              | II            | 0.41  | 7                   | 21.875          | -                    | 5         | -             | yes       | -       | -   | 577 (~0%)   | 501 (~0%)  | -    |
| + compute_1                              | II            | 0.08  | 12                  | 37.500          | -                    | 1         | -             | yes       | -       | -   | 5626 (~0%)  | 4540 (~0%) | -    |
| + compute                                | II            | 0.08  | 13                  | 40.625          | -                    | 1         | -             | yes       | -       | -   | 4732 (~0%)  | 4304 (~0%) | -    |
| + simulatedAnnealingTop_Pipeline_4       | -             | 0.01  | 671                 | 2.097e+03       | -                    | 671       | -             | no        | -       | -   | 477 (~0%)   | 749 (~0%)  | -    |
| o Loop 1                                 | -             | 2.29  | 669                 | 2.091e+03       | 71                   | 1         | 600           | yes       | -       | -   | -           | -          | -    |
| + simulatedAnnealingTop_Pipeline_5       | -             | 0.01  | 671                 | 2.097e+03       | -                    | 671       | -             | no        | -       | -   | 477 (~0%)   | 749 (~0%)  | -    |
| o Loop 1                                 | -             | 2.29  | 669                 | 2.091e+03       | 71                   | 1         | 600           | yes       | -       | -   | -           | -          | -    |
| + simulatedAnnealingTop_Pipeline_6       | -             | 0.01  | 403                 | 1.259e+03       | -                    | 403       | -             | no        | -       | -   | 145 (~0%)   | 211 (~0%)  | -    |
| o Loop 1                                 | -             | 2.29  | 401                 | 1.253e+03       | 3                    | 1         | 400           | yes       | -       | -   | -           | -          | -    |