ThoughtChip

Patent pending and patented technologies bring consciousness to machines and devices controlled by volition alone (i.e., no need to bore holes in people's heads and embroid their brains with an over-glorified Singer sewing machine.)

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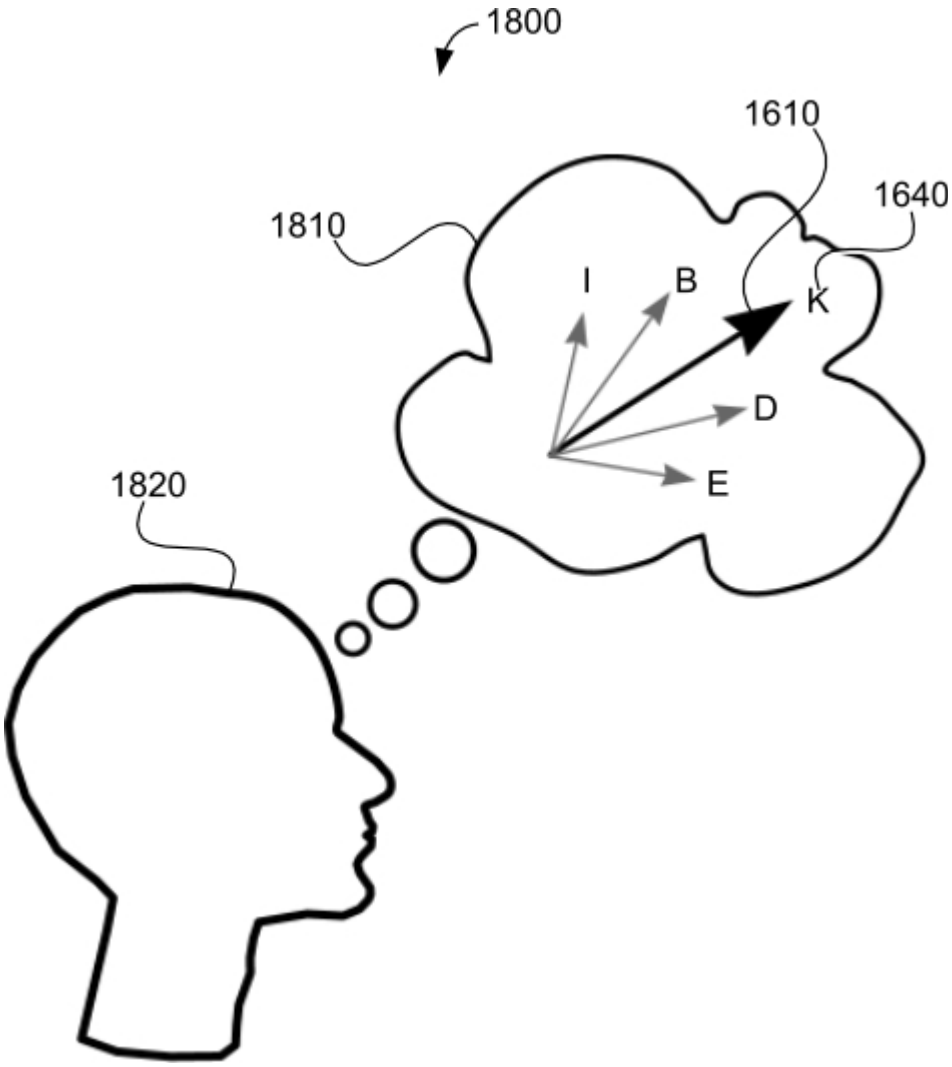
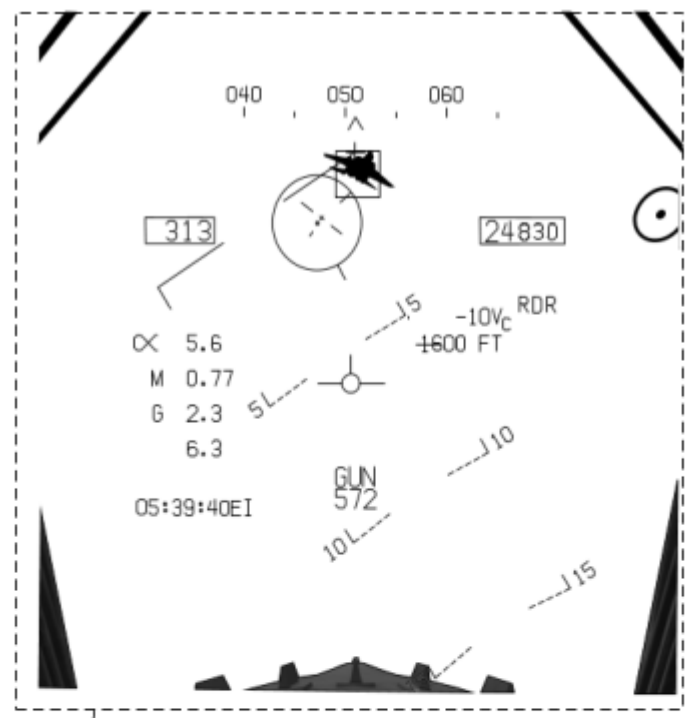
Problem



With the advent of quantum computing and the renewed will to return to the Moon and beyond, by now, man should be able to control machines and devices with just thoughts alone. Joysticks, touch-pads/screens, steering wheels, and TV remotes, by now, should be a thing of the past.

Bigger Problem



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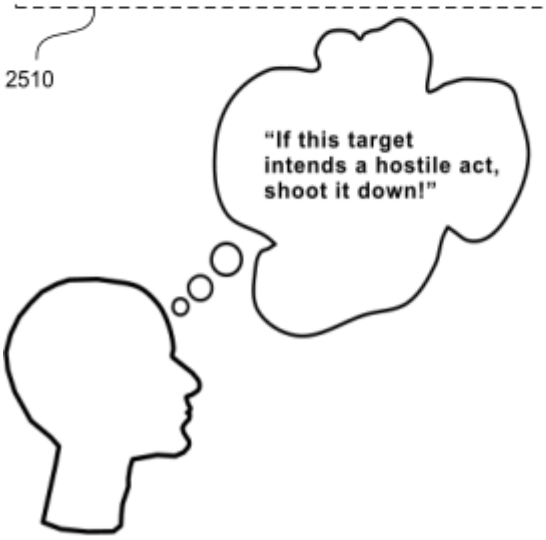

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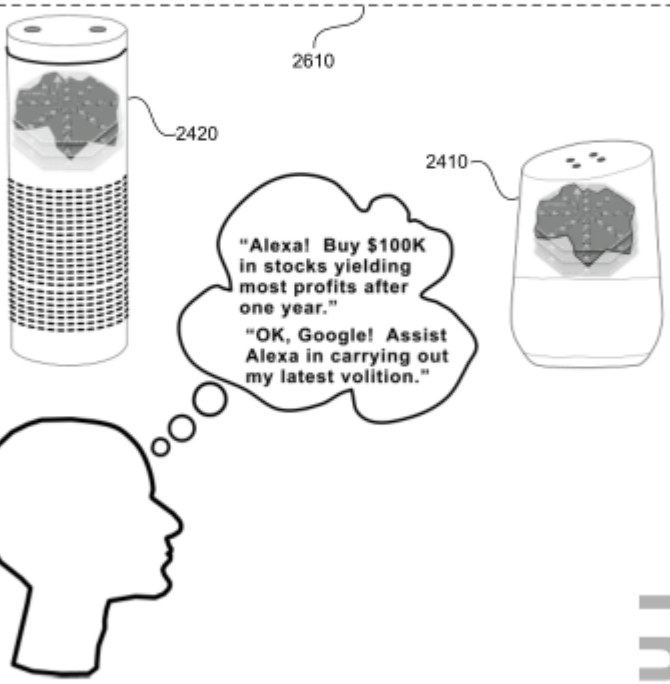
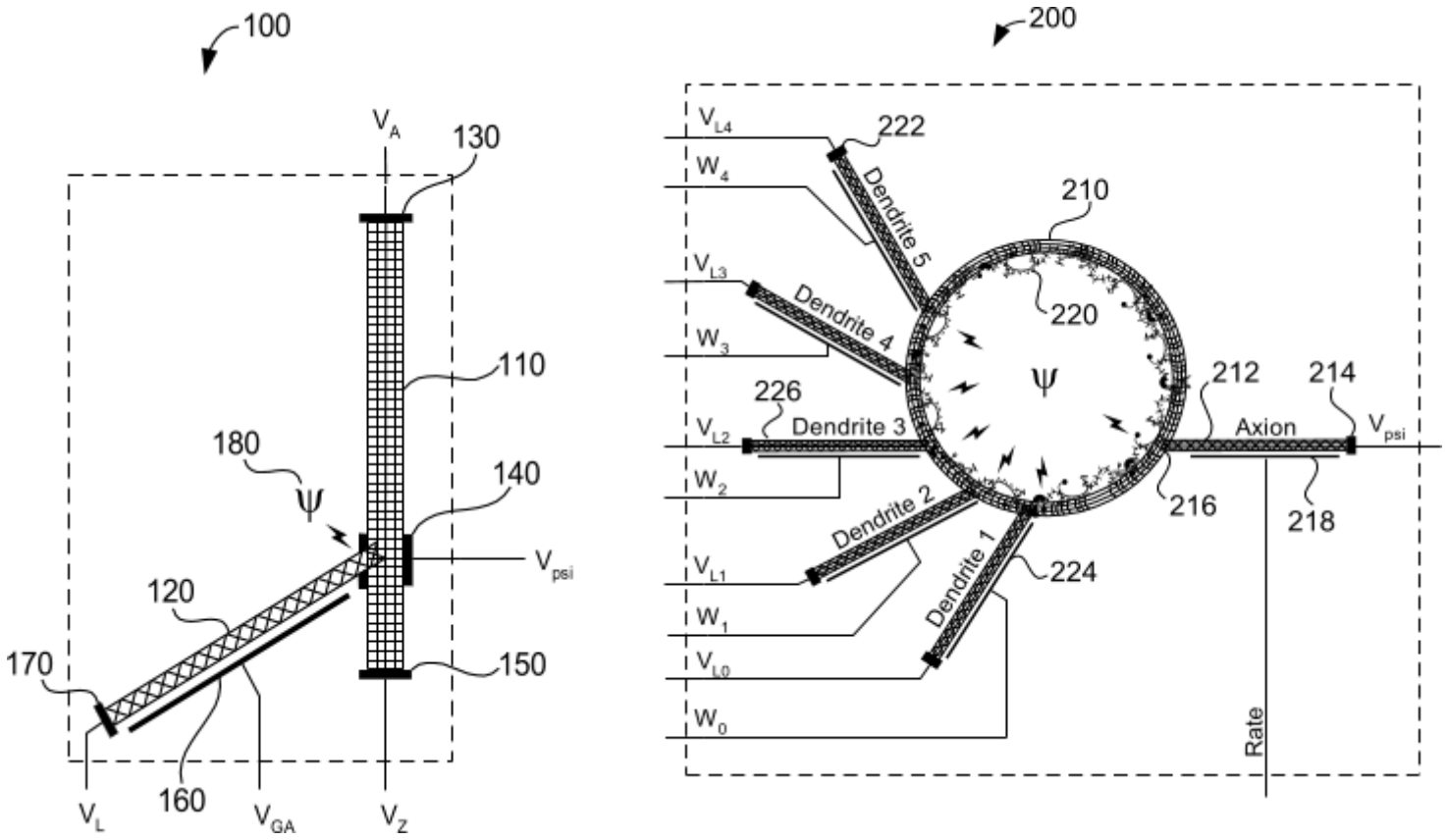


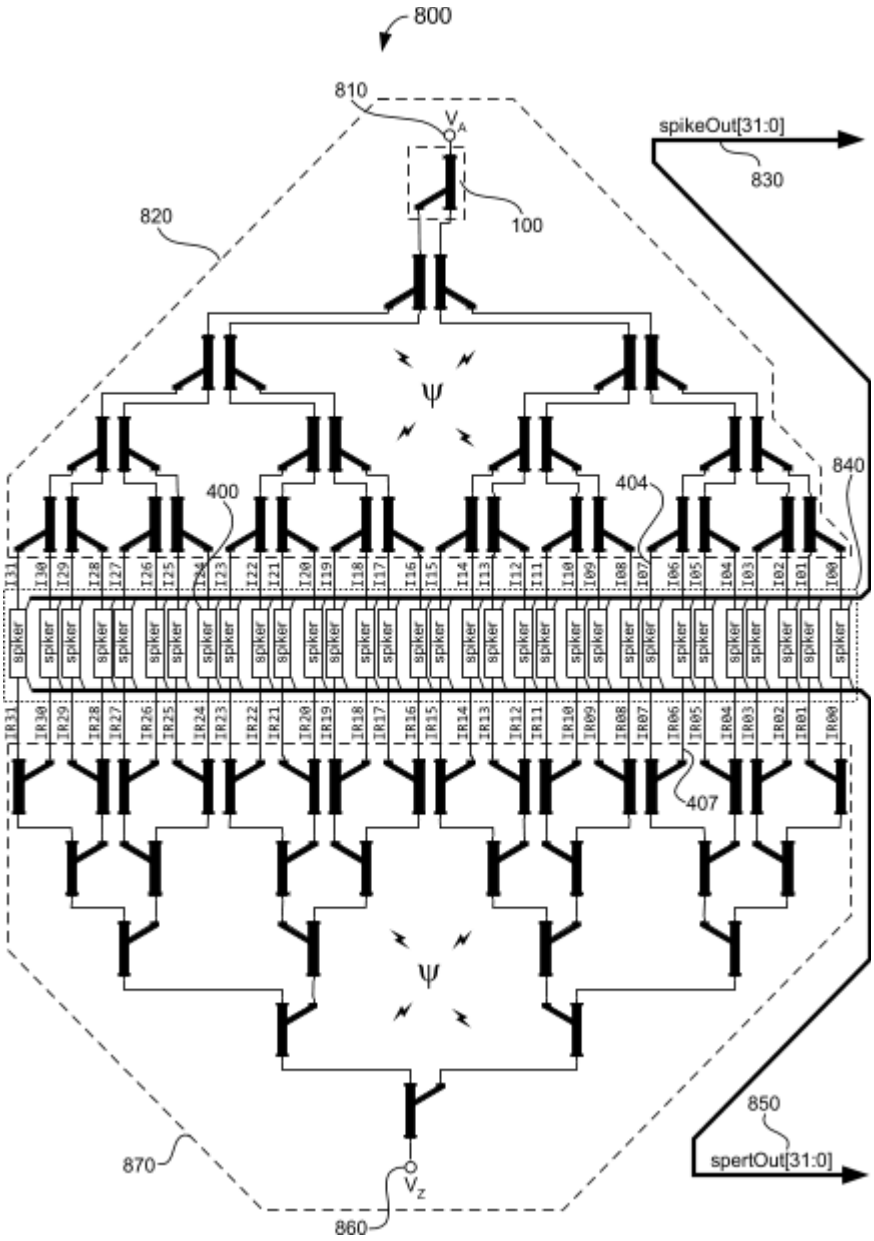
Controlling direction and magnitude with one's volition is one thing, but extracting information about a thing presents an even bigger problem. Like, for example, where does the information come from and, precisely, how to extract and make use of such information?

Solution (Part A)



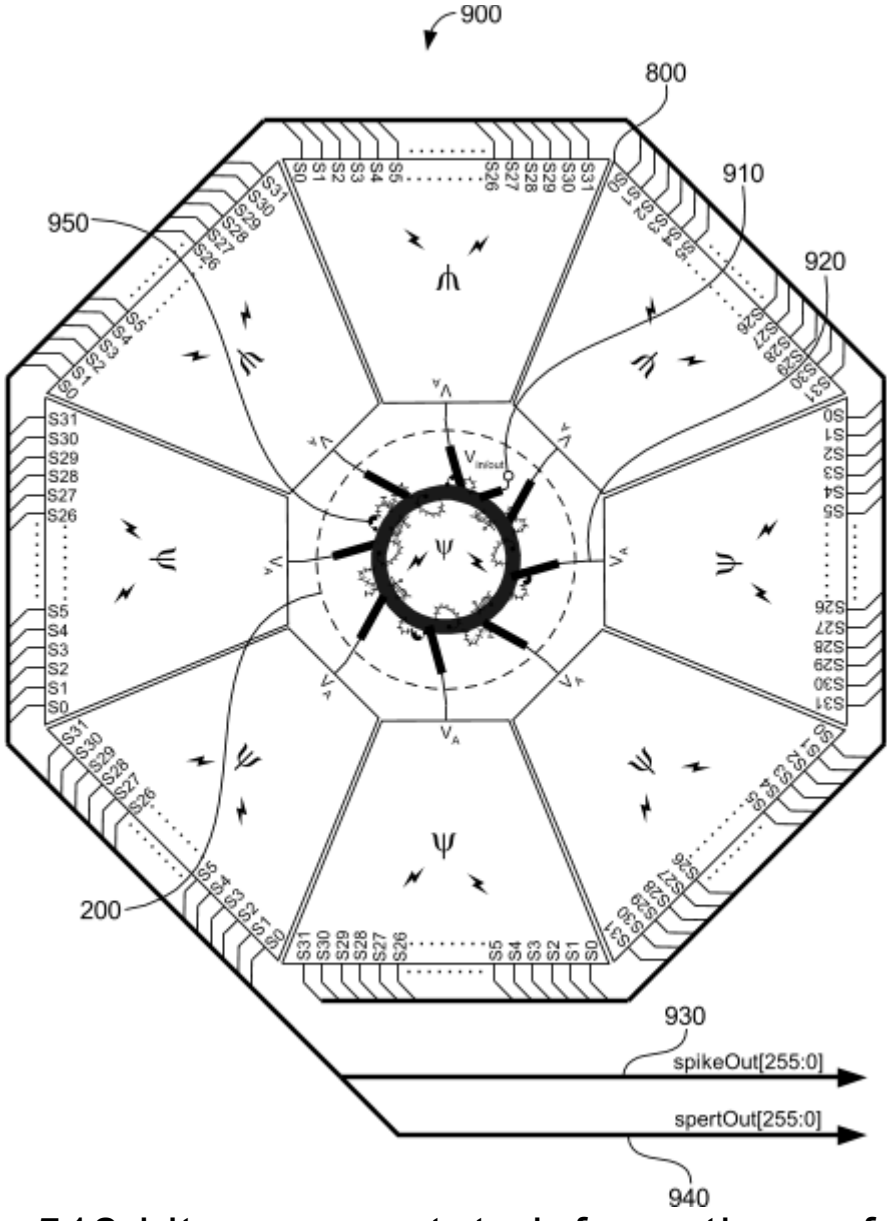
The solution to the previous slides employs a new science involving the most closely held non-secret there is. In a nutshell, all the information in the universe, past, present, and future is available and accessible via the tinniest bit of nothing found at the interior of a carbon nanotube or nanotoroid, i.e., the vacuum state, aka, the zero point. The information is all folded up. The challenge is figuring out how to tap into, unfold, and make use of it. **100** and **200** above show a conscious gate transistor (CGT) and artificial neuron built with carbon nanotubes and nanotoroid.

Solution (Part B)



Behold the vacuum state information unfolder. Only the first subsection shown here--there are eight of them--each built using qty. (62) conscious gate transistors. The percipient's volition influences current flow, i.e., which path to take at any given instant. The trillion dollar question of course, is, how does it know? Answer: it's conscious. Hint for dealing with it: everything you see here is at the atomic scale, hence it's quantum level stuff, meaning, classical physics does not necessarily apply.

Solution (Part C)



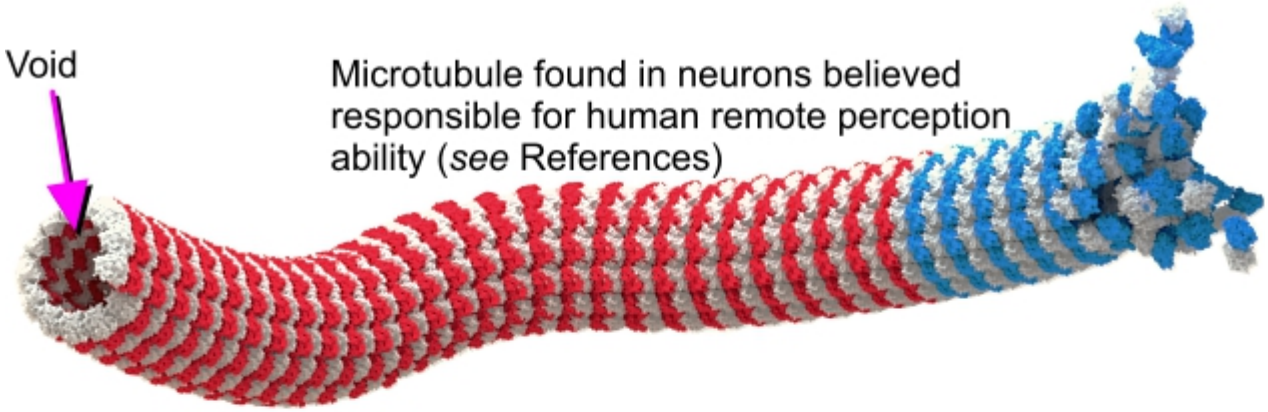
This is the 512-bit vacuum state information unfolder, minus the fused artificial spiking neural network circuitry and newly patented Instruction Set Architecture (ISA) compute engine used to process the information. The new ISA compute engine is needed here because it has the ability to compute using dual operands of up to 1024 bits each, every clock cycle. For more information, hyperlinks to the actual patent applications and other pertinent information are provided on the last slide.

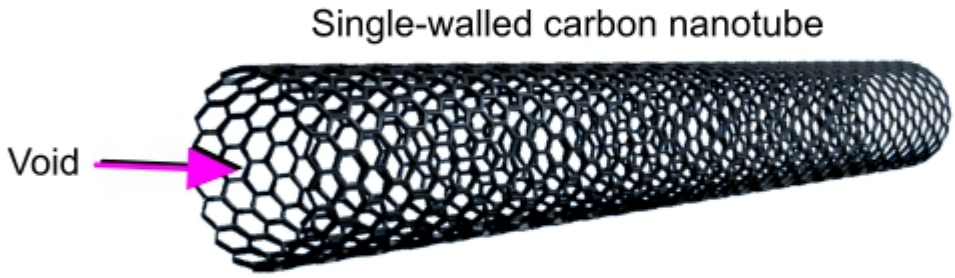
Value Proposition

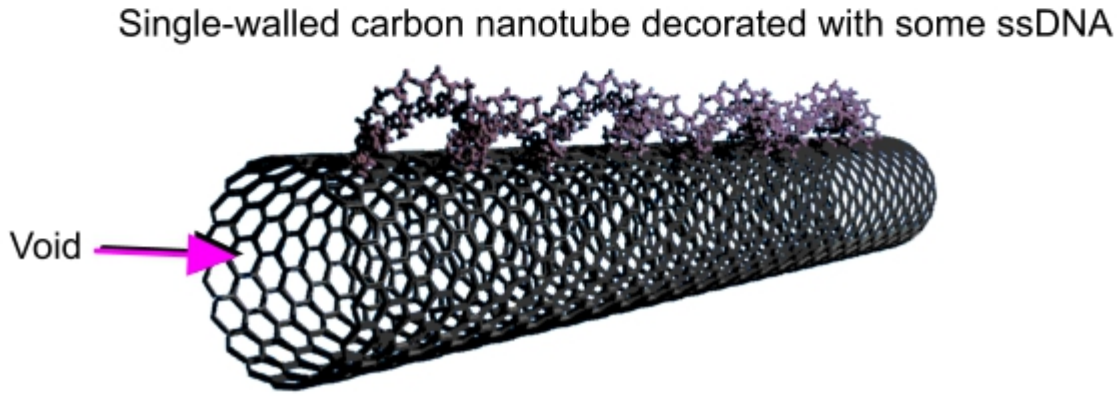
The new conscious gate transistor and vacuum state information unfolder technologies, along with the newly patented ISA compute engine technologies, will render all presently known quantum computer and microprocessor technologies obsolete. These new technologies, once employed, will forever alter the destiny of man.

Moreover, the new technology is not limited to use by humans alone. For example, with proper training of both the subject and the system using real-time feedback, a common brown bat will be able to pilot an F-22 fighter jet into combat and achieve a higher enemy kill rate than a human pilot. A pet dog will now be able to have a meaningful conversation--in English or other language--with its human master.

How/Why Does It Work?







All the information in the universe, past, present, and future (albeit all folded up) is available and accessible in places comprising the tiniest bit of nothing, i.e., the vacuum state or zero point. Due to their electrical properties, all of the above have the ability to be modulated by the very information that is conveyed through them, some configurations being more efficient or application-specific than others.

Current Status

A 91-page provisional patent application entitled, APPARATUS, SYSTEM, AND METHOD FOR CONSTRUCTING CONSCIOUS COMPUTERS AND MACHINES was filed with the USPTO July 20, 2020. A true and correct copy of it, along with official filing receipt, can be downloaded from the CGT repository at the link provided on the last slide.

The 102-page utility patent application (**17350805**) for the above invention was filed with the USPTO June 17, 2021. A true and correct copy of it, along with original electronic filing receipt, can be downloaded from the same repository at the link provided on the last slide.

According to 35 USC 122 and 37 CFR 1.211, the above utility application should have been officially published for public inspection at the USTPO website on or before January 28, 2022. To date, no secrecy order has been received. It is speculated that one possible reason for the delay in publishing, is so that the powers that be (and their compartmentalized contractors) can skirt the provisional rights granted to the inventor provided for under 35 USC 154 after publication, but while still pending, while “they” figure out not only the how and the why of the new science, but also possible work-arounds.

A list of References used in the research, including hyperlinks to the materials, can be downloaded at the link provided on the last slide.

Current Status (cont.)

A 137-page patent for one of the independent claims in the new ISA compute engine issued on March 15, 2022 as patent number **US 11,275,584 B2**. It can be downloaded at the link provided on the last slide.

Due to a unity of invention restriction, a first divisional application was filed on December 18, 2021. The application number is **17555408**. The first page and claims can be downloaded at the link provided on the last slide.

A second divisional application with a much broader claim than the issued patent above was filed on February 3, 2022. The application number is **17591963**. Both divisionals are officially published.

A version of the newly patented ISA has been prototyped in a $30 Lattice Semiconductor FPGA. An animated .gif file showing a demo and it running its on-chip real-time debugger can be seen at the link provided on the last slide.

Synthesizable Verilog RTL for the HedgeHog fused artificial spiking neural network for evaluation in a Xilinx Kintex Ultra FPGA can be downloaded at link provided on the last slide.

Business Model

The inventor will retain exclusive ownership of all right, title, and interest in and to the patents and patent applications. Licensing for the conscious gate transistor technology will not be available until after official publication of subject patent application.

Newly funded ThoughtChip will purchase a non-exclusive license from inventor using a portion of the proceeds raised from VC sources and will pay sales-based royalties quarterly to inventor for use of the patented and patent pending technology.

ThoughtChip will manufacture or have manufactured individual packaged CGTs, information unfolders, and various conscious computers, machines, and devices incorporating them.

Go-To-Market Plan

Alphabet/Google, IBM, Intel, Apple, Microsoft, Elon (to name a few,) might very well be among the chief investors (at least indirectly) and also most likely the primary customers of ThoughtChip's patented products. Most of these entities are already well aware of the technology, as most of them and the entire IEEE mailing list of various of its committees, received not only a copy of the provisional patent applications, but also the utility patent applications shortly after each was filed.

In fact, in response to one of such communications, a Fellow from the IEEE 754 Standards committee sent an email stating that they believe that one or more claims in the ISA application may be essential to the Standard and suggested that a FRAND Letter of Assurance (LOA) be sent to them. To date no such letter has been sent.

Management Team

Presently, there is no management team in place, meaning, investors will have to create one. Such management team will determine how much capital to raise and what it will be used for.

Caveat Emptor

Investors should be aware that another possible explanation as to why subject utility patent application has not yet been officially published at the USPTO website for public inspection is that it might possibly be under review by one or more agencies of the United States. Meaning, that if “they” are unable to come up with a work-around, “they” may be inclined to do a “taking” of private property under applicable law, and, in turn, license it out to companies of their choosing.

It is hoped that if funds can be raised and proper management team put in place, a taking will not be necessary.

Last Slide (links)

91-page conscious gate transistor provisional patent application with official filing receipt:

https://github.com/jerry-D/Conscious_Gate_Transistor/blob/master/ConsciouGateTransistor_Provisional_Application_merged.pdf

102-page conscious gate transistor utility patent application with electronic filing receipt:

https://github.com/jerry-D/Conscious_Gate_Transistor/blob/master/1618-0339_Nonprovisional_Application-merged.pdf

References used in the conscious gate transistor research:

https://github.com/jerry-D/Conscious_Gate_Transistor/blob/master/references_2021.pdf

137-page patent number US 11,275,584 B2:

https://github.com/jerry-D/HedgeHog-Fused-Spiking-Neural-Network-Emulator-Compute-Engine/blob/master/US-11275584-B2_I.pdf

First divisional patent application (first page and claims only):

https://github.com/jerry-D/HedgeHog-Fused-Spiking-Neural-Network-Emulator-Compute-Engine/blob/master/pub_17555408_merged.pdf

Second divisional patent application (first page and claims only):

https://github.com/jerry-D/HedgeHog-Fused-Spiking-Neural-Network-Emulator-Compute-Engine/blob/master/DIV2_P1_claims.pdf

Poster-sized HedgeHog fused artificial spiking neural network data sheet:

https://github.com/jerry-D/HedgeHog-Fused-Spiking-Neural-Network-Emulator-Compute-Engine/blob/master/HedgeHog.pdf

Commemorative ThoughtChip poster:

https://github.com/jerry-D/Conscious_Gate_Transistor/blob/master/ThoughtChip_Poster1.pdf

Commemorative IEEE 754 ISA compute engine poster:

https://github.com/jerry-D/SYMPL_IEEE754-2019_ISA/blob/main/SYMPL_IEEE_754_poster_v1_3.png

New ISA demos (gif):

https://github.com/jerry-D/SYMPL_IEEE754-2019_ISA/blob/main/SYMPL_RTMDX.gif

https://github.com/jerry-D/SYMPL_IEEE754-2019_ISA/blob/main/SYMPdemo2.gif

YouTube video showing operational Remote Viewers tackle the conscious gate transistor (read the video description at YouTube before watching):

https://youtu.be/Hdq3M4zQx_o