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25 July 2023

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(List of remaining 19 addressees continued after my signature.)

OPEN LETTER to the IEEE for a Fully Compliant IEEE 754-2019 Hardware Floating-Point Instruction Set Architecture (ISA) Compute Engine and Offer of Non-Exclusive Patent License

Dear Executives, Professors, Investors and Media:

The purpose of this Open Letter is multi-fold and concerns matters of immense public importance.

Firstly, to bring your attention to the fact that I recently received three US Patents relating to the world's first universal floating-point hardware compute engine capable of computing directly with dual, human-readable, decimal character sequence floating-point representation operands up to 20 significant decimal characters in length (i.e., IEEE 754 "H=20" double-precision) or integer operands up to 1024 bits (128 bytes) each, in any combination, and produce a computed result—EVERY clock cycle—without first having to explicitly convert the character representations in software to binary format.

The ISA is not a "load-store" architecture, but rather a "mover" architecture, because its hardware shell fundamentally only knows how to do one thing—MOV.

This newly patented IEEE 754-2019 floating-point Instruction Set Architecture (ISA) is the world's only ISA that can implement in hardware ALL floating-point operations mandated by the IEEE 754-2019 Standard (including ConvertFrom and ConvertTo “H=20” decimal character sequences) for conforming implementations, using a single instruction per floating-point operation.

Moreover, this new IEEE 754-2019 floating-point ISA is also the world's first, and only, ISA to completely dispense with the use of “opcodes” in the ISA instruction repertoire, thereby freeing the hardware from the cumbersome process of fetching, decoding, and executing them, making the new ISA way more efficient than the now obsoleted INTEL, AMD, ARM, Qualcomm, etc., architectures.

Because the new IEEE 754-2019 floating-point ISA can compute directly with dual, human-readable, decimal character sequence floating-point representations having up to H=20 significant decimal character digits in length, including those with “token” exponents, and produce a result every clock cycle, this ISA is ideal for AI applications that scour textual information from web pages, without the need for the cumbersome and inefficient task of explicitly converting these human-readable, textual floating-point representations to binary format before computing with them.

The US Patents that are concerned with the subject matter of this letter (“the patents”), are identified immediately below.

US Patent No.: **US 11,275,584 B2**, entitled: **UNIVERSAL FLOATING – POINT INSTRUCTION SET ARCHITECTURE FOR COMPUTING DIRECTLY WITH DECIMAL CHARACTER SEQUENCES AND BINARY FORMATS IN ANY COMBINATION**, filed: Jul . 30 , 2020, issue date: Mar. 15 , 2022;

US Patent No.: **US 11,635,956 B2**, entitled: **FULLY PIPELINED HARDWARE OPERATOR LOGIC CIRCUIT FOR CONVERTING HUMAN-READABLE DECIMAL CHARACTER SEQUENCE FLOATING-POINT REPRESENTATIONS TO IEEE 754-2008 BINARY FLOATING-POINT FORMAT REPRESENTATIONS**, filed: Dec. 18,2021, issue date: Apr. 25, 2023; and

US Patent No.: **US 11,635,957 B2**, entitled: **HARDWARE-IMPLEMENTED UNIVERSAL FLOATING-POINT INSTRUCTION SET ARCHITECTURE FOR COMPUTING DIRECTLY WITH HUMAN-READABLE DECIMAL CHARACTER SEQUENCE FLOATING-POINT REPRESENTATION OPERANDS**, filed: Feb. 3, 2022, issue date: Apr. 25, 2023.

I am the sole inventor and exclusive owner of all right, title, and interest to/in the patents. If your respective organization would like to obtain a non-exclusive, commercial license under the patents, please don't hesitate to contact me, as I would be happy to provide your organization with one or more licenses under negotiated terms.

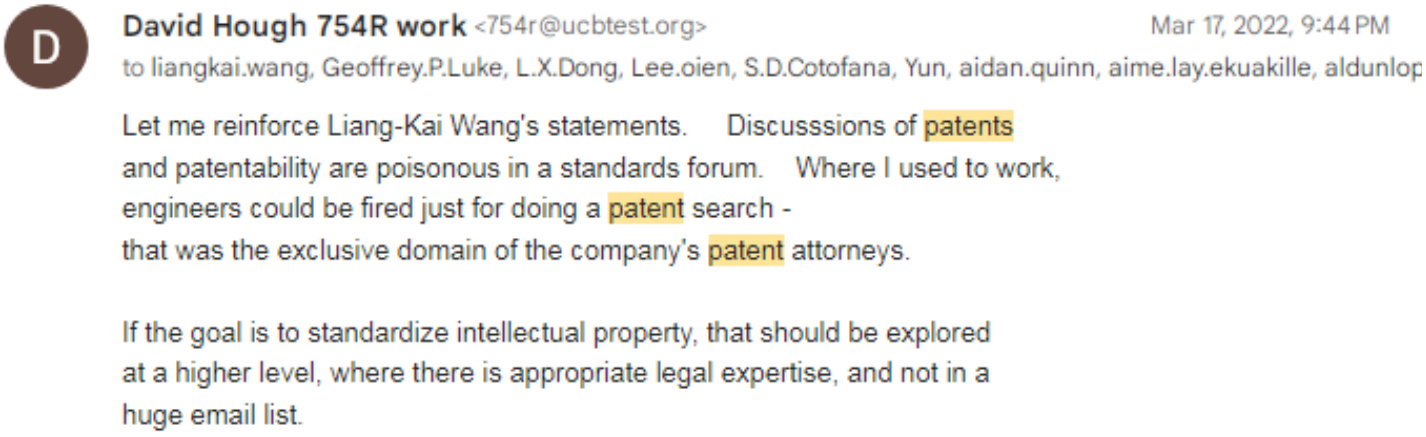
Secondly, I would like to propose that the IEEE adopt the new IEEE 754-2019 floating-point ISA as a new Standard for FULLY compliant hardware implementations of the Standard. Main reason (there are several) why I believe it should, is Claim 1 of the '**957** patent cited above, which reads as follows:

> "1. A universal floating-point Instruction Set Architecture (ISA) compute engine implemented entirely in hardware, said ISA compute engine comprising:
>
> means for converting human-readable decimal character sequence floating-point representation operands to binary format without explicitly performing a conversion-to-binary-format process in software; and
>
> means for computing directly with the converted human-readable decimal character sequence floating-point representation operands."

As can be seen from Claim 1 above, it is very broad. To move beyond the Dark Ages of ARM and INTEL architectures, into the future realm of AI, industry requires this ISA—*per se*—because there is no way around it.

A little over a year ago, I attempted to raise the issue with the IEEE 754 Floating-Point Standards committee, but was immediately chastised by several of its "Fellow" and "Program Manager" members, as if I had committed some kind of crime for getting patents covering operations mandated by IEEE 754 for conforming implementations implemented entirely in hardware. One of these communications from an IEEE Standards Program Manager suggesting that the patents are potentially essential to the IEEE 754 Standard.

So you can see what I'm talking about, here are just a couple screen captures of such responses from the group:



D

David Hough 754R work <754r@ucbtest.org> Mar 17, 2022, 9:44 PM

to liangkai.wang, Geoffrey.P.Luke, L.X.Dong, Lee.oien, S.D.Cotofana, Yun, aidan.quinn, aime.lay.ekuakille, aldunlop

Let me reinforce Liang-Kai Wang's statements. Discusssions of patents and patentability are poisonous in a standards forum. Where I used to work, engineers could be fired just for doing a patent search - that was the exclusive domain of the company's patent attorneys.

If the goal is to standardize intellectual property, that should be explored at a higher level, where there is appropriate legal expertise, and not in a huge email list.

Tom Thompson <thomas.thompson@ieee.org> Fri, Mar 18, 2022, 2:22 PM

to me, David

Hello Mr. Harthcock,

I am sending this email as a follow-up to your original email dated March 17, 2022.

Please be advised that it is against the IEEE Privacy policy to send email correspondence to a list of email addresses. In the future, I would ask that you send any IEEE 754-2019 related inquiries to the Working Group (WG) Chair, David Hough (copied above), or myself as the staff Progam Manager. At present this WG is not actively working on any updates or revisions to the IEEE 7540-2019 standard. If you are interested in being notified in the future of any new work by this WG you can indicate your interest via our myProject system.

With respect to the patent information. Please note that IEEE Standards Association (IEEE SA) WGs are not permitted to discuss any potential essential patient claims. You can find information on the IEEE SA Patent Policy on the Patent Committee section of the IEEE SA website or in Clause 6 of the IEEE SA Standards Board Bylaws.

I hope this information is helpful. Should you have any further questions please feel free to contact me.

Regards,

Tom Thompson
Program Manager
+1 732-562-5564 | standards.ieee.org

IEEE SA
STANDARDS ASSOCIATION

Dr. Hough, who is with Oracle, claims that discussing patents in a standards forum is "poisonous," without explaining why he believes that. I can only surmise that he believes such discussions are poisonous because forum members are employees of publicly-traded companies that hope to avoid enhanced damages for willful infringement of the patents being discussed in the forum that are potentially essential to the Standard.

In other words, I surmise that such companies' default mindset is to go ahead and start using whomever's patented technology now and then only pay up if and when they get caught, their reasoning being, why pay now when they only "might" have to pay later. And if caught, plead ignorance on foreknowledge of the patents in suit so as to escape enhanced damages for willfulness.

In my opinion, this is why, according to Mr. Thompson above, it's against IEEE policy to discuss patents in Standards forums. The companies whose employees are engaging in Standards discussions don't want them to become tainted with knowledge about patents that are potentially essential to the Standard. Again, why pay now when you can pay later, and only if caught. This, in my opinion, is very close to cartel-like behavior, because, from my perspective as "the little

guy" consumer and non-IEEE member, I have no voice because us little people have been shut out by Standards-setting members who are employees of publicly traded corporations. This is not fair.

Thirdly, now that I have gotten that off my chest, I will now make the following suggestion to the IEEE and the corporations whose employees make up the Standards committees there—this one time and one time only—that such corporations form a IEEE 754 Floating-Point ISA Consortium and pass the "kitty" around. If such Consortium can do that, there might be enough in the kitty that can be used to twist my arm hard enough so that I tap out and let go of the patents. Assuming, *arguendo*, that I do let go of the patents in that scenario, the IEEE/Consortium can do whatever they it wants with them.

Stated another way, if these corporate members are so concerned about getting caught, why not see if Jerry's arm can be twisted into letting go of them, in that, the last time I checked, such companies most likely have enough wherewithal between them to twist pretty darn hard. All it requires is setting aside some ego and corporate greed to make it happen.

As a note on this point, I visited Yahoo Finance online and looked up the publicly traded companies' market capitalization as of July 25 and added them up. It comes out to be roughly $15.845 Trillion total market capitalization between just the ones in the addressees list. So it seems to me that it shouldn't be that big of a problem.

Please be informed that if you'd like to discuss licensing and/or do any arm-twisting, you'd have to do that directly with me, as I am not a lawyer and do not plan to be represented by one outside the US Patent and Trademark Office. If you need to contact me, just use the email address under my signature.

Also be informed that if you'd like to evaluate the ISA, there is an evaluation version of the HedgeHog Fused Artificial Spiking Neural Network that incorporates it and which you can download for free at my GitHub repository. Among the things that can be found there is a version of the open-source CustomASM table-driven cross-assembler that I modified to support the new ISA and it includes a custom rule table I created to support the new ISA.

A link to my GitHub repository is under my signature. For more information about me personally, I've provided a link to my FaceBook timeline, also after my signature.

Fourthly, is the fact there is yet another pending patent application, which in the context of AI, is inextricably connected to the patents mentioned above and this is why I bring it to your attention now. The pending patent application is identified as:

US Patent Application No.: **17/350,805**, Publication No .: **US 2022/0376193 A1**, entitled: **COMPLEX NANOSTRUCTURE CONFIGURABLE AS A TRANSISTOR, MULTIPLEXER, OR INFORMATION UNFOLDER**, filed: June 17, 2021, publication date: Nov. 24 , 2022.

I am the sole inventor and exclusive owner of all right, title, and interest to/in the pending patent application. Based on a new science, the pending patent application discloses, among other things, a new kind of carbon nanotube transistor (CNT) that can be perturbed using human volition alone. It also discloses is a new kind of multiplexer built from CNTs and nano-toroid.

Most importantly, especially as the pending patent application relates to AI generally and conscious computers and machines particularly, it discloses a new kind of information unfolder also built from these specially configured CNTs and optional nano-toroid, which is able to extract information from the vacuum state (sometimes referred to as the zero point) and unfold it with the aid of a properly trained artificial neural network such as the HedgeHog described above. A poster-sized information sheet of the HedgeHog is available for free download at my repository using the GitHub link under my signature.

I bring it up because I would like to raise enough money thru licensing of the patents to start a new company named ThoughtChip. Among the first capital purchases would be several Focused Ion Beam Microscopes (FIBs), Atomic Force Microscopes (AFMs), bonding machines, etc., everything I would need to start producing evaluation versions of the invention stack-mounted on Analog Devices AD8229 instrumentation amplifiers.

Also for your information, there is a ThoughtChip “pitch-deck” located in my repository at GitHub in case you'd like to have a look at how to prototype one stack-mounted on an Analog Devices AD8229 instrumentation amplifier, if you think you might be interested in participating in that startup.

I thank you for your time and consideration.

Sincerely,

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