Amber ARM-compatible core :: Overview

Details

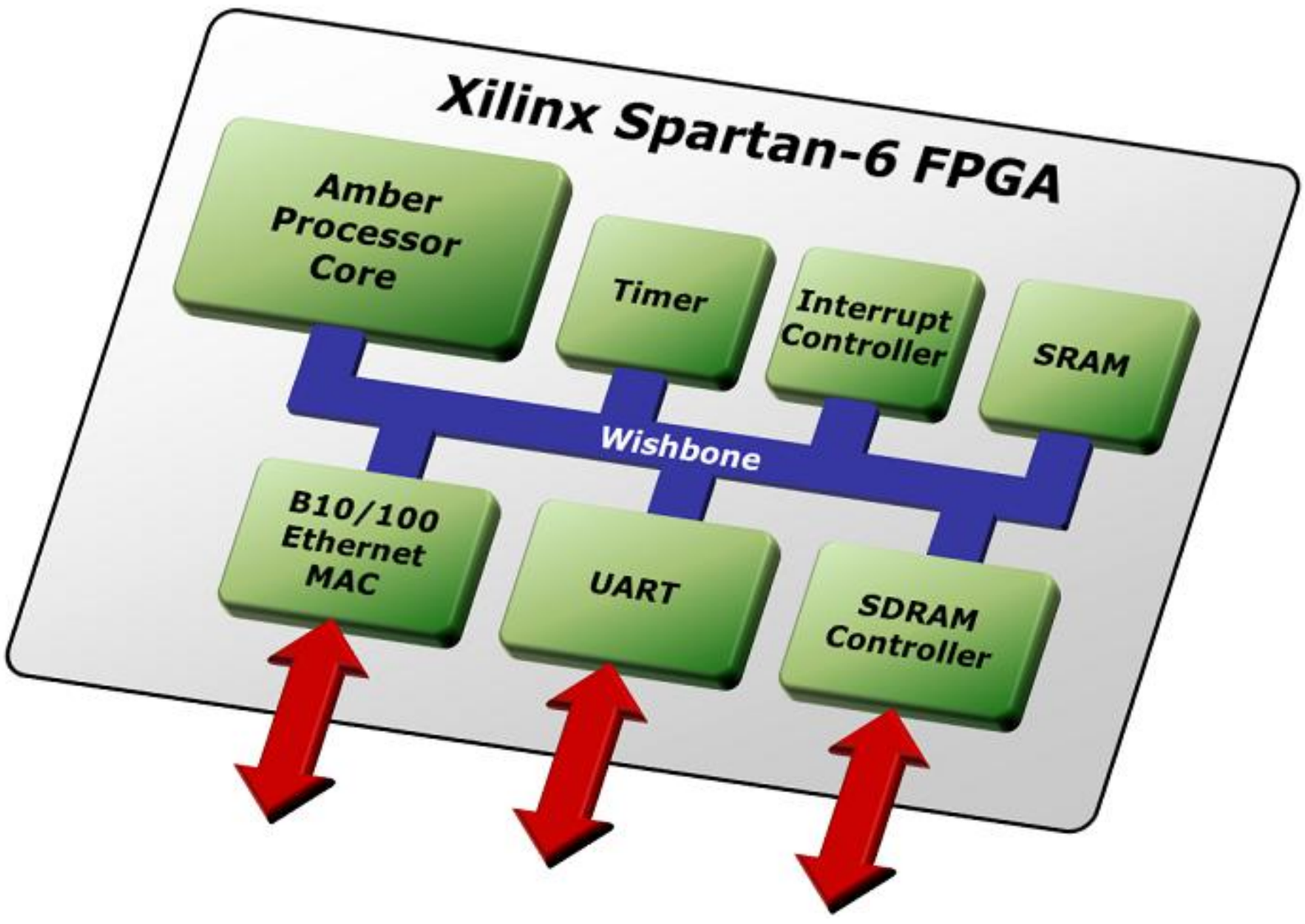
Name: amber
Created: Dec 23, 2010
Updated: Nov 30, 2014
SVN Updated: May 20, 2013
SVN: Browse
Latest version: download
Statistics: View

Other project properties

Category: Processor
Language: Verilog
Development status: Stable
Additional info: Design done, FPGA proven, Specification done
WishBone Compliant: Yes
License: LGPL

Description

The Amber processor core is an ARM-compatible 32-bit RISC processor. The Amber core is fully compatible with the ARM® v2a instruction set architecture (ISA) and is therefore supported by the GNU toolset. The Amber project provides a complete embedded system incorporating the Amber core and a number of peripherals, including a UART, a timer and an Ethernet MAC.



There are two versions of the core provided in the Amber project. The Amber 23 has a 3-stage pipeline, a unified instruction & data cache, a 32-bit Wishbone interface, and is capable of 0.75 DMIPS per MHz. The Amber 25 has a 5-stage pipeline, seperate data and instruction caches, a 128-bit Wishbone interface, and is capable of 1.05 DMIPS per Mhz. Both cores implement exactly the same ISA and are 100% software compatible. The cores do not contain a memory management unit (MMU) so they can only run the non-virtual memory variant of Linux. The cores has been verified by booting a 2.4 Linux kernel.

The cores were developed in Verilog 2001, and are optimized for FPGA synthesis. For example there is no reset logic, all registers are reset as part of FPGA initialization. The complete system has been tested extensively on the Xilinx SP605 Spartan-6 FPGA board. The full Amber system with the A23 core uses 32% of the Spartan-6 XC6SLX45T-3 FPGA Look Up Tables (LUTs), with the core itself occupying less than 20% of the device using the default configuration, and running at 40MHz. It has also been synthesized to a Virtex-6 device at 80MHz.

The older v2a version of the ARM instruction set is supported because it is still

fully supported by the GNU tool chain and is not covered by patents so can be implemented without a license from ARM. For a description of the ISA, see
Archimedes Operating System - A Dabhand Guide or
Acorn RISC Machine Family Data Manual

For project documentation, see amber-user-guide.pdf and amber-core.pdf.