CHE-MING, CHANG

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EDUCATION

Incoming Ph.D. candidate in Electrical and Computer Engineering, Georgia Institute of Technology
Advisor: Prof. Sung-Kyu Lim
Research Topic: AI/ML-driven EDA for heterogeneous integration

B.S. in Electrical Engineering, National Taiwan University Sept., 2020 - Jun., 2024
Overall GPA: **4.17 / 4.30**
Dean's List Award 2023 Spring
TSMC Semiconductor Advanced IC Design Program in National Taiwan University

Highlighted Coursework: Logic Synthesis and Verification, Physical Design for Nanometer ICs, Integrated Circuit Design, Computer-aided VLSI System Design, Digital Signal Processing in VLSI, Machine Learning

PUBLICATION

[1] **Che-Ming Chang**, Jie-Hong Roland Jiang, Dah-Wei Chiou, Ting Hsu and Guin-Dar Lin, "Quantum Circuit Compilation for Trapped-Ion Processors with the Drive-Through Architecture," in *IEEE Trans. Quantum Eng.*, vol. 6, pp. 1-14, 2025.

[2] Cheng-Yu Chiang, Yi-Hsien Chiang, Chao-Chi Lan, Yang Hsu, **Che-Ming Chang**, Shao-Chi Huang, Sheng-Hua Wang, Yao-Wen Chang, and Hung-Ming Chen, "Mixed-Size Placement Prototyping Based on Reinforcement Learning with Semi-Concurrent Optimization," in *Proc. of ASPDAC*, Tokyo, Japan, January 2025, pp. 893–899.

[3] **Che-Ming Chang**, Prashanth Vijayaraghavan, Charles Mackin, Ashutosh Jadhav, Hsinyu Tsai, Vandana Mukherjee and Ehsan Degan, "Enhancing LLMs for HDL Code Optimization using Domain Knowledge Injection," *Under Review*, 2025.

[4] Shao-Yu Lo, **Che-Ming Chang**, Yao-Wen Chang, "Warpage Modeling for Advanced Packaging with DeepONet-Based Operator Learning," *Under Review*, 2025.

[5] Yi-Hsien Chiang, Cheng-Yu Chiang, **Che-Ming Chang**, Chao-Chi Lan, Shao-Chi Huang, Sheng-Hua Wang, Yao-Wen Chang, "Correlation-Aware Representation Learning and Clustering for Reinforcement Learning-Based Mixed-Size Placement," *Under Review*, 2025.

RESEARCH EXPERIENCE

Electronic Design Automation Lab Aug., 2023 - Jan., 2025
Research Assistant, Advised by Prof. Yao-Wen Chang *Taipei, Taiwan*

Mixed-Size Placement Prototyping Based on Reinforcement Learning with Semi-Concurrent Optimization [2]

- Proposed an innovative method to move all macros concurrently and iteratively by a deep Q-network model as an agent in reinforcement learning (RL) in contrast to previous works that place them sequentially.
- Demonstrated 12.3% / 9% additional HPWL reduction on ISPD'05 benchmarks compared to DREAMplace / modern ML-based placer GraphPlanner.

Warpage Modeling for Advanced Packaging with DeepONet-Based Operator Learning

- Developed a convolutional neural network (CNN)-based deep operator network (DeepONet) to predict warpage in advanced packaging designs.
- Achieved 435× speedup over an 8-multiprocess finite element method (FEM) while maintaining an average warpage error of 1.9%.

IBM Almaden Research Center, AI for EDA group Jun., 2024 - Sept., 2024
Research Intern, Advised by Prashanth Vijayaraghavan *San Jose, CA, USA*

Enhancing LLMs for HDL Code Optimization using Domain Knowledge Injection

- Proposed RTLOpt, the first comprehensive dataset designed to evaluate RTL optimization techniques, including pipelining and clock gating.
- Introduced MASCOT, a framework for HDL code optimization by injecting and retrieving domain-specific knowledge into the code generation process, aided with compiler and simulator feedback.
- Achieved 20% / 10% improvements for larger LLMs /small fine-tuned LLMs compared to zero-shot and ReAct / Chain-of-Thought baseline on HDL optimization tasks.

Applied Logic and Computation in System Design Lab Sept., 2022 - June, 2024
Research Assistant, Advised by Prof. Jie-Hong Roland Jiang *Taipei, Taiwan*

Quantum Circuit Compilation for Trapped-Ion Processors with Drive-Through Architecture [1]

- Proposed an analytical method to compile a QASM circuit onto a "drive-through" modular architecture by gate partitioning followed by a fidelity-aware placement.
- Achieved 10.8% / 9.6% higher fidelity compared to modern qubit mappers SABRE / t|ket⟩, while ensuring the practicality and scalability of our approach.

PROJECT EXPERIENCE

Approximate Logic Synthesis with Multi-Objective Simulated Annealing Oct., 2023 - Dec., 2023
Final Project in Logic Synthesis and Verification, GitHub *Taipei, Taiwan*

- Utilized multi-objective simulated annealing to synthesize approximate circuits within the given error bound based on the synthesis tool ABC.
- Demonstrated substantial area reduction (8-98%) over IWLS benchmarks within 1% error rate and shows quality (5-91%) and runtime improvements over the existing ALS tool ALSRAC.

QR decomposition engine for 5G MIMO demodulation Oct., 2023 - Dec., 2023
Final Project in Computer-aided VLSI System Design *Taipei, Taiwan*

- Implemented QR decomposition engine with 2.2% soft LLR error rate in Verilog.
- Achieved 206 MHz operating frequency with 37.5 mW power under TSMC 130nm technology with full VLSI design flow (RTL to GDS).

Real-Time FPGA-based Acoustic Imaging Nov., 2022 - Jan., 2023
Final Project in Laboratory of Digital Circuit System, GitHub *Taipei, Taiwan*

- Implemented a low-complexity delay-and-sum algorithm on Altera DE2-115 FPGA using SystemVerilog to visualize the position of sound sources in real-time via VGA output.
- Demonstrated significant reduction in implementation cost compared to currently high manufacturing costs.

AWARDS AND HONORS

Taiwan Chip-based Industrial Innovation Program Research Scholarship, NSTC Sep, 2024 - Jan. 2025
Scholarship for Overseas Internship Program, NTU / Ministry of Education June, 2024 - Aug. 2024
Research Scholarship, MediaTek-NTU Research Center Mar., 2024- June, 2024
Second Prize and Global Nominee, NASA Space App Challange Oct., 2023
College Student Research Scholarship, National Science and Technology Council Aug., 2023 - Feb., 2024
Dean's List Award 23'Spring, NTU June, 2023

SKILLS

Languages	Mandarin (Native), English (Proficient)
Programming Languages	C/C++, Python, Verilog, SystemVerilog, MATLAB, Javascript, LaTeX
Experience with EDA Tools	Synopsys VCS / DC / PT, Cadence Innovus, Berkeley ABC, Yosys