

**PE-xxxx
Revision B**

WS1050 MEMS CYCLING AND HOLD DOWN

TEST PROCEDURE

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1. Purpose and Scope

1.1 Purpose

This document defines the procedures and requirements for cycling and continuous hold down stresses for MEMS tunable capacitors.

1.2 Scope

This procedure applies to the qualification and ongoing production monitoring of WS1050.

2. Responsibilities

The Product Engineering function is responsible for assuring compliance to the requirements of this document.

3. REFERENCE DOCUMENTS

Document No.	Document Name
PE-0002	Equipment Calibration Procedure

[Table 1 Reference Document List](#)

4. FORMS

Form No.	Form Name

[Table 2 Form List](#)

5. DEFINITIONS (Not Applicable)

6. EQUIPMENT AND MATERIALS

Equipment consists of:

Item	Model	Manufacturer	Comments
Computer (equipment controller)	PC with Window XP, 7	Any	
Software (equipment controller)	LabView 2012 or Higher		
GPIO-USB-HS	778927-01	National Instruments	
Triple Output Power Supply	E3631A	Agilent/Keysight	w/ GBIP interface
Source Meter	2400	Keithley	w/ GBIP interface
DMM	2000	Keithley	w/GPIB interface
FPGA	PIX-7813R	National Instruments	
PXI Card Chassis	PIX-1033	National Instruments	
DUT boards	Various ¹	---	WiSpry Design
SHC68-68-RDIO Shielded Cable	191667-01	National Instruments	NI Cables

[Table 3 MEMS Reliability Stress Stand Equipment List](#)

Notes:

¹ WS1050 board is 36 positions (model WS-EVB-165)

7. REQUIREMENTS AND PROCEDURES

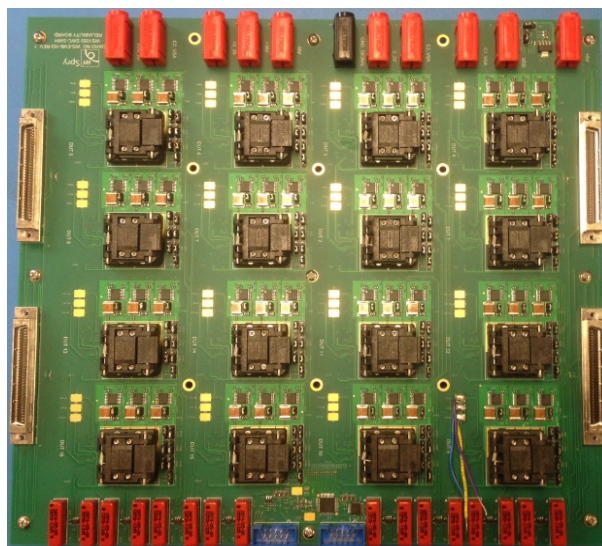
7.1 Basic Hardware, Software, and Environmental Requirements

7.1.1 Cycling and hold down hardware (boards, cables, connectors, bench equipment) must be able to:

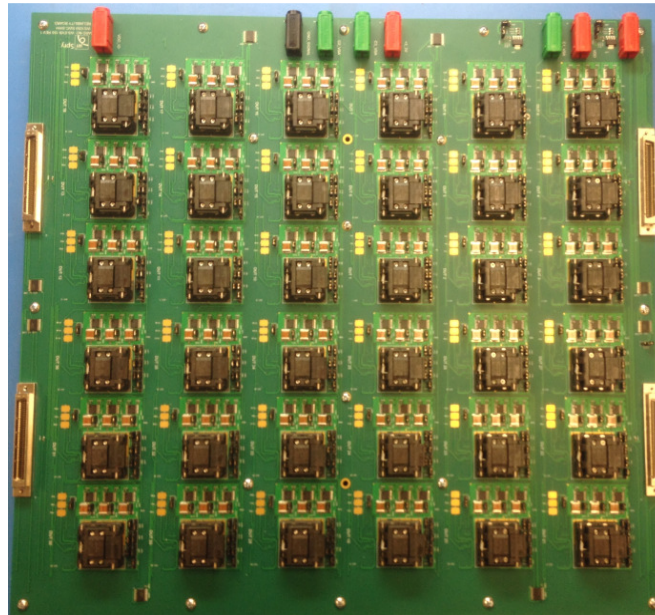
7.1.1.1 Meet the electrical conditions specified in sections 7.2 and 7.3.

7.1.1.2 Meet WiSpry calibration requirements specified in PE-0002.

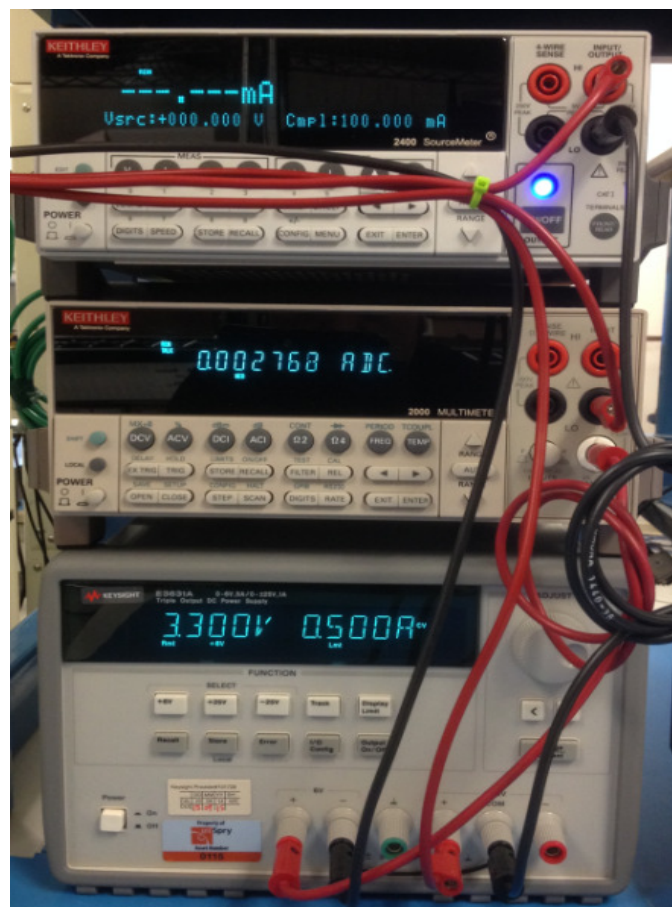
7.1.1.3 Be sufficiently robust to ensure minimum leakage currents.



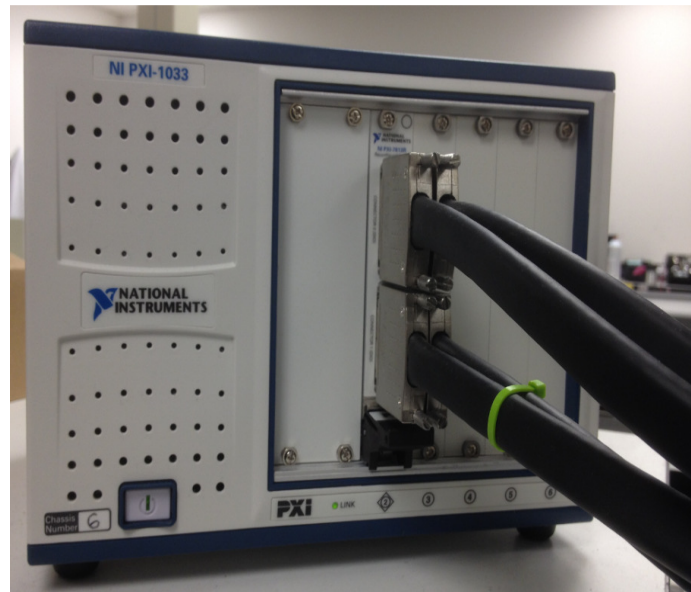
[Picture 16 DUT Board](#)



Picture 2 36 DUT Board



Picture 3 Test Equipment



Picture 4 Chassis and NI Cables

- 7.1.2 Cycling and hold down software should:
 - 7.1.2.1 Allow for insitu monitoring for stiction events.
 - 7.1.2.2 Meet the electrical conditions specified in sections 7.2 and 7.3.
- 7.1.3 Cycling and hold down environmental controls shall:
 - 7.1.3.1 Provide control of temperature and humidity.
 - 7.1.3.1.1 The ESPEC where we can control the temperature and humidity

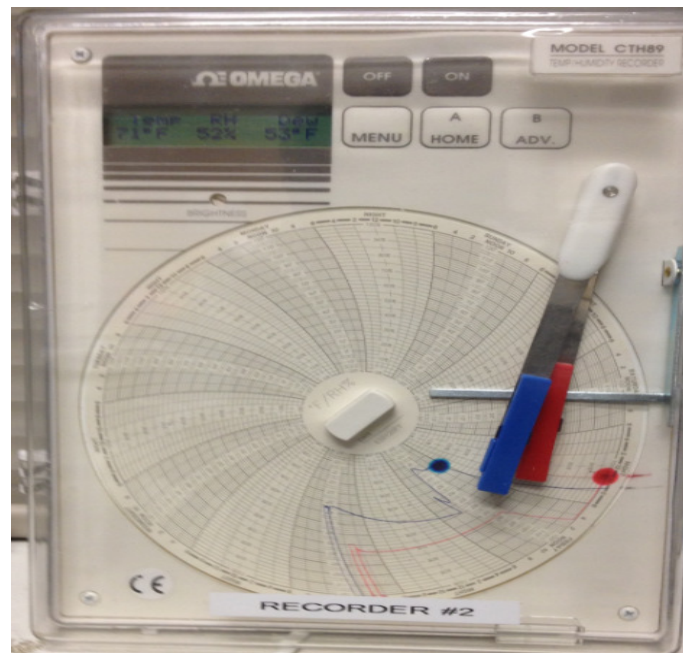


Picture 5 the ESPEC Oven Controls Temperature and Humidity

- 7.1.3.1.2 Yamato ovens where we control temperature, not humidity. But lab humidity is monitored by using OMEGA model CTH89



Picture 6 the Yamato Oven Controls Temperature



Picture 7 the OMEGA Monitors the Lab Humidity

- 7.1.3.2 Meet calibration requirements defined in PE-0002.

7.2 MEMS Switch Cycling Stress

The cycling conditions for product qualification and ongoing monitoring are:

Stress Condition	Requirement
MEMS Operating Voltage (V_{OP})	44 V
V_{DD}	3.7 V @ 12 KHz
Temperature	65 °C
Frequency	12 KHz
Duty Cycle	25%
Dual Voltage Actuation (DVA)	OFF
Beam Actuation	All beams cycles simultaneously
Beam Read Points	0, 2K, 10K, 100K, 1M, 5M, 10M, 20M, 30M ... TTF
Test Sequence	In series: Bank 1, Bank 2, then Bank 3

[Table 4 MEMS Switch Cycling Stress Conditions for Product Qualification](#)

7.3 MEMS Continuous Hold Down Stress

The continuous hold down conditions for product qualification and ongoing monitoring are:

Stress Condition	Requirement
MEMS Operating Voltage (V_{OP})	44 V
V_{DD}	3.3 V
Temperature	65 °C
Frequency	----
Duty Cycle	100%
Dual Voltage Actuation (DVA)	OFF
Beam Actuation	All beams cycles simultaneously and held for the stress duration
Beam Read Points	0, 5m, 10m, 15m, 30m, 45m, 60m, 90m ... 5h, 6h, 7h ... TTF
Test Sequence	In series: Bank 1, Bank 2, then Bank 3

[Table 5 MEMS Continuous Hold down Stress Conditions for Product Qualification](#)

7.4 General Set-up and Handling Guidelines

- 7.4.1 Device Under Test (DUT) should be handled according to class 1 procedure (ESD)
- 7.4.2 Stabilize oven temperature prior to loading parts, 15 minutes minimum
- 7.4.3 Preconditioning of new stress boards (to remove excess absorbed moisture), 24 hour bake at 85C
- 7.4.4 Socket inspection after each run and cleaning/repair as required

7.5 Test Set-up Procedure

7.5.1 Figure 1 shows the test set-up block diagram for WS1050 Reliability Test, Multi DUT.

7.5.1.1 Using banana plug cables to connect all test equipments as in Figure 1.

7.5.1.2 For power supply E3631A, use channel 1 for VDD, channel 2 for +3.3V.

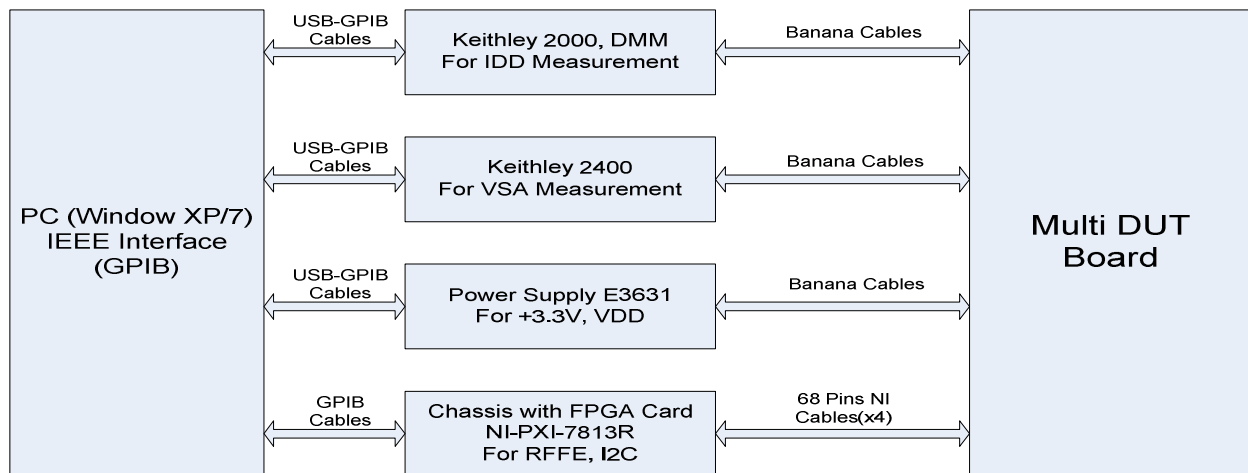
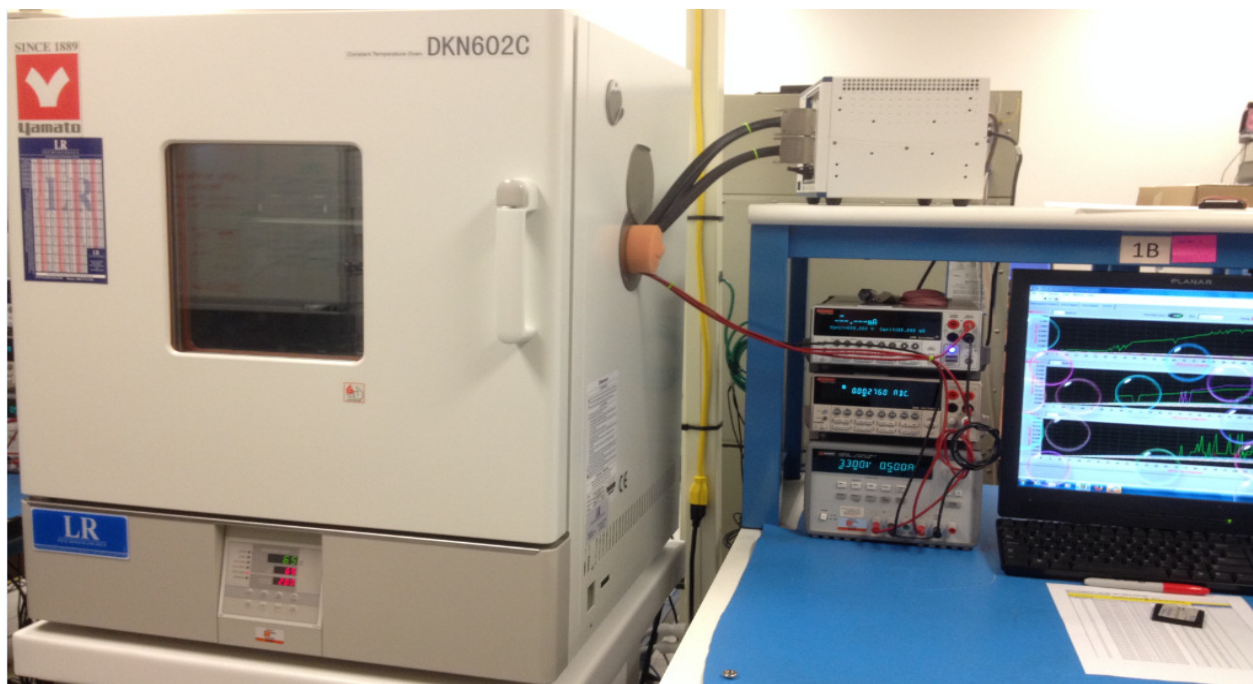


Figure 1 MEMS Cycling and Hold down Reliability Stress Test Set-Up Block Diagram



Picture 8 MEMS Cycling and Hold down Reliability Stress Test Set-Up

7.5.2 Figure 2 shows the front panel of the test program (for the WS1050 version 1.5)

7.5.3 Contact WiSpry Engineering for the latest version of the test program.

7.5.4 Test programs are located in directory: S:\Software_Control\Released\36 DUT Board

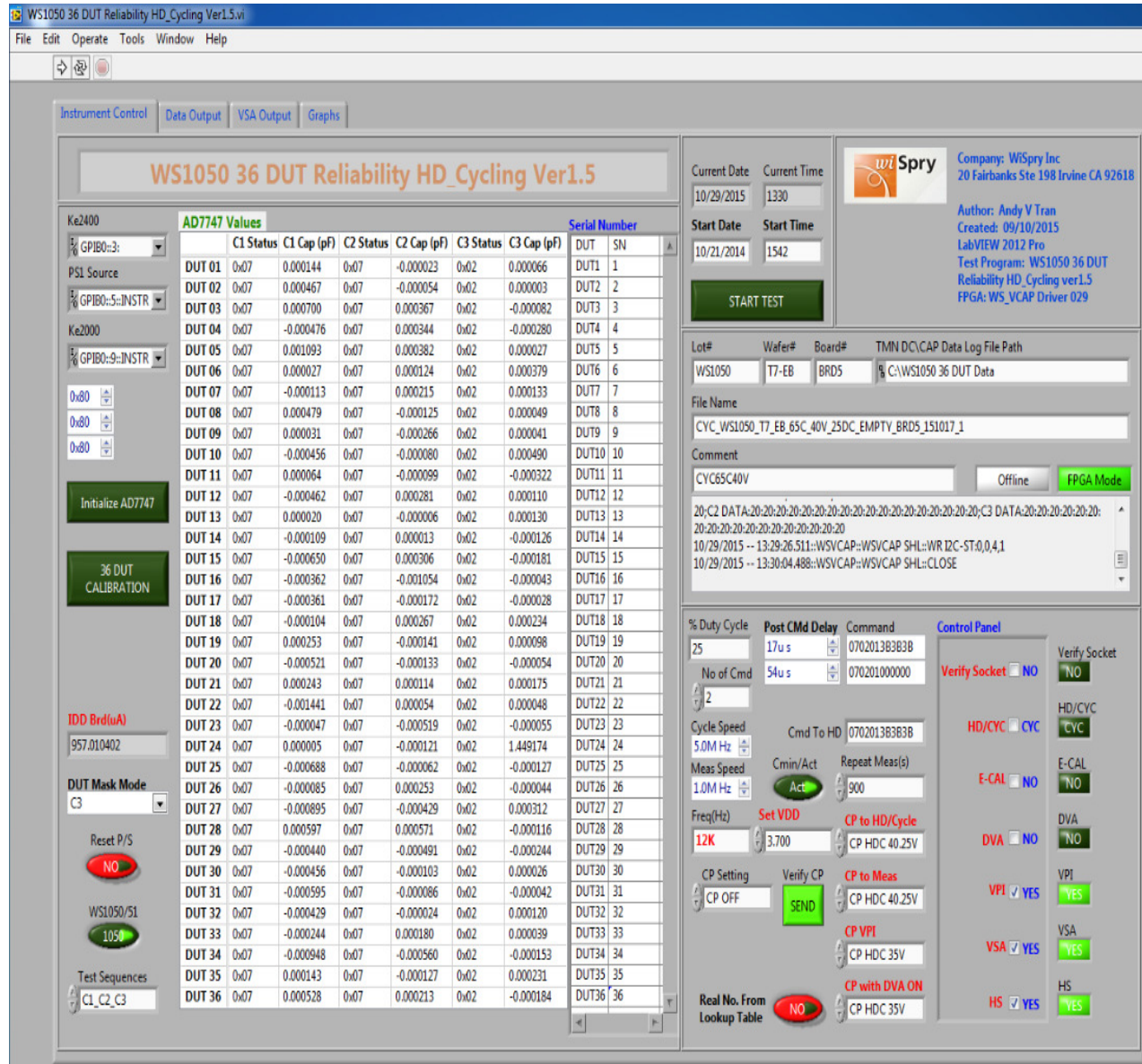


Figure 2 Front Panel of the WS1050 36 DUT Stress Test Program

- For calibration (Figure 4): All sockets should be empty and the capacitance values of 36 DUT should be around zeros “~0” for all three banks. If not, click on “36 DUT CALIBRATION” button to zero out the sockets

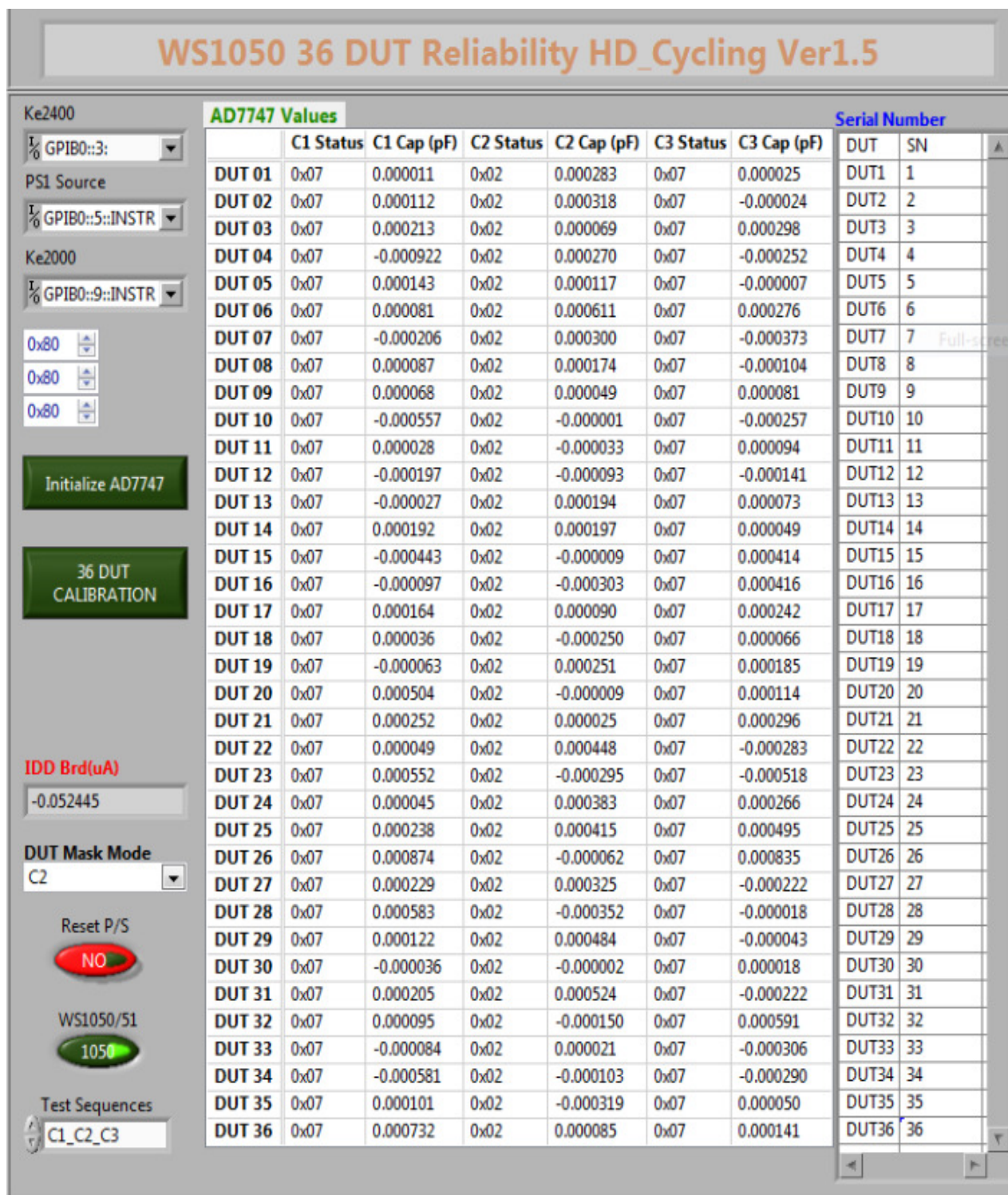


Figure 4 Empty Socket Calibration Summary Window

Initialize AD7747

Note: If sockets are not zeros “~0”, click on “Initialize AD7747” button to initialize the ADI chip, make sure the capacitance values will be less than 1pF (<1pF) for all three banks of 36 DUT, click on “36 DUT CALIBRATION” button to zero out the sockets.

- Set-up test condition (Fig. 5): The front panel below was set by default with cycling, DVA OFF, E-CAL OFF, VPI ON, VSA ON, HS (hand shake check) = ON, VDD = 3.7V, cycle speed = 12 KHz, CP stress = 40.25V, CP VPI = 35V.

Figure 5 Test Condition Set-Up Front Panel for default cycling conditions (DVA = OFF, ECAL = OFF, VPI = ON, HS (Handshake) = ON, Duty Cycle = 25%, VDD = 3.7V, Frequency = 12 KHz, Charge Pump = 40.25V, Charge Pump VPI = 35V

- Verify Socket: This run is required for the first set up with the new board to verify the board is stable before stressing devices, and the reading point will depend on “Repeat Meas(s)” set up.
 - HD/CYC: Check/Uncheck this box to run Hold down Stress/Cycling Stress
 - E-CAL: Check/Uncheck this box to run a stress with E-CAL ON/OFF
 - DVA: Check/Uncheck this box to run a stress with Dual Voltage Actuation ON/OFF
 - VPI: Check/Uncheck this box to run a Voltage Pull-In. This run is to monitor all the beam closed completely (by bank) based on the capacitance values for each read point
 - VSA: Check/Uncheck this box to run a stress with a Voltage Self Actuation Test (by bank)
 - HS: Check/Uncheck this box to run the handshake check to verify the contact.
- Set-up with standard stress (cycle): All Drivers ON, All Drivers OFF, 25% Duty. All numbers should be set as same as the boxes are shown below:

Figure 6 All Drivers ON and All Drivers OFF Set Up Box for 25% Duty Cycle. The numbers in the command box should be represented as shown

- | % Duty Cycle | Post Cmd Delay | Command |
|--------------|----------------|--------------|
| 33 | 18u s | 0702013B0000 |
| No of Cmd | 18u s | 070201003B00 |
| 3 | 18u s | 07020100003B |

- Set-up for stress (Hold Down): All Drivers should be closed during hold down, 100% duty, this was set by default

Cmd To HD 0702013B3B3B

- Figure 9 shows the front panel is set-up to collect the test data.

Lot#	Wafer#	Board#	TMN DC\CAP Data Log File Path
WS1050	T7-EB	BRD5	C:\WS1050_36 DUT Data

File Name

CYC_WS1050_T7_EB_65C_40V_25DC_EMPTY_BRD5_141017_1

Comment

CYC65C40V

Offline FPGA Mode

```

05/19/2014 -- 12:24:35.853::WSVCAP::APP::Application Started
05/19/2014 -- 12:24:37.606::WSVCAP::WSVCAP SHL::WR I2C-REG:0x0A;MASK:
0xFFFFFFFFFF;C1 DATA:22:22:22:22:22:22:22:22:22:22:22:22:22:22:C2 DATA:22:22:22:22:
22:22:22:22:22:22:22:22:22:22:22:22:22:22:C3 DATA:22:22:22:22:22:22:22:22:22:22:22:22
05/19/2014 -- 12:24:37.773::WSVCAP::WSVCAP SHL::WR I2C-ST:0,0,4,1
    
```

Note: The file name format will be:
stress lot# wafer# design temperature CPV Stress duty brd# yymmdd run

- The test can be set to start immediately by clicking on the START TEST button; alternatively the start date and time can be programmed as shown in Figure 10.

Figure 10 Cycling or Hold down Stress Initiation for immediate or delayed start

Note: The time shall be set at least 30 minutes to wait after loading parts to the board in the oven/chamber. This time is required for the stabilization of the board dwell time at the temperature before to run stress.

- The front panel (Figure 11) displays the capacitance values for every read point.

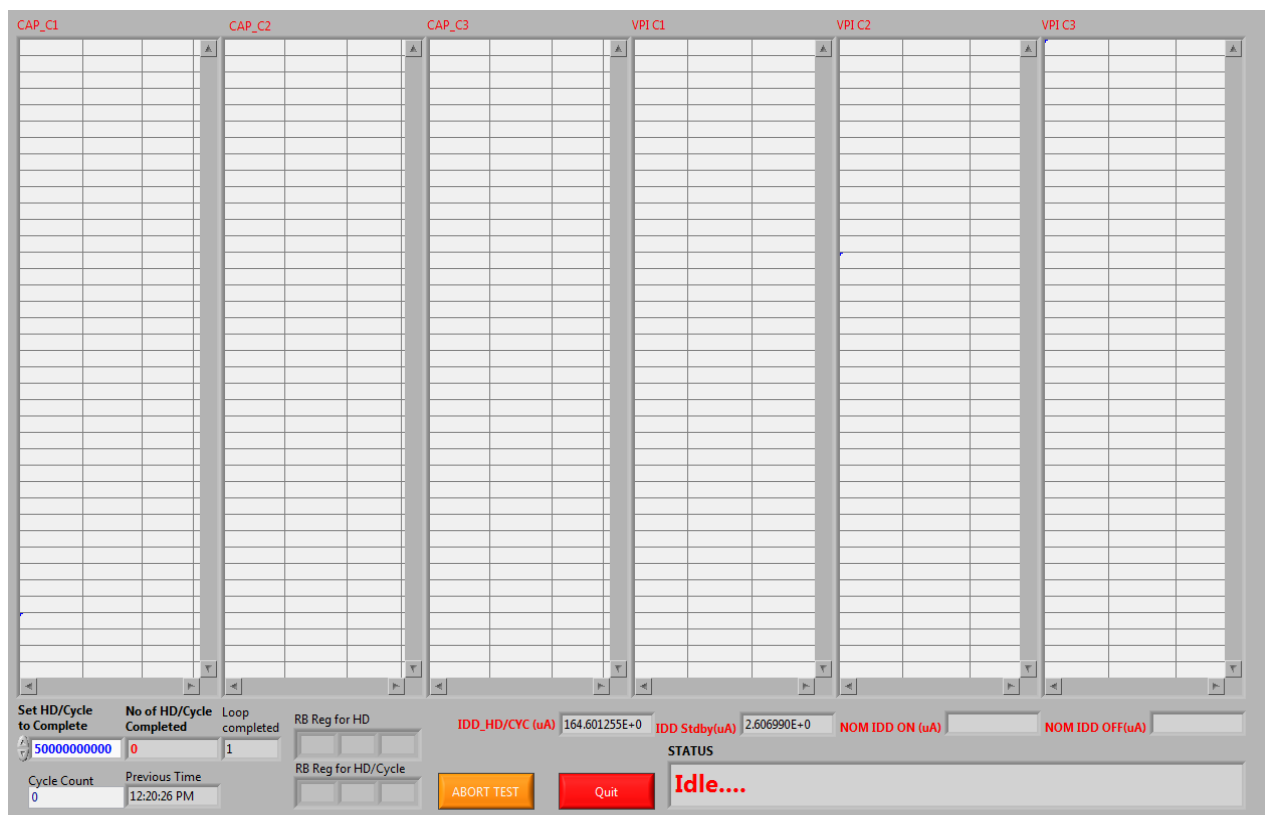


Figure 11 This Front Panel will display the capacitance values at every read point

- The front panel (Figure 12) displays VSA, HS check, EFUSE, % Delta CAP for every read point

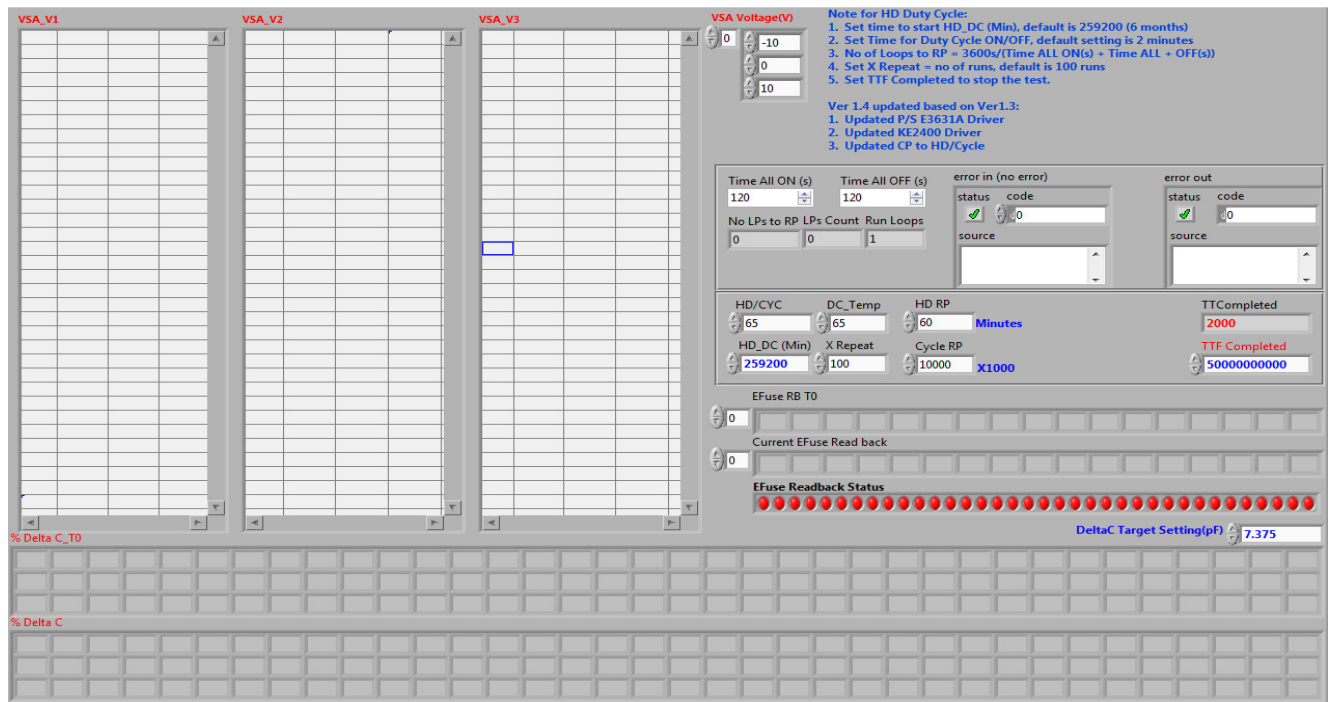


Figure 12 the Front Panel shown will display the VSA, HS check, EFUSE, %Delta CAP for every read point

- Figure 13 shows the output results, so that changes in CMIN can be monitored during stress.

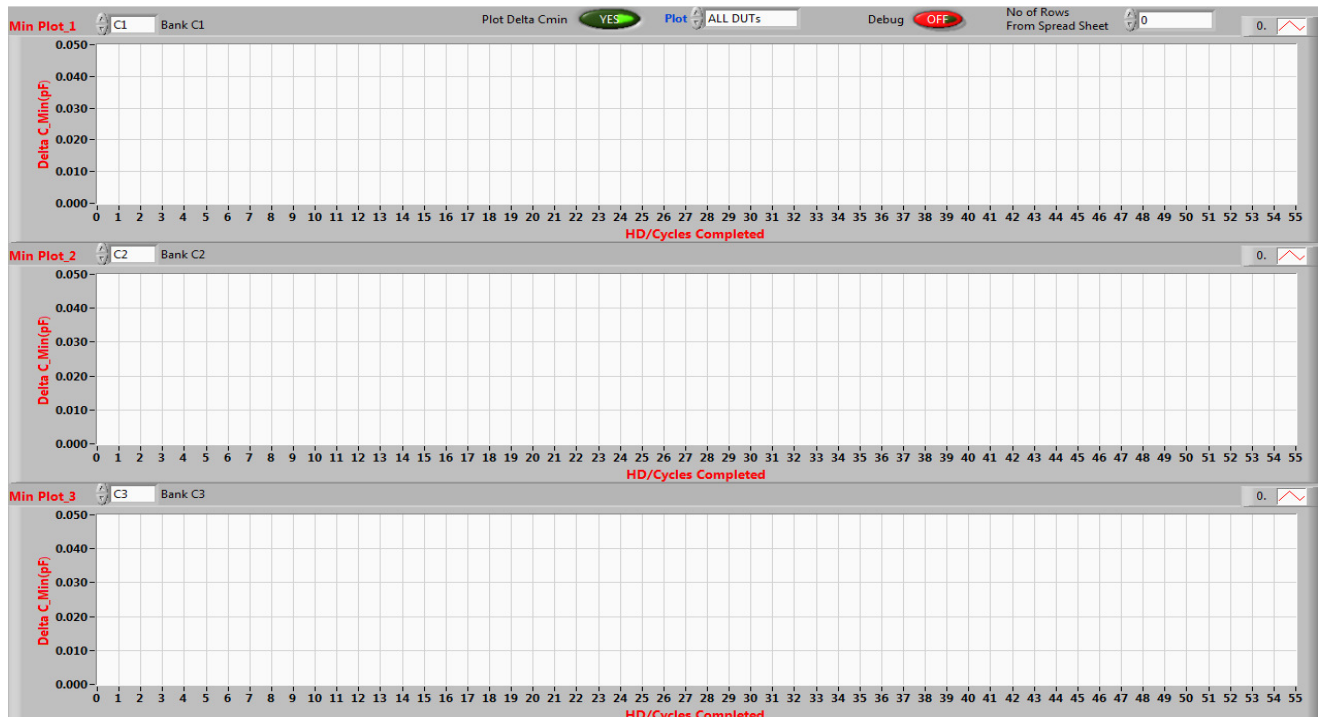


Figure 13 This shows the Output results for monitoring the instantaneous changes in CMin

- Stop stress or abort the test: The test can be aborted immediately by click on the ABORT TEST button (Figure 14) or enter the number that will be set to complete the test (5 billion cycles was set by default).

Figure 14 This Front Panel can be used to ABORT the stress or to set the minimum number of cycles to achieve. The button ABORT TEST will abort the stress

- This is a special test for Hold down during cycle test.
 - The standard Hold down depends on the number set up from the box “HD_DC (min)”, (259200 min = 6 months is set by default).
 - When the number from “Set HD/Cycle to Completed” = “HD_DC (min)” then the next run will be two minutes ON (turn All Drivers ON), two minutes OFF (turn All Drivers OFF)

Figure 15 This Front Panel can be used for Hold down during cycle test.

8. REVISION HISTORY

Rev	Description	Editor	Date
A	Initial Release	M. Johnson	12-Aug 2015
-	Review and Write the suggestion to modify and update	Shawn/Mark/Dana	27-Oct 2015
B	Modified and Updated	Andy V Tran	30-Oct 2015