

CONNECTOR 0 (RDI0)

CONNECTOR 3 (RDI0)

TERMINAL 68

TERMINAL 34

TERMINAL 1

TERMINAL 35

TERMINAL 68

TERMINAL 34

TERMINAL 1

TERMINAL 35

CONNECTOR 1 (RDI0)

CONNECTOR 2 (RDI0)

TERMINAL 68

TERMINAL 34

TERMINAL 1

TERMINAL 35

TERMINAL 68

TERMINAL 34

TERMINAL 1

TERMINAL 35

DIO39 68 34 DIO38

DIO37 67 33 DIO36

DIO35 66 32 DIO34

DIO33 65 31 DIO32

DIO31 64 30 DIO30

DIO29 63 29 DIO28

DIO27 62 28 +5V

DIO26 61 27 +5V

DIO25 60 26 DGND

DIO24 59 25 DGND

DIO23 58 24 DGND

DIO22 57 23 DGND

DIO21 56 22 DGND

DIO20 55 21 DGND

DIO19 54 20 DGND

DIO18 53 19 DGND

DIO17 52 18 DGND

DIO16 51 17 DGND

DIO15 50 16 DGND

DIO14 49 15 DGND

DIO13 48 14 DGND

DIO12 47 13 DGND

DIO11 46 12 DGND

DIO10 45 11 DGND

DIO9 44 10 DGND

DIO8 43 9 DGND

DIO7 42 8 DGND

DIO6 41 7 DGND

DIO5 40 6 DGND

DIO4 39 5 DGND


DIO3 38 4 DGND

DIO2 37 3 DGND

DIO1 36 2 DGND

DIO0 35 1 DGND

NI PXI-7813R



WS1050 Reliability Test Board (SWC/SHD), 36 DUT

NI PXI-7813R, there are 4 connectors, J1 to J4 with total is 160 Digital I/O

For Control DUT, RFFE

1. SCL: 1 Digital I/O

2. SDA: 1 Digital I/O

3. DAT0: 9 Digital I/O

Total Digital I/O used for RFFE is 11 Digital I/O

For Capacitance Measurement, I2C

1. SCL: 1 Digital I/O

2. SDA: 3 banks x 9 DUT = 27 Digital I/O

Total Digital I/O used for I2C is 28 Digital I/O

9 DUT required 11 + 28 = 39 Digital I/O

1 Channels will be available

NI 781xR Connector Pin Assignments and Locations

RFFE-SCL\_S1-9

RFFE-SDA\_S1-9

DAT0-S1

S1

DUT 1

DAT0-S2

DAT0-S9

S2

DUT 2

S9

DUT 9

I2C-SCL

I2C-SDA-C1-S1

I2C-SDA-C2-S1

I2C-SDA-C3-S1

I2C-SDA-C1-S2

I2C-SDA-C2-S2

I2C-SDA-C3-S2

I2C-SDA-C1-S9

I2C-SDA-C2-S9

I2C-SDA-C3-S9

J1: DUT 1 to 9

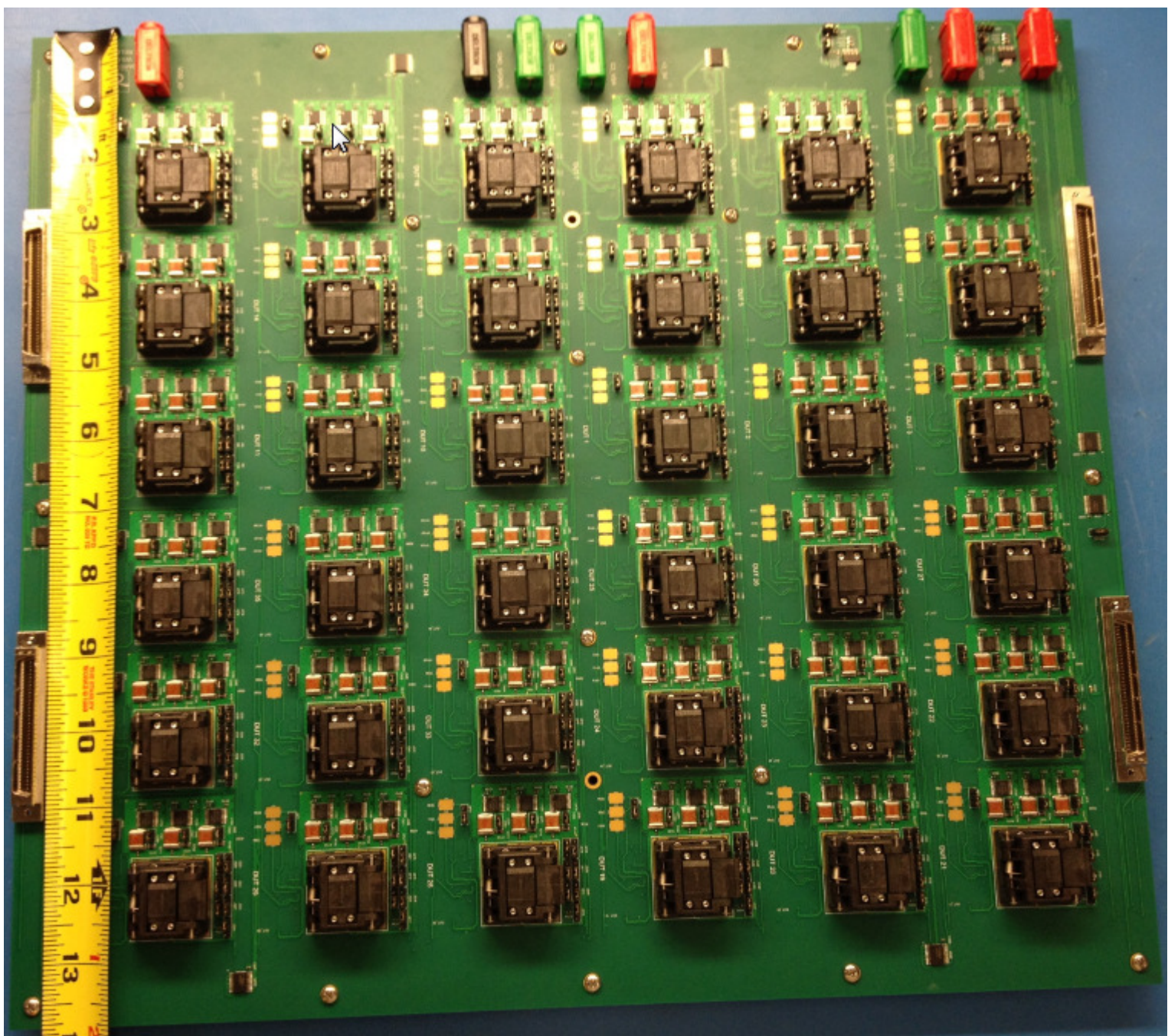
J2: DUT 10 to 18

J3: DUT 19 to 27

J4: DUT 28 to 36



36 DUT Board Layout:



Test Setup Block Diagram:

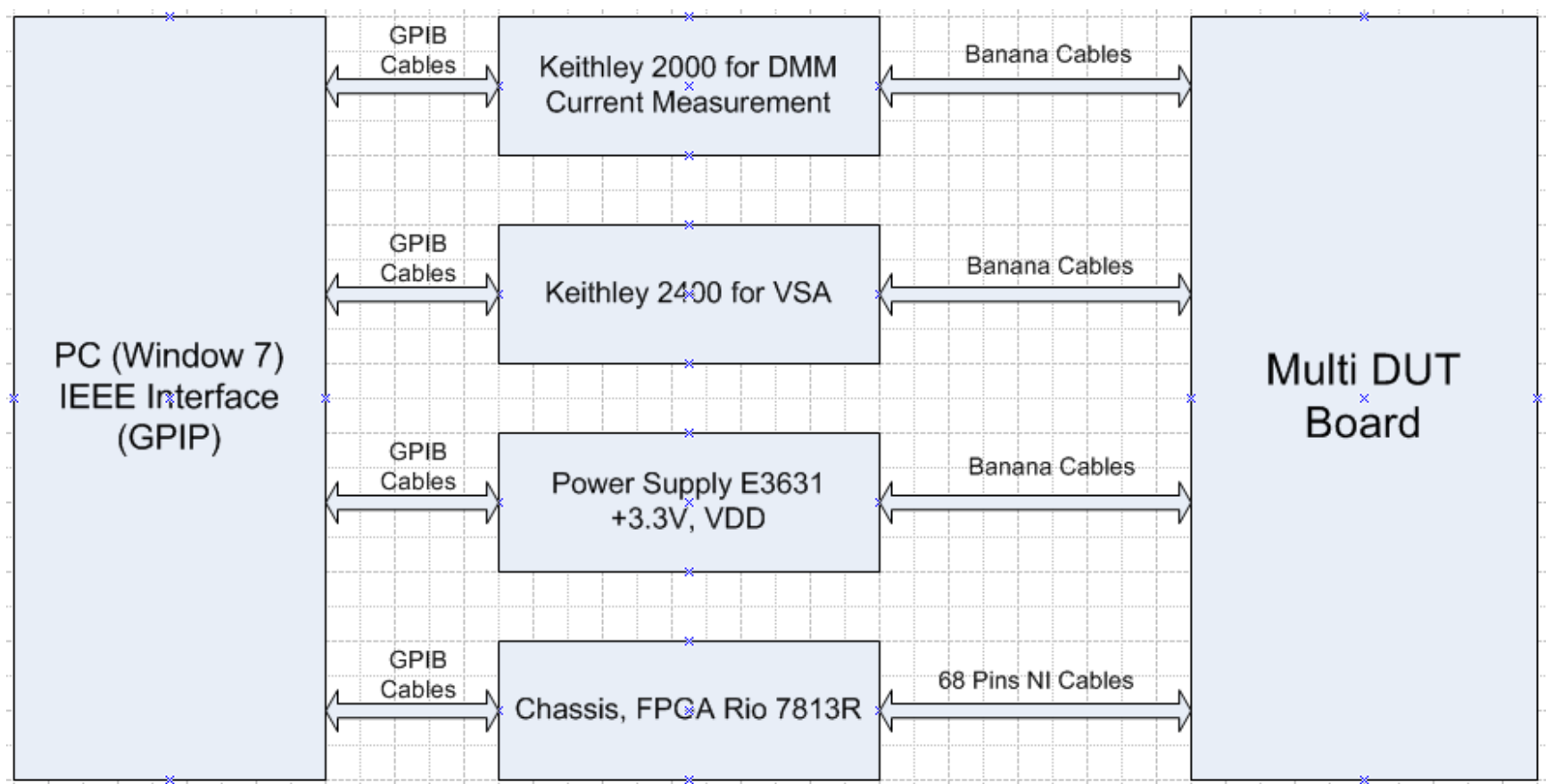


Fig 1. Test Setup Block Diagram

Hardware:

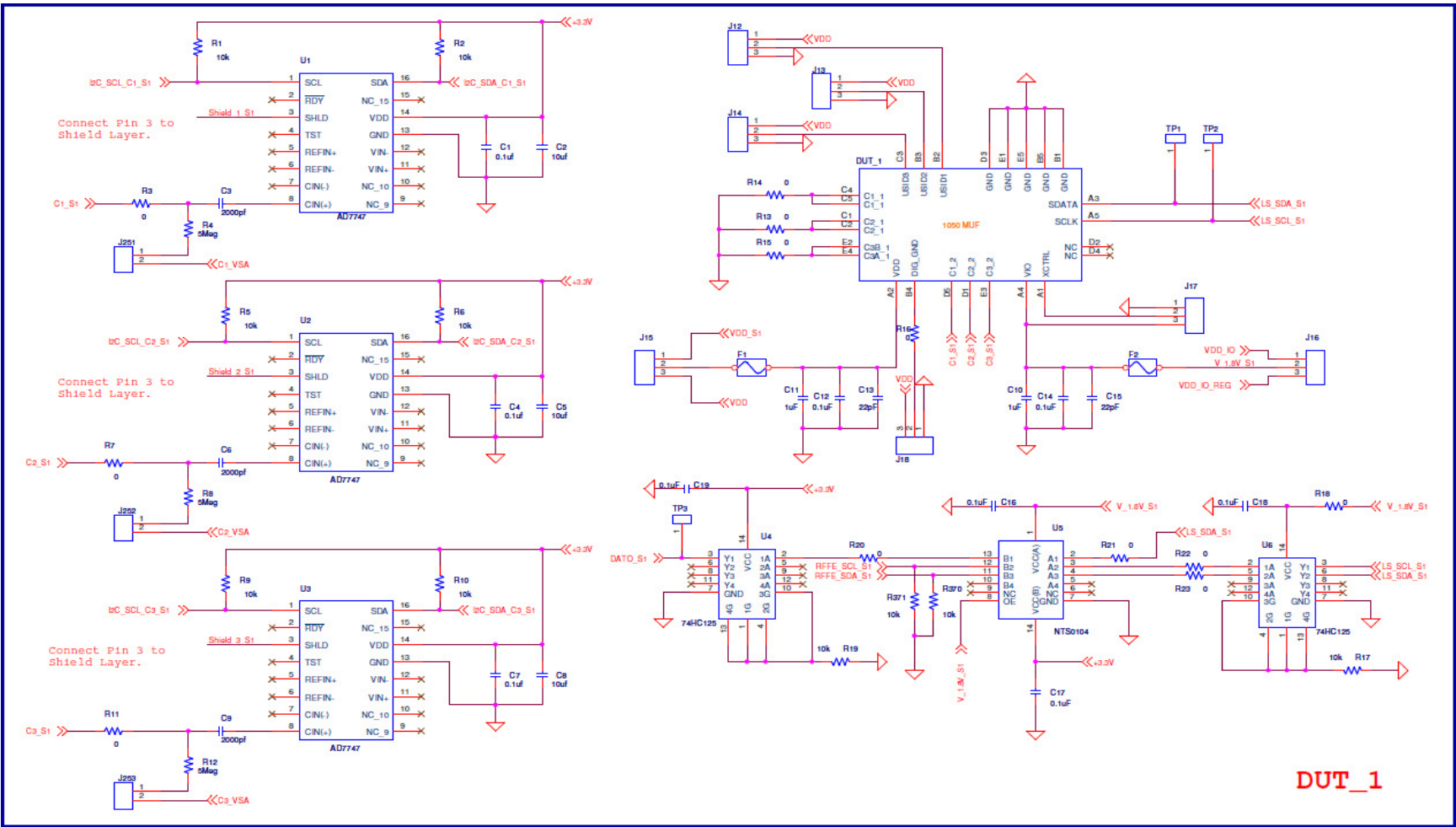
- 1. Keithley 2000 (DMM)
- 2. Keithley 2400 (Source meter for VSA test)
- 3. Agilent Power supply E3631 (Power source for +3.3V, VDD)
- 4. Chassis PXI 1033
- 5. FPGA card Rio 7813R, 160 digital I/O channels
- 6. SHC68-68-RDIO Cables (4)
- 7. Several banana plugs

Software:

- 1. FPGA Revision :
  - a. WS\_VCAP Driver 029 (36 DUT)
  - b. WS\_VCAP Driver 024 (16 DUT)
- 2. Stress Test Program
  - a. WS1050 36 DUT Reliability HD\_Cycling Ver1.3 (36 DUT)
  - b. WS1050 16 DUT Reliability HD\_Cycling Ver1.8 (16 DUT)

Schematic:

- 1. Schematic WS1050 36 DUT Reliability REV E.
- 2. Schematic WS1050 16 DUT Reliability REV G.



Test Sequences:

- 1. Turn ON +3.3V, this will turn on AD7747 and voltage regulator LM317 to generate 1.8V for VIO
- 2. Turn ON VDD (HD = 3.3V; Cycle = 3.7V)
- 3. Set CP OFF
- 4. Measure IDD standby
- 5. Set CP Voltage to stress
- 6. Set DVA (ON/OFF)
- 7. Set ECAL (ON/OFF)
- 8. Set VPI (ON/OFF) Note: If VPI OFF, skip steps 31 to 41.
- 9. Set VSA (ON/OFF) Note: If VSA OFF, skip steps 42 to 54.
- 10. Set HS (ON/OFF) Note: If HS check OFF, skip step 55.
- 11. Start HD/Cycle (Non linear RP).
- 12. Turn All Drivers ON
- 13. Measure IDD All Drivers ON
- 14. Turn All Drivers OFF
- 15. Measure IDD All Drivers OFF
- 16. Measure C1\_Min
- 17. Measure C1\_F1
- 18. Measure C1\_F2
- 19. Measure C1\_S1 to C1\_S14F12



- 20.Measure C1\_Min2
- 21.Measure C2\_Min
- 22.Measure C2\_F1
- 23.Measure C2\_F2
- 24.Measure C2\_S1 to C2\_S14F12
- 25.Measure C2\_Min2
- 26.Measure C3\_Min
- 27.Measure C3\_F1
- 28.Measure C3\_F2
- 29.Measure C3\_S1 to C3\_S14F12
- 30.Measure C3\_Min2
- 31.Set DVA OFF, ECAL OFF (this is for VPI)
- 32.Set CP Voltage for VPI
- 33.Measure C1\_Min
- 34.Measure C1\_Max
- 35.Measure C1\_Min2
- 36.Measure C2\_Min
- 37.Measure C2\_Max
- 38.Measure C2\_Min2
- 39.Measure C3\_Min
- 40.Measure C3\_Max
- 41.Measure C3\_Min2
- 42.Set Ke2400 to V1 = -10V
- 43.Measure VSA C1\_V1
- 44.Measure VSA C2\_V1
- 45.Measure VSA C3\_V1
- 46.Set Ke2400 to V2 = 0V
- 47.Measure VSA C1\_V2
- 48.Measure VSA C2\_V2
- 49.Measure VSA C3\_V2
- 50.Set Ke2400 to V3 = 10V
- 51.Measure VSA C1\_V3
- 52.Measure VSA C2\_V3
- 53.Measure VSA C3\_V3
- 54.Set Ke2400 to 0V.
- 55.Run HS check on Register 1 (bank C1)
- 56.Save Data
- 57.Loop back to step 11

Note:

Test Sequence: Test program can measure read point by bank order, C1-C2-C3; C2-C1-C3 or C3-C2-C1

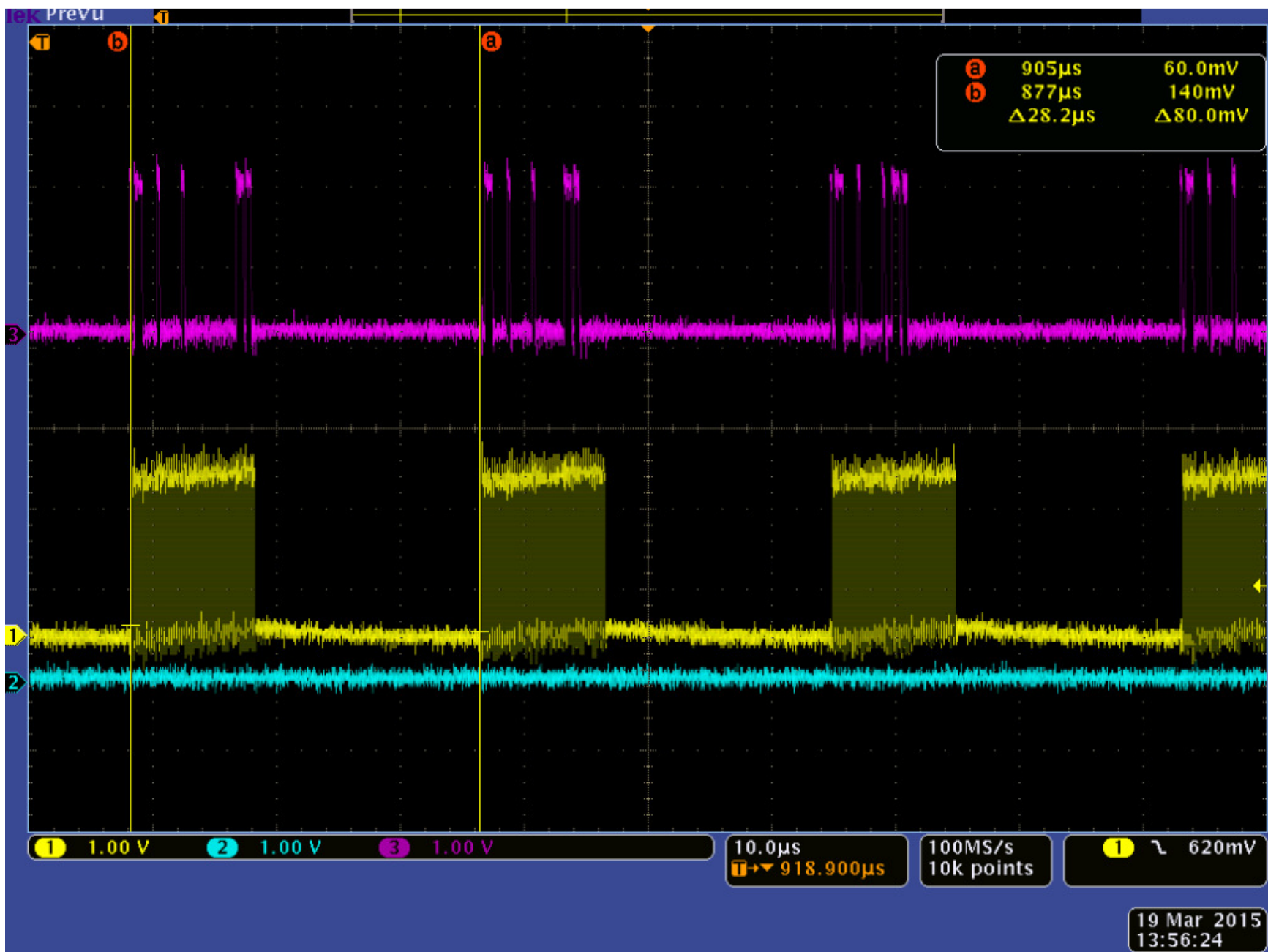
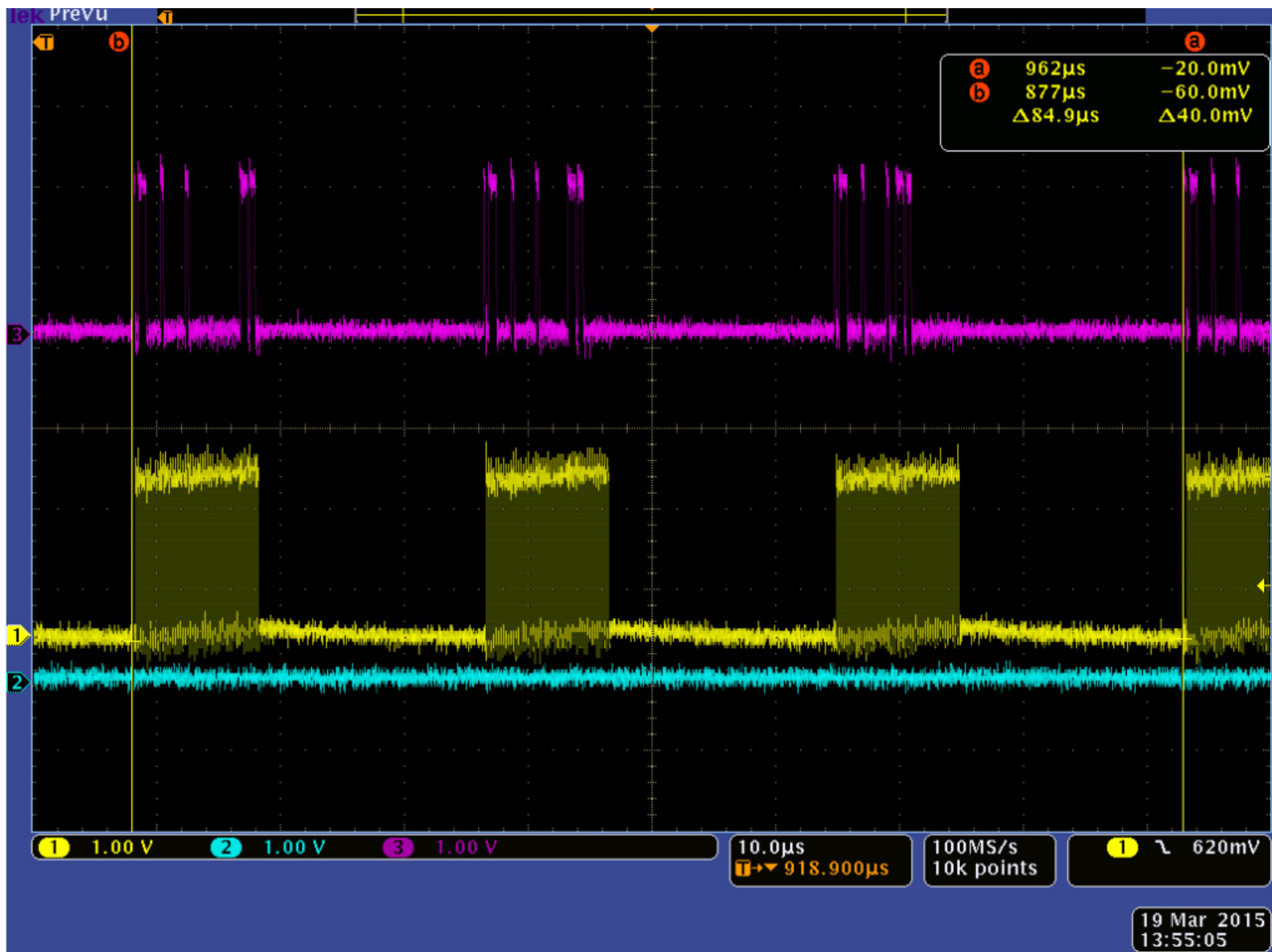
Stress Sequence: Test program can stress parts by bank order by setting commands:

070201|XX|XX|XX  
070201|XX|XX|XX  
070201|XX|XX|XX

XX can be 3B all drivers ON  
XX can be 00 all drivers OFF

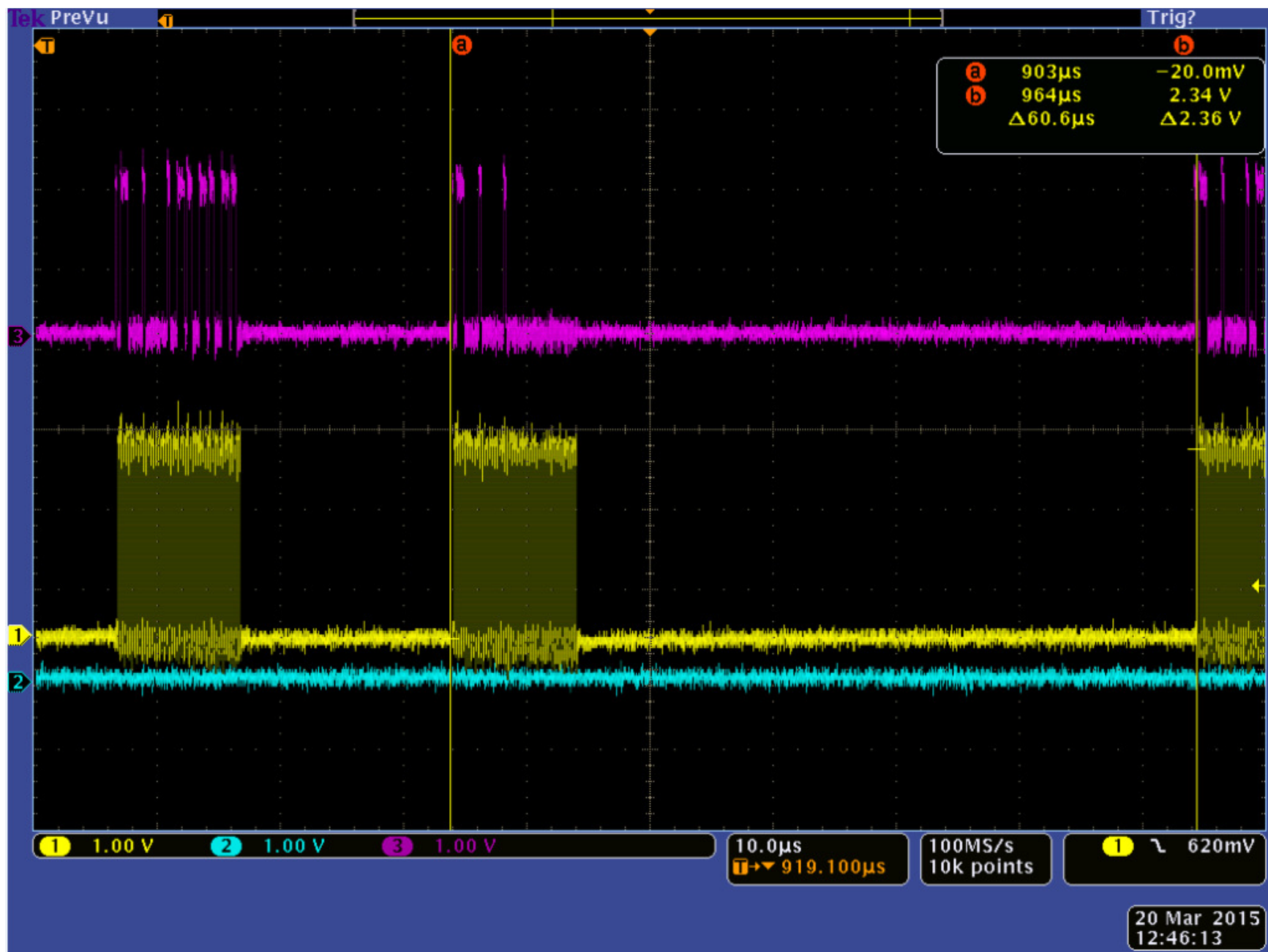
Cycling speed is12KHz with signal CLK is 5MHz.

With 33% Duty Cycle:





With 25% Duty Cycle



1. Main GUI for calibration and set up test:

[illegible]

2. GUI to monitor the test setup (CP voltage, DVA ON/OFF, ECAL ON/OFF) before stress, monitor cap values for each drivers, and time completed stress

Instrument Control | Data Output | VSA Output | Graphs

40V\_1 40V\_2 40V\_3 VPI C1 VPI C2 VPI C3

Set HD/Cycle to Complete: 50000000000  
No of HD/Cycle Completed: 0  
Loop completed: 1

Cycle Count: 0  
Previous Time: 12:20:26 PM

RB Reg for HD  
RB Reg for HD/Cycle

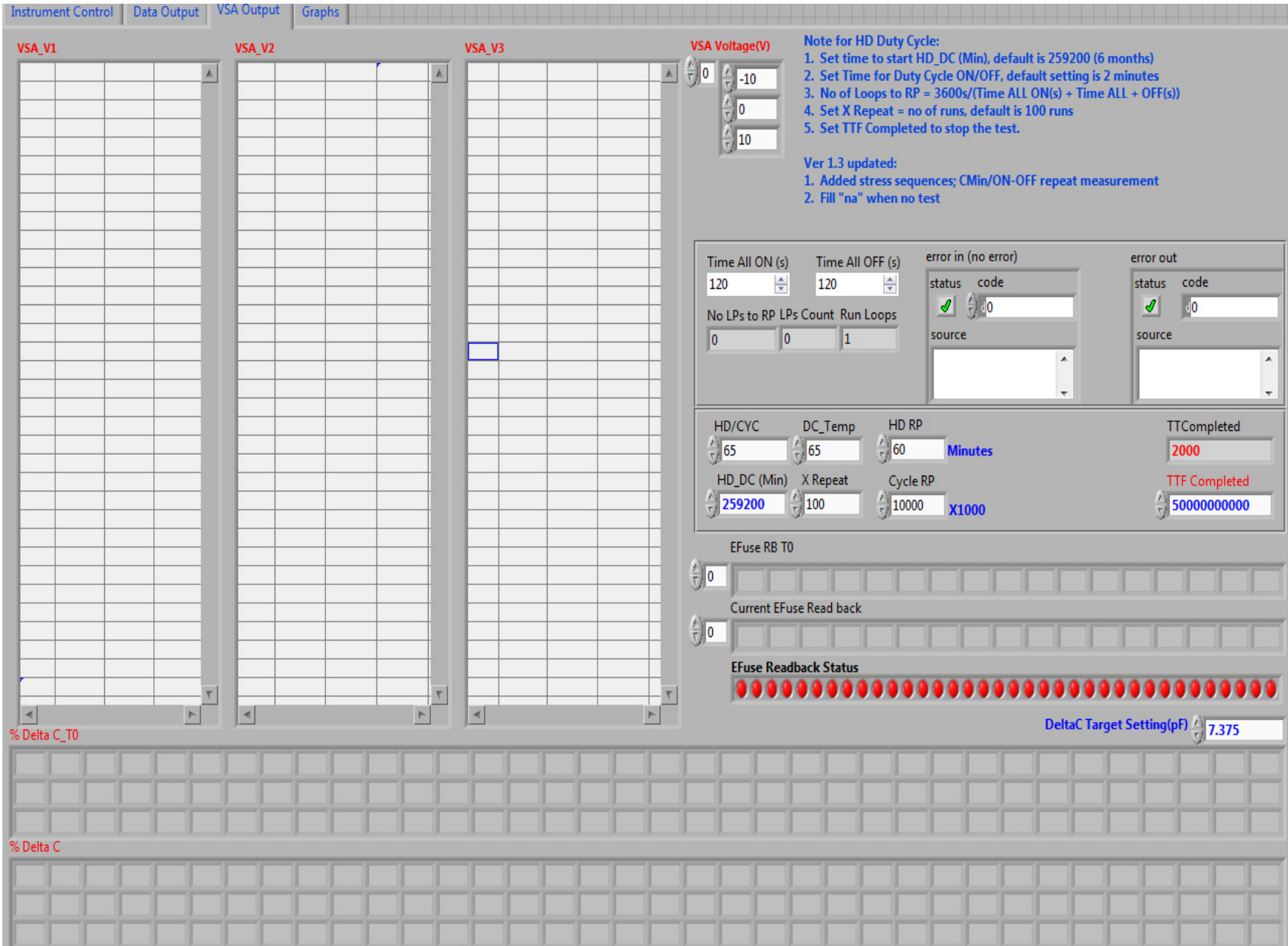
IDD\_HD/CYC (uA): 164.601255E+0  
IDD Stdby(uA): 2.606990E+0  
NOM IDD ON (uA):  
NOM IDD OFF(uA):

STATUS  
Idle....

ABORT TEST Quit



3. GUI to monitor VSA test, HS check, EFUSE read back and % Delta C change



4. GUI to monitor CMIN changes during the stress

