WS1050 Package parts 36 DUT Reliability

Test Procedures

Introduction:

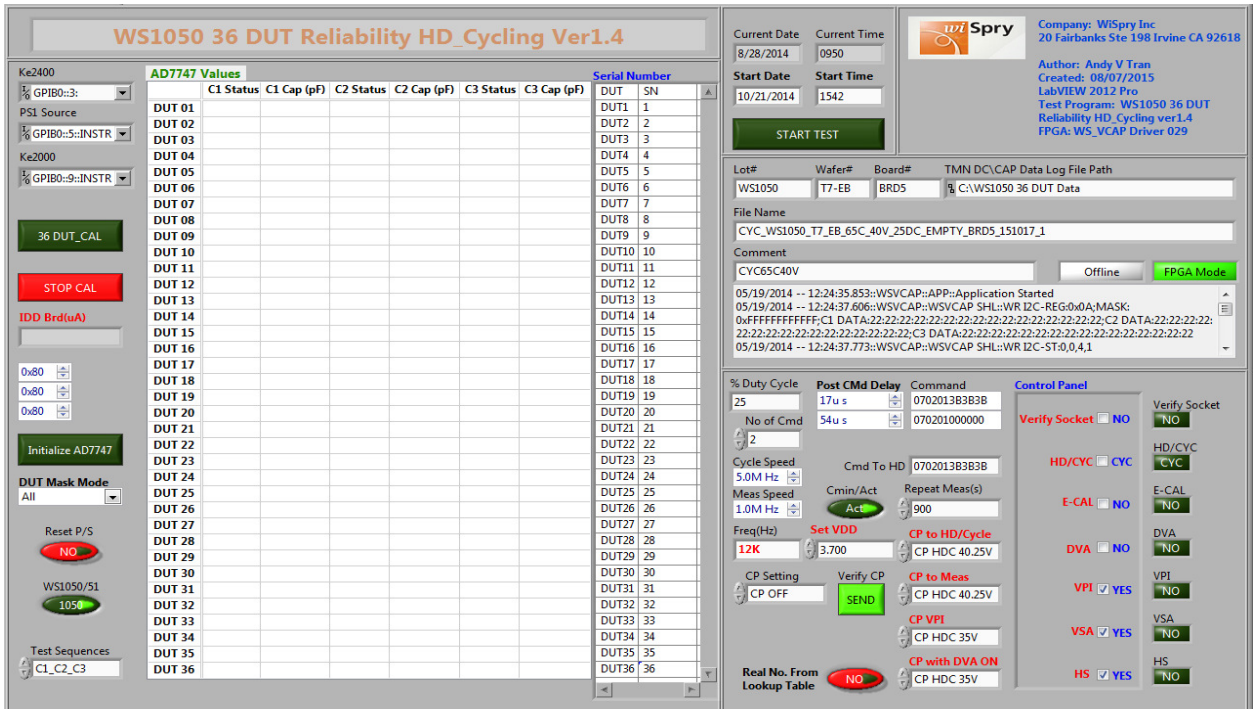
The purpose of this test procedure is for set up to run Hold Down and Cycle on package parts, toggle 7, WS1050 from 36 DUT board, and this test procedure will be used for internal only.

Hardware and Software requirement:

a. Hardware:
   1. Agilent 3631A, This PS will be used for VDD, +3.3V
   2. Ke2000 as a DMM for current measurement
   3. Ke2400 for VSA test (positive and negative voltages)
   4. PXI 1033 chassis
   5. NI PXI-7813R, FPGA Card for RFFE and I2C
   6. 4 NI Cables, SHC68-68-RDIO Cable
   7. 36 DUT Board
   8. Several banana cables

b. Software:

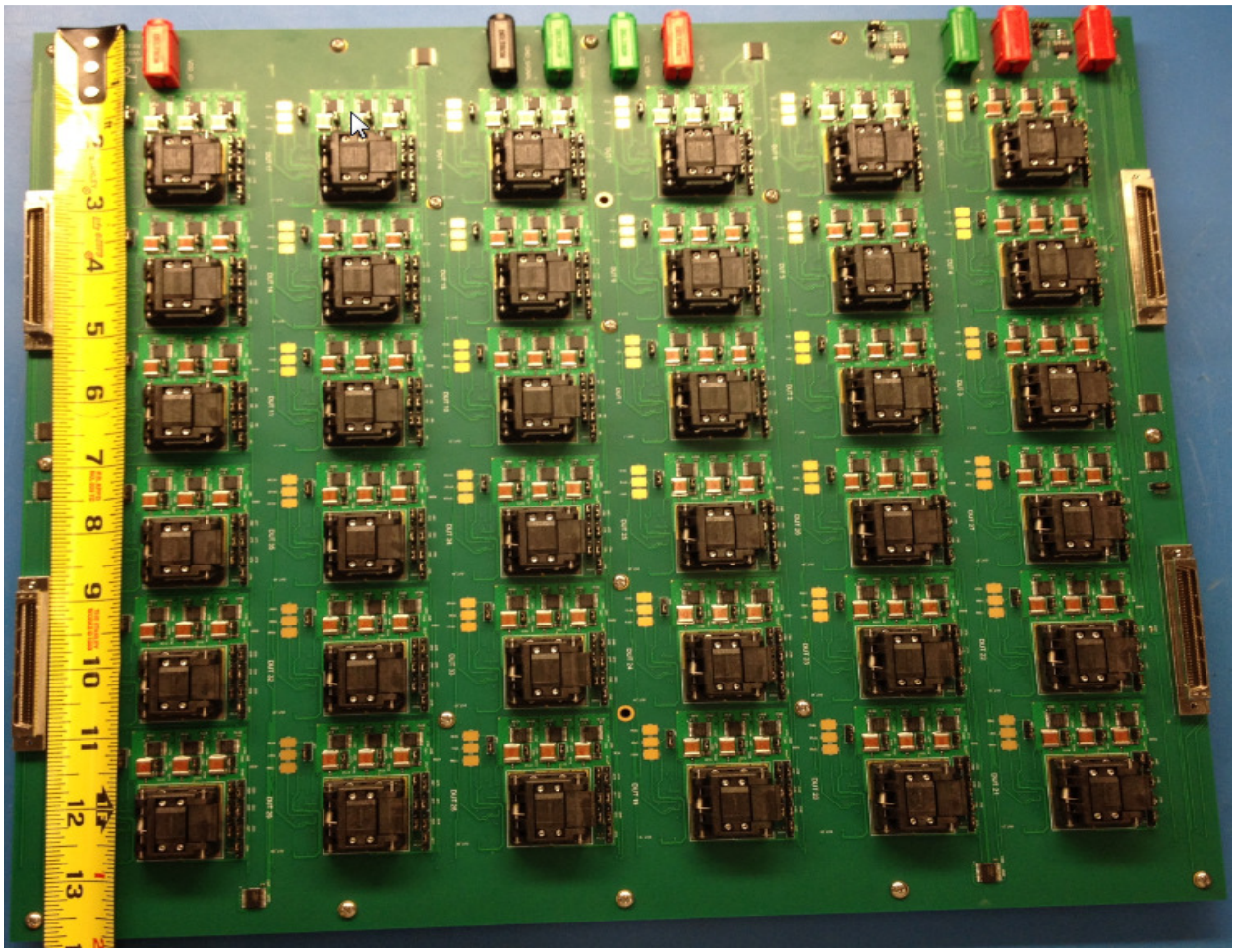
Test program: Executable for WS1050 36 DUT Reliability HD_Cycling Ver1.4



This test program will be found at the link below:

[S:\Software_Control\Released\36 DUT Board\WS1050 36 DUT Reliability HD_Cycling Ver1.4]

36 DUT Board:



Test Set up Block Diagram:

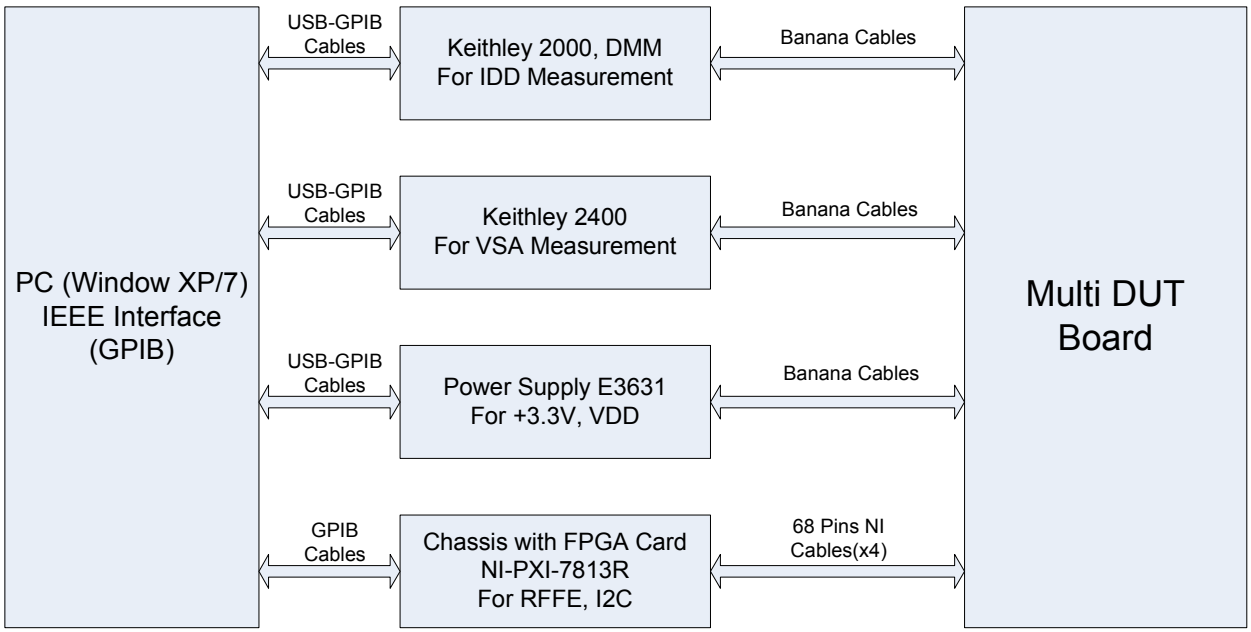
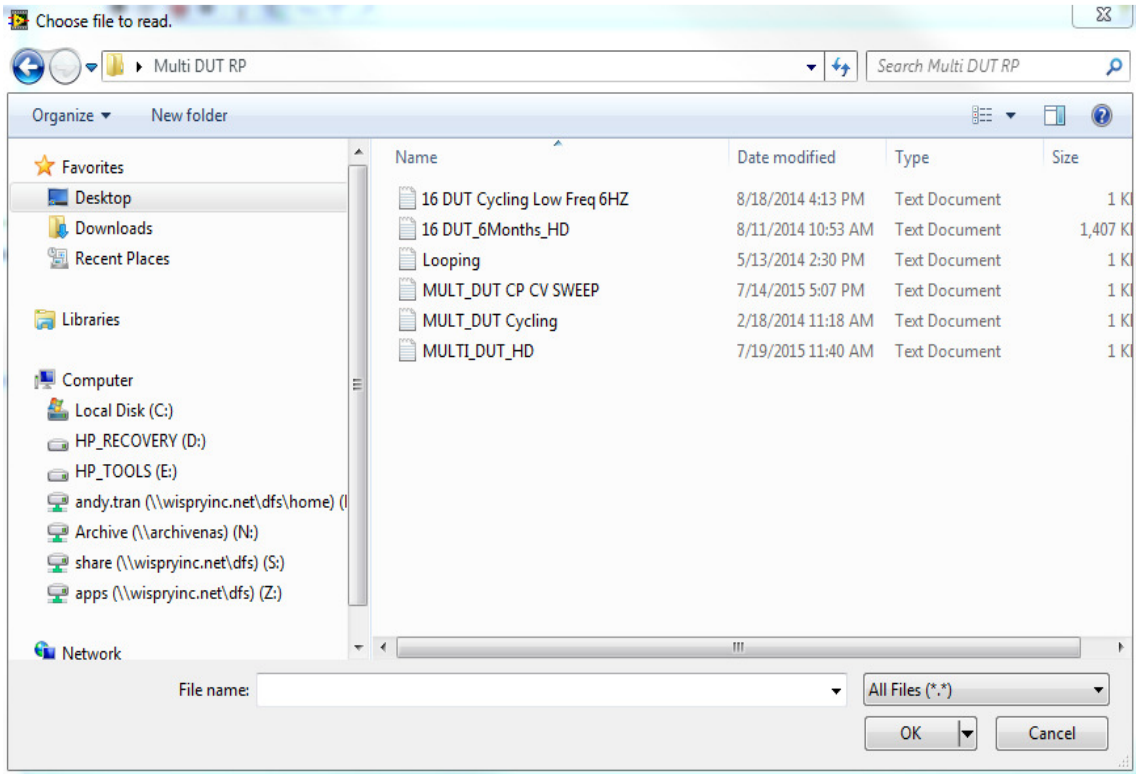


Fig 1. Test Setup Block Diagram

Set up and run Test Program:

1. Set temperatures from the oven/chamber:
   Adjust temperatures from the oven/chamber to meet the requirement (25C, 45C, 55C, 65C or 85C)
2. From the labVIEW test program click  this button to run the test program, it will pop up a dialog box to ask for a look up table for read point.

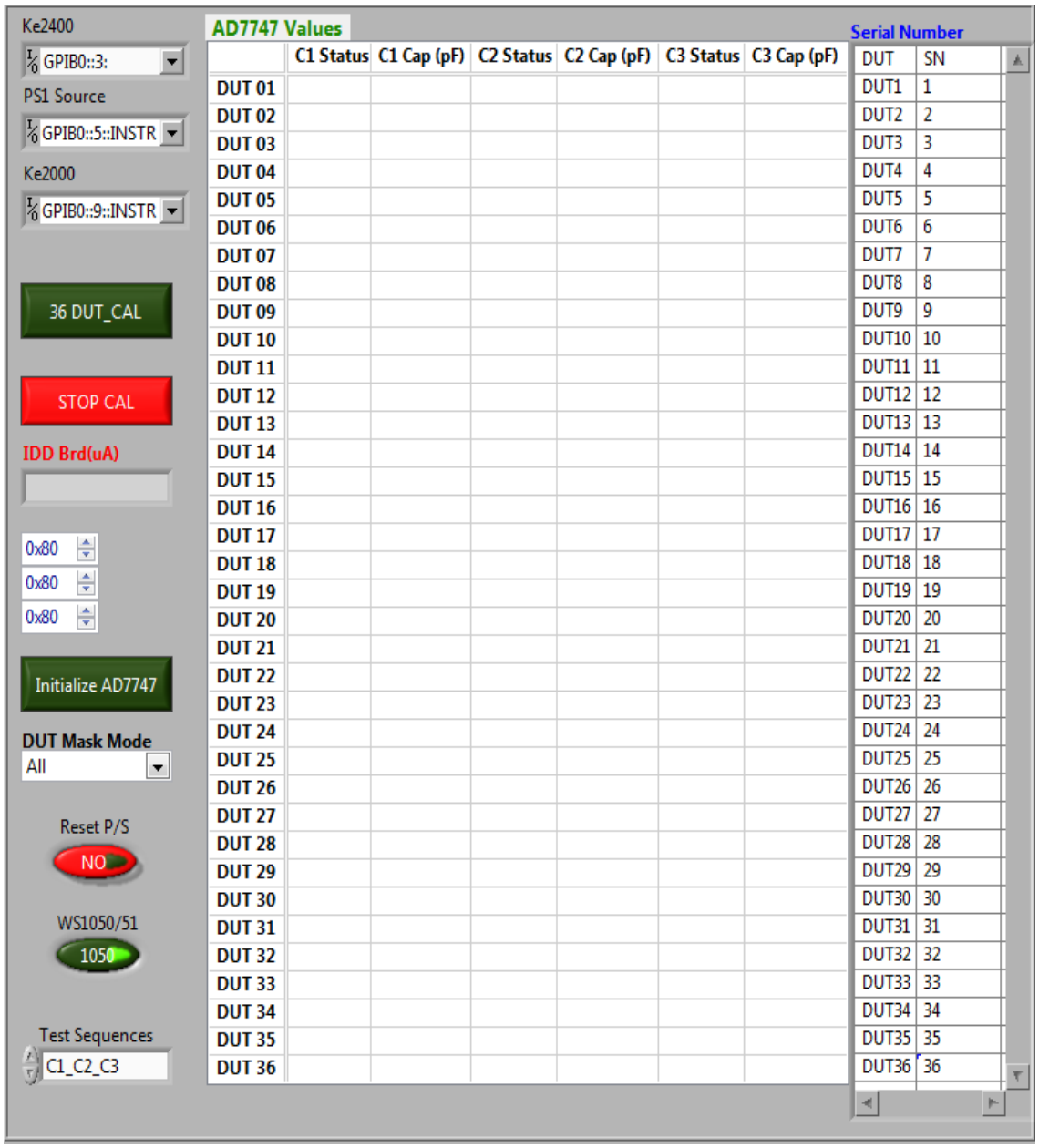


Note: it will depend on what stress you are running to pick the correct file.
For instance:
If you are running cycling, the file will be selected is MULT_DUT Cycling
If you are running Hold Down, the file will be selected is MULT_DUT HD

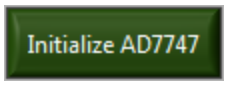
3. For Calibration Multi DUT, make sure all sockets are empty and the CAP values of 36 DUT will be ~0 for all three banks. If not, click on 36 DUT_CAL button

to zero out the sockets, then click STOP CAL button

to stop the calibration.



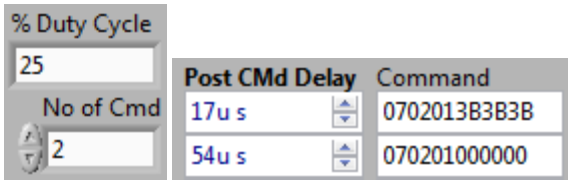
Note: If sockets are not zeros “~0”, click on Initialize AD7747 button



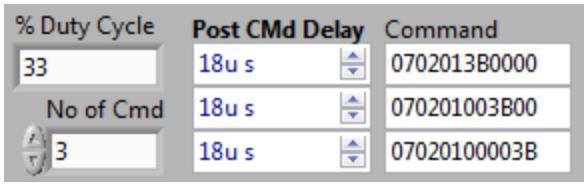
to initial ADI chip, the CAP values will be ~0.45pF for all three banks of 36 DUT. Click on 36 DUT_CAL button to zero out the sockets and click on Stop Cal to stop the calibration.

4. Setup test conditions. This step is a very important step to set up for stressing parts. Therefore, confirm with the people (Dana/Shawn/Mark) whoever requested for this setup.

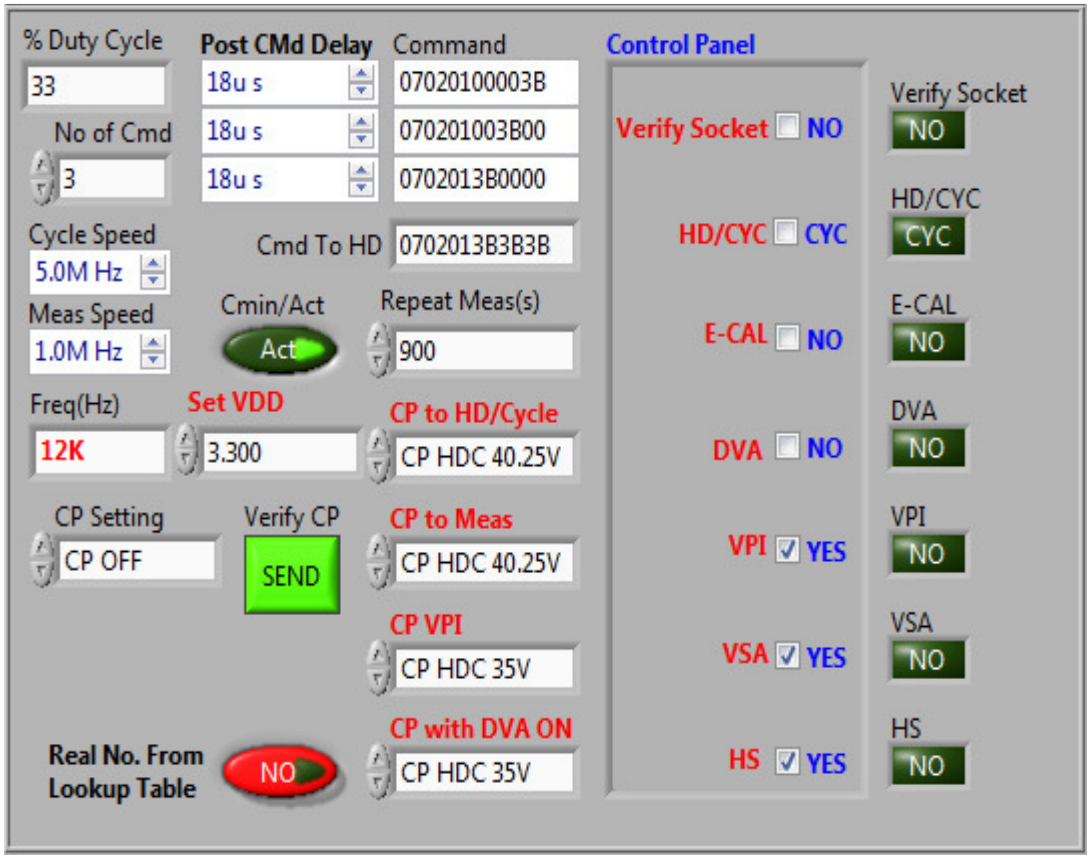
   a. Setup with standard stress (cycle): All drivers ON, All Drivers OFF, 25% Duty Make sure the numbers will be set as same as the boxes below (this number will be set by default when open the test program)



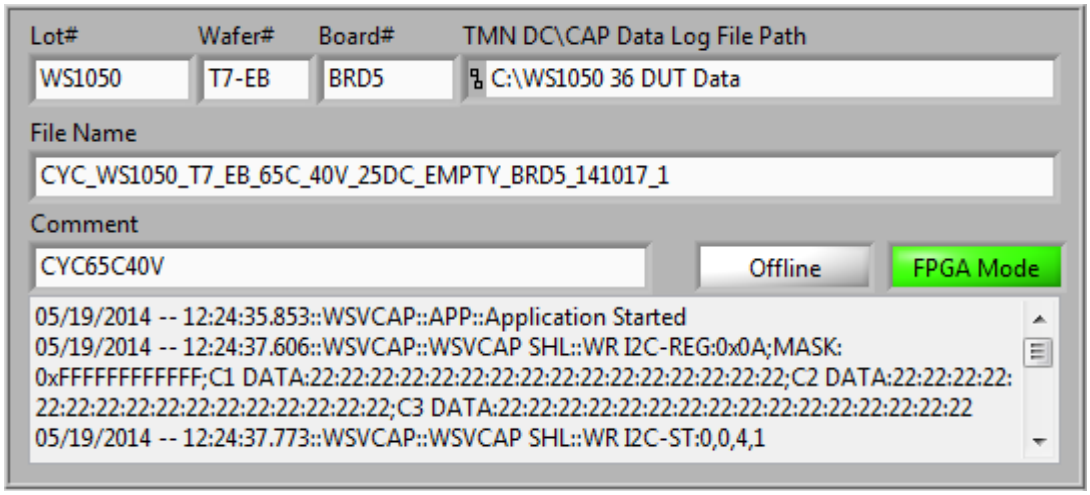
b. Setup with special stress (cycle): C1 ON, C1 OFF C2 ON, C2 OFF C3 ON, C3 OFF C1 ON. 33% Duty. Make sure all the numbers will be set as same as the boxes below



c. The front panel below is for more test setup conditions: HD/CYC, E-CAL ON/OFF; DVA ON/OFF; VPI ON/OFF; VSA ON/OFF; HS ON/OFF. Note: CYC, VPI, VSA and HS were setup "ON" by default

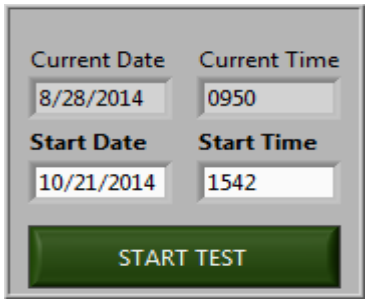


5. The front panel below is setup for data output

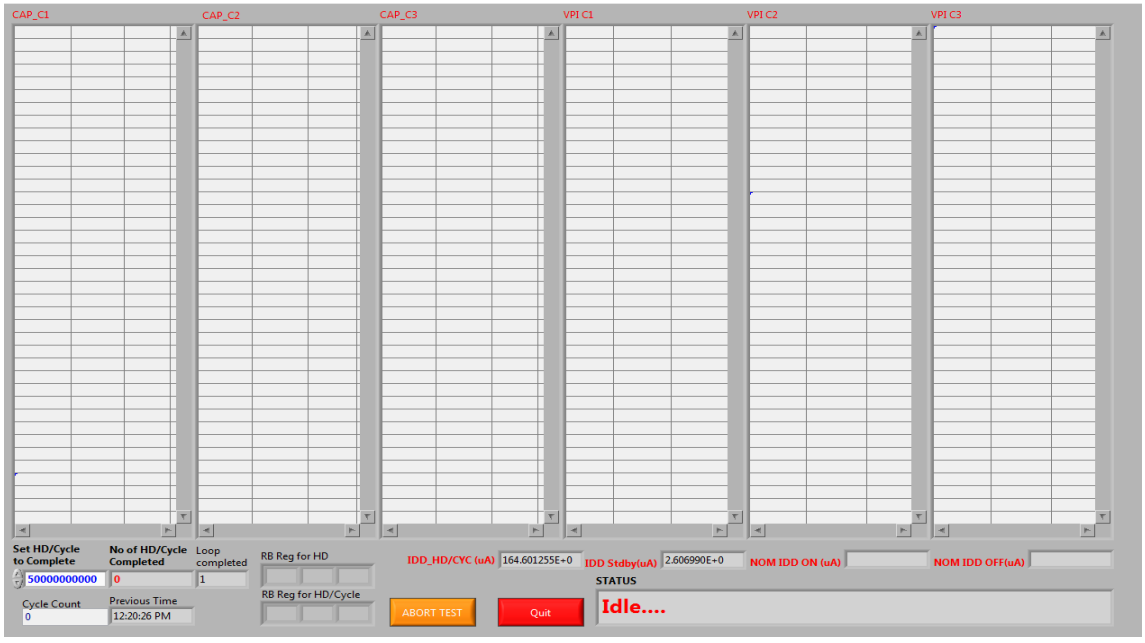


Note: The file name will be
Stress_Lot#_Wafer#_Design_Temperature_CPV_Duty cycle_Brd#_yymmdd_run

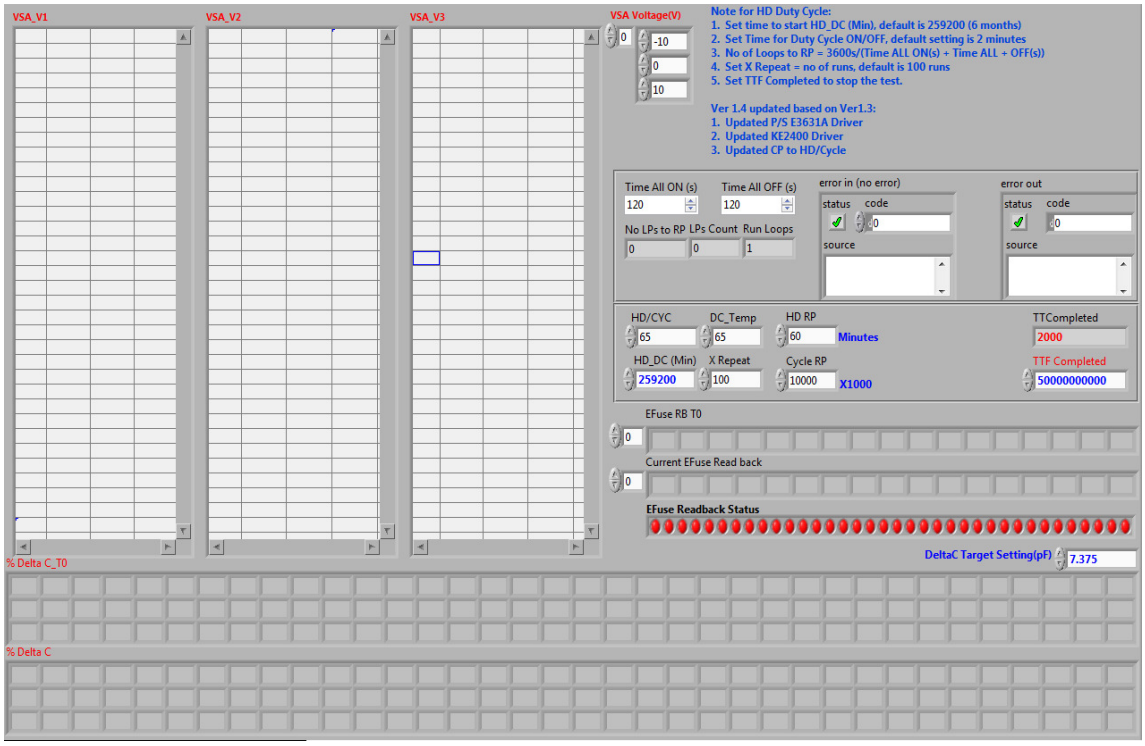
6. The session below is to setup for day and time to run stress: We can start to run the test immediately by click on the START TEST button or we can setup date and time to run the test by enter the Start Date and Start Time



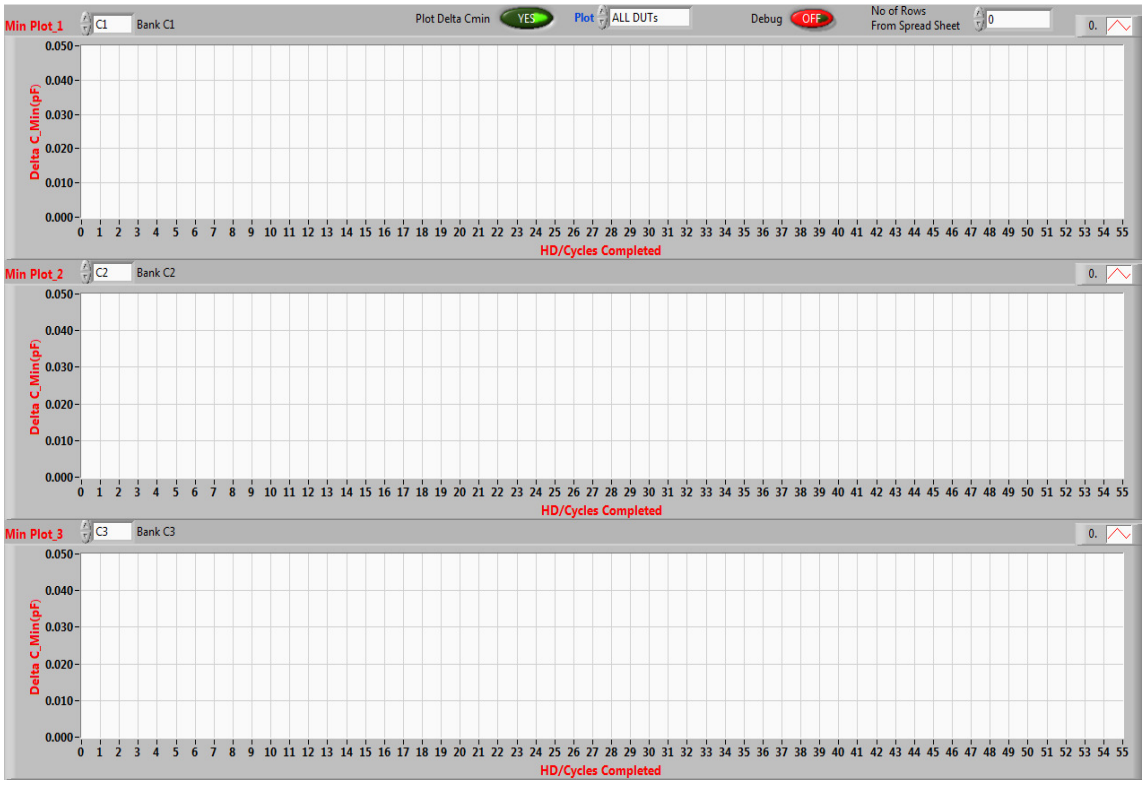
7. The front panel below will indicate CAP values, and VPI of reading point



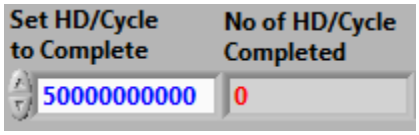
8. The front panel below will indicate VSA, HS check, EFUSE, % delta C of reading point



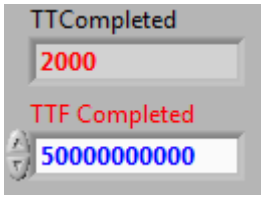
9. These graphs will monitor the CMIN changes during the stress



Note:
We can stop the stress by enter the number that will be completed stress



This box will be found on page 2 (Data Output) of the test program



This box will be found on page 3 (VSA Output) of the test program.