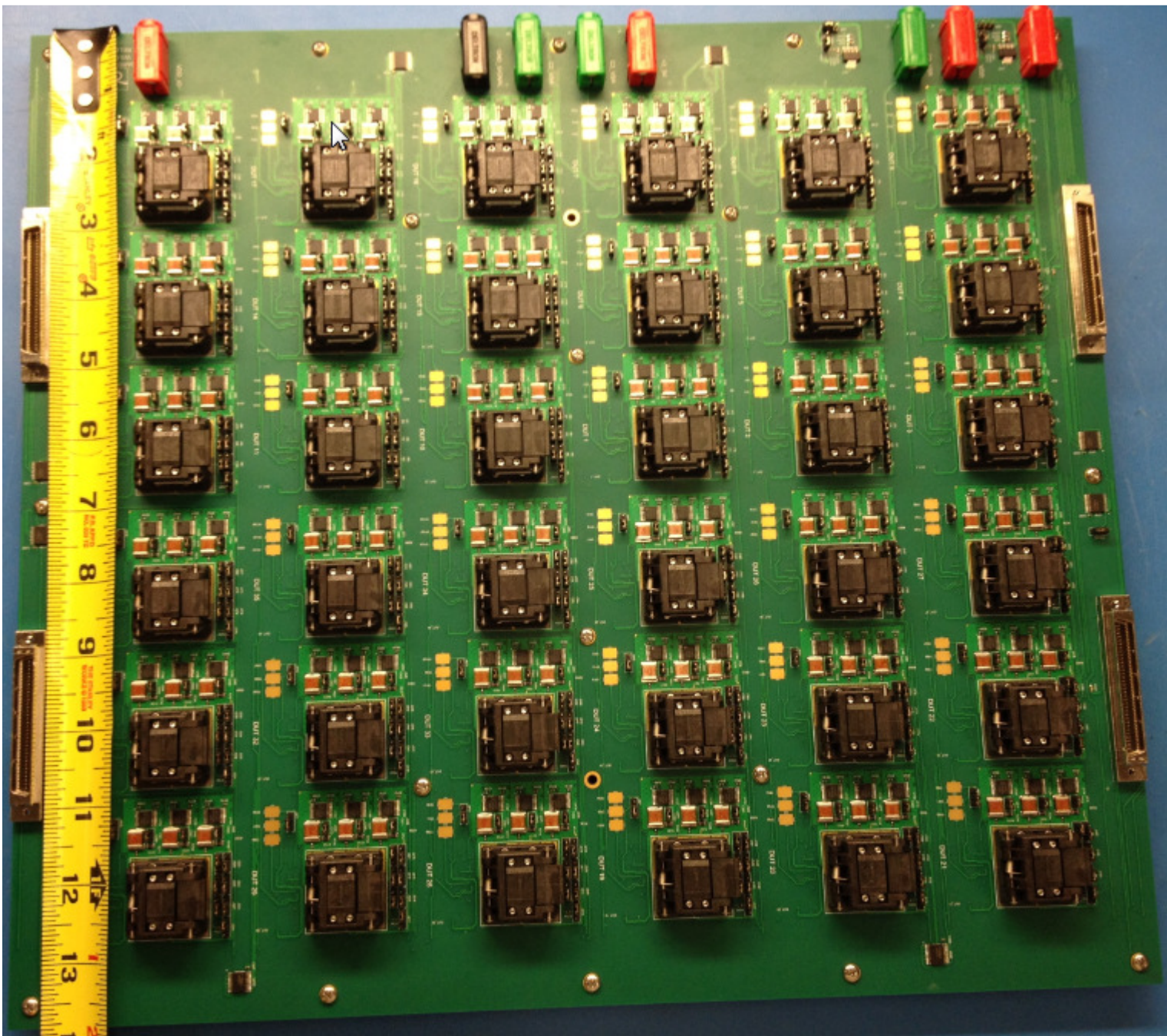


36 DUT Board Layout:



Test Setup Block Diagram:

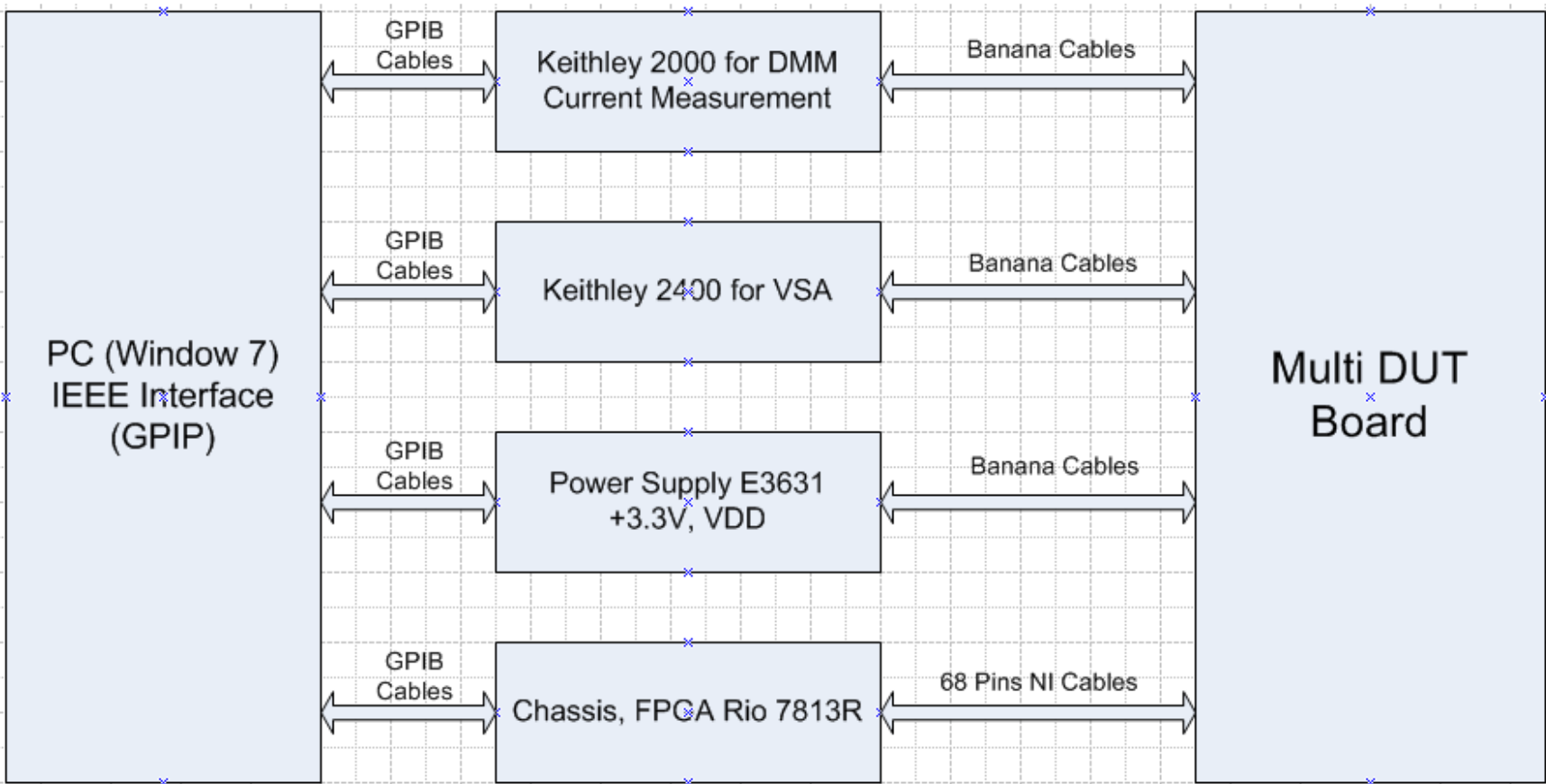


Fig 1. Test Setup Block Diagram

Hardware:

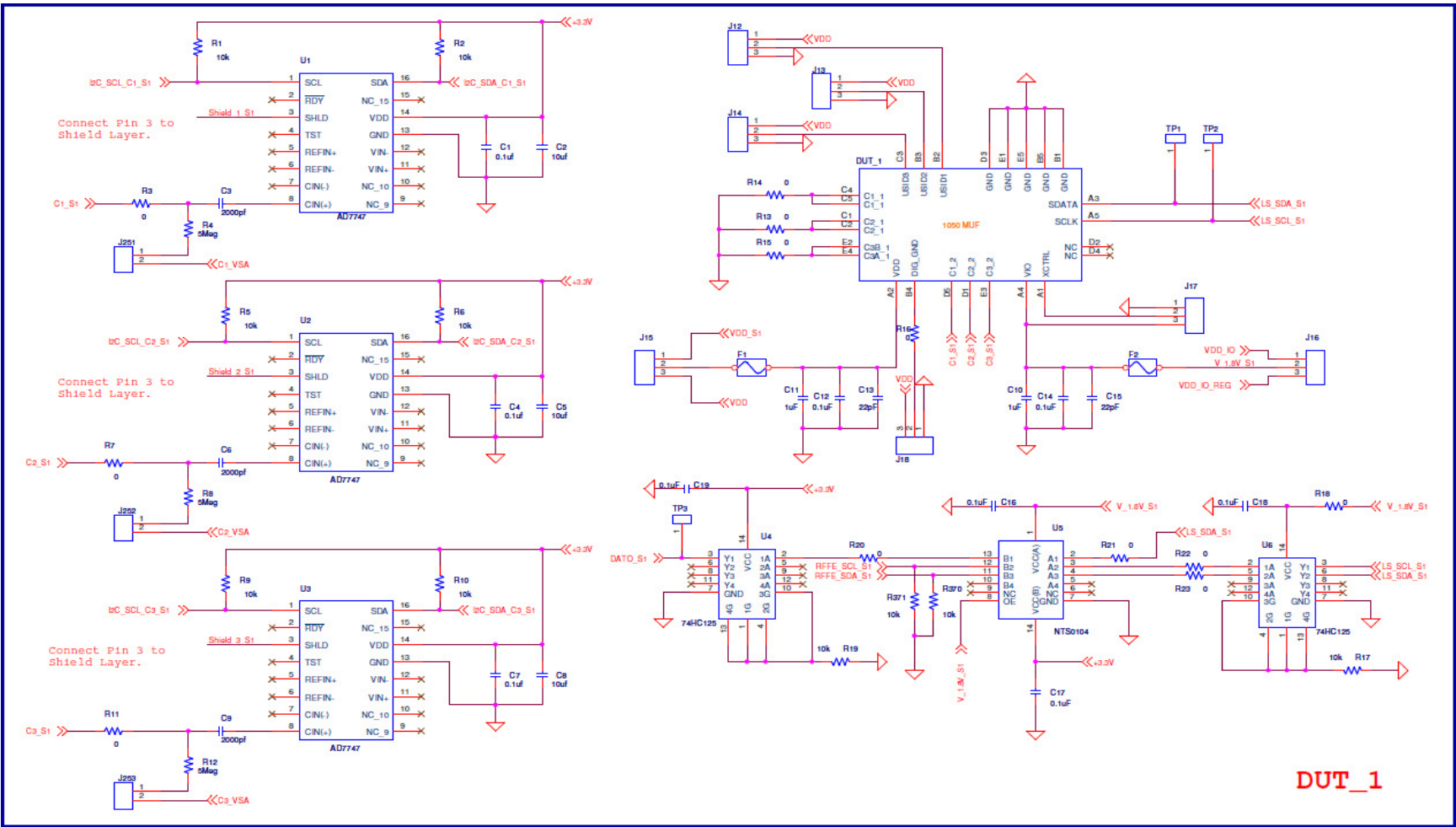
- 1. Keithley 2000 (DMM)
- 2. Keithley 2400 (Source meter for VSA test)
- 3. Agilent Power supply E3631 (Power source for +3.3V, VDD)
- 4. Chassis PXI 1033
- 5. FPGA card Rio 7813R, 160 digital I/O channels
- 6. SHC68-68-RDIO Cables (4)
- 7. Several banana plugs

Software:

- 1. FPGA Revision :
 - a. WS_VCAP Driver 029 (36 DUT)
 - b. WS_VCAP Driver 024 (16 DUT)
- 2. Stress Test Program
 - a. WS1050 36 DUT Reliability HD_Cycling Ver1.3 (36 DUT)
 - b. WS1050 16 DUT Reliability HD_Cycling Ver1.8 (16 DUT)

Schematic:

- 1. Schematic WS1050 36 DUT Reliability REV E.
- 2. Schematic WS1050 16 DUT Reliability REV G.



Test Sequences:

- 1. Turn ON +3.3V, this will turn on AD7747 and voltage regulator LM317 to generate 1.8V for VIO
- 2. Turn ON VDD (HD = 3.3V; Cycle = 3.7V)
- 3. Set CP OFF
- 4. Measure IDD standby
- 5. Set CP Voltage to stress
- 6. Set DVA (ON/OFF)
- 7. Set ECAL (ON/OFF)
- 8. Set VPI (ON/OFF) Note: If VPI OFF, skip steps 31 to 41.
- 9. Set VSA (ON/OFF) Note: If VSA OFF, skip steps 42 to 54.
- 10. Set HS (ON/OFF) Note: If HS check OFF, skip step 55.
- 11. Start HD/Cycle (Non linear RP).
- 12. Turn All Drivers ON
- 13. Measure IDD All Drivers ON
- 14. Turn All Drivers OFF
- 15. Measure IDD All Drivers OFF
- 16. Measure C1_Min
- 17. Measure C1_F1
- 18. Measure C1_F2
- 19. Measure C1_S1 to C1_S14F12

- 20.Measure C1_Min2
- 21.Measure C2_Min
- 22.Measure C2_F1
- 23.Measure C2_F2
- 24.Measure C2_S1 to C2_S14F12
- 25.Measure C2_Min2
- 26.Measure C3_Min
- 27.Measure C3_F1
- 28.Measure C3_F2
- 29.Measure C3_S1 to C3_S14F12
- 30.Measure C3_Min2
- 31.Set DVA OFF, ECAL OFF (this is for VPI)
- 32.Set CP Voltage for VPI
- 33.Measure C1_Min
- 34.Measure C1_Max
- 35.Measure C1_Min2
- 36.Measure C2_Min
- 37.Measure C2_Max
- 38.Measure C2_Min2
- 39.Measure C3_Min
- 40.Measure C3_Max
- 41.Measure C3_Min2
- 42.Set Ke2400 to V1 = -10V
- 43.Measure VSA C1_V1
- 44.Measure VSA C2_V1
- 45.Measure VSA C3_V1
- 46.Set Ke2400 to V2 = 0V
- 47.Measure VSA C1_V2
- 48.Measure VSA C2_V2
- 49.Measure VSA C3_V2
- 50.Set Ke2400 to V3 = 10V
- 51.Measure VSA C1_V3
- 52.Measure VSA C2_V3
- 53.Measure VSA C3_V3
- 54.Set Ke2400 to 0V.
- 55.Run HS check on Register 1 (bank C1)
- 56.Save Data
- 57.Loop back to step 11

Note:

Test Sequence: Test program can measure read point by order, C1-C2-C3; C2-C1-C3 or C3-C2-C1

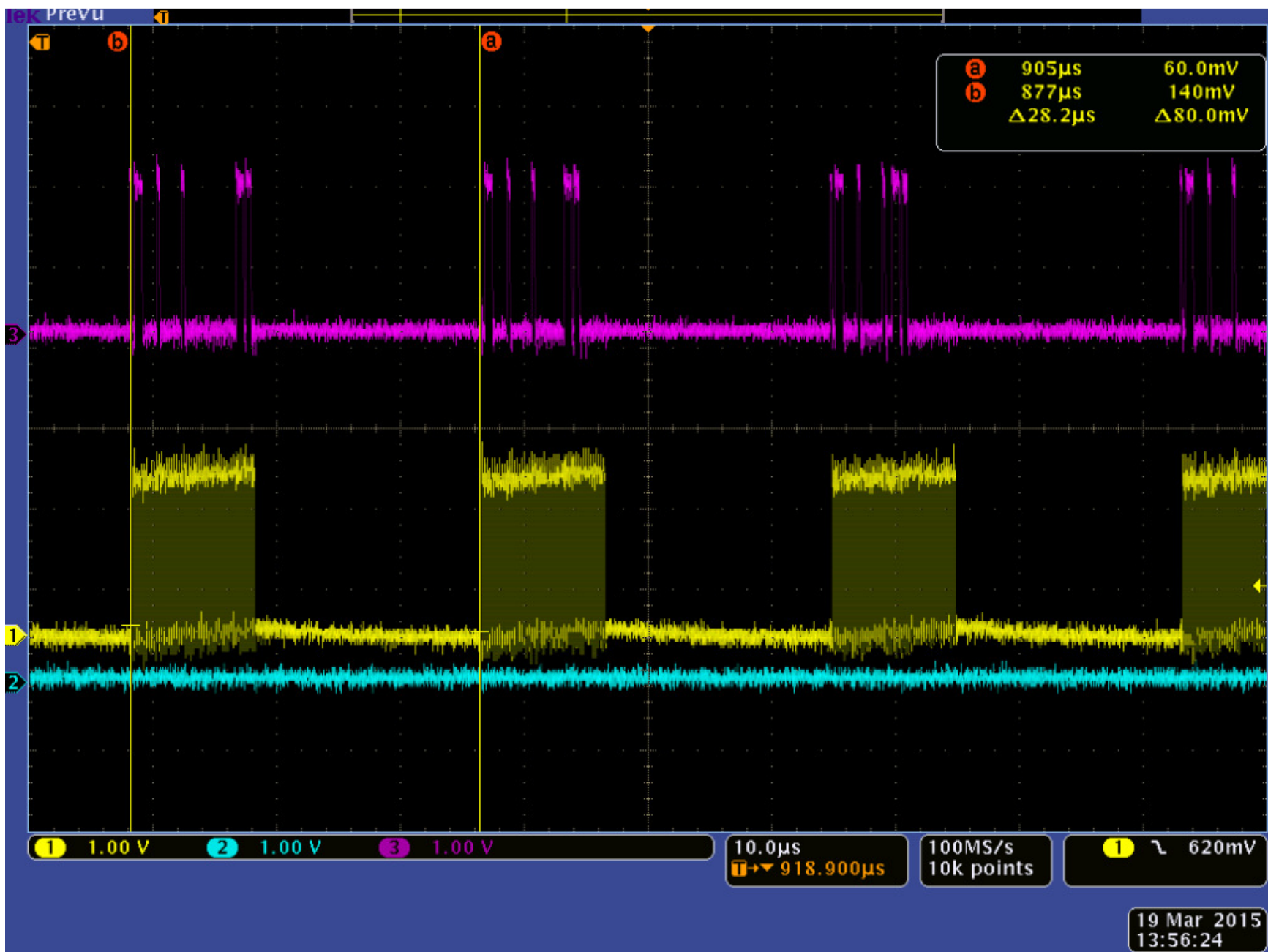
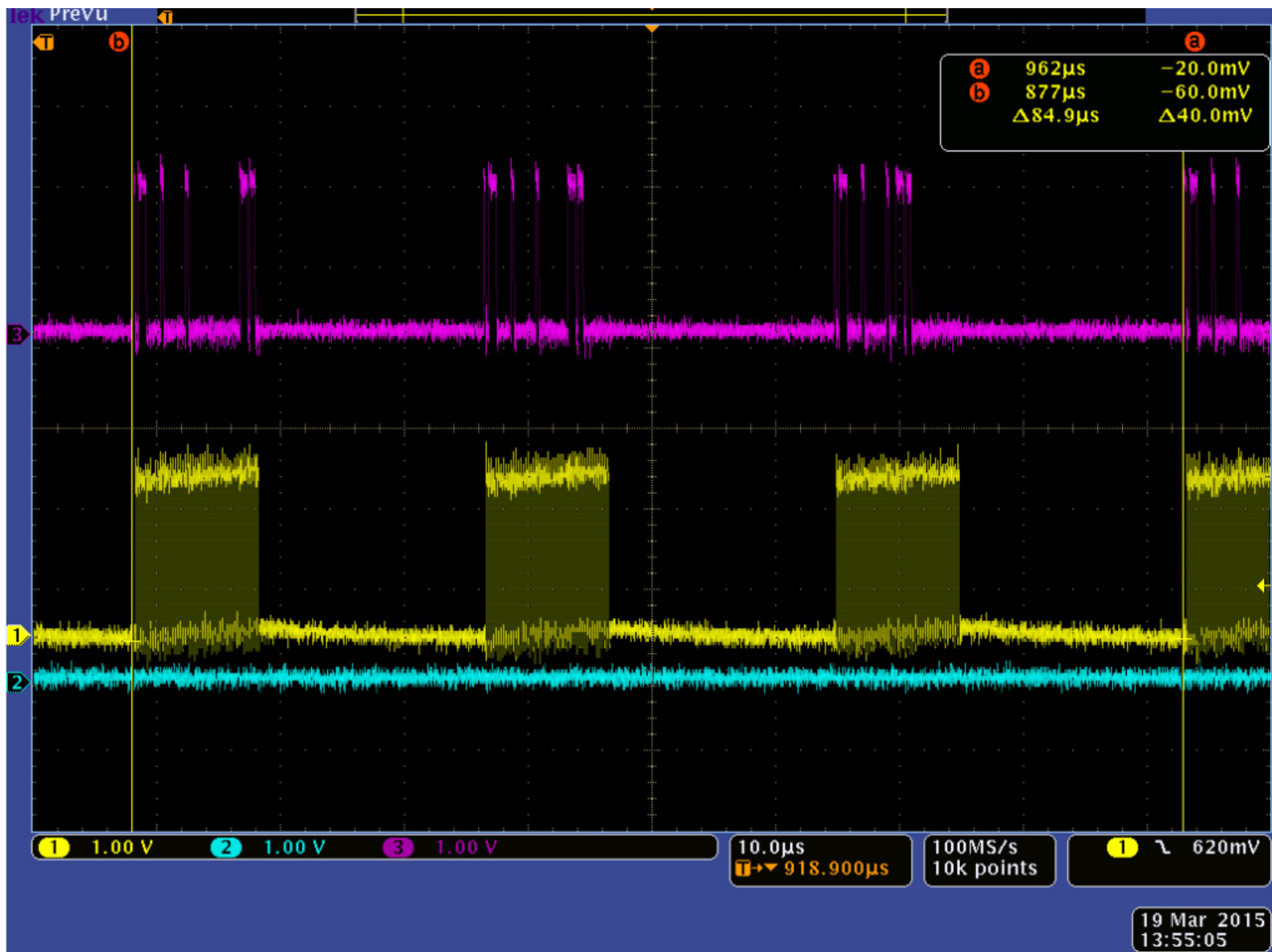
Stress Sequence: Test program can stress parts by order by setting commands:

070201|XX|XX|XX
070201|XX|XX|XX
070201|XX|XX|XX

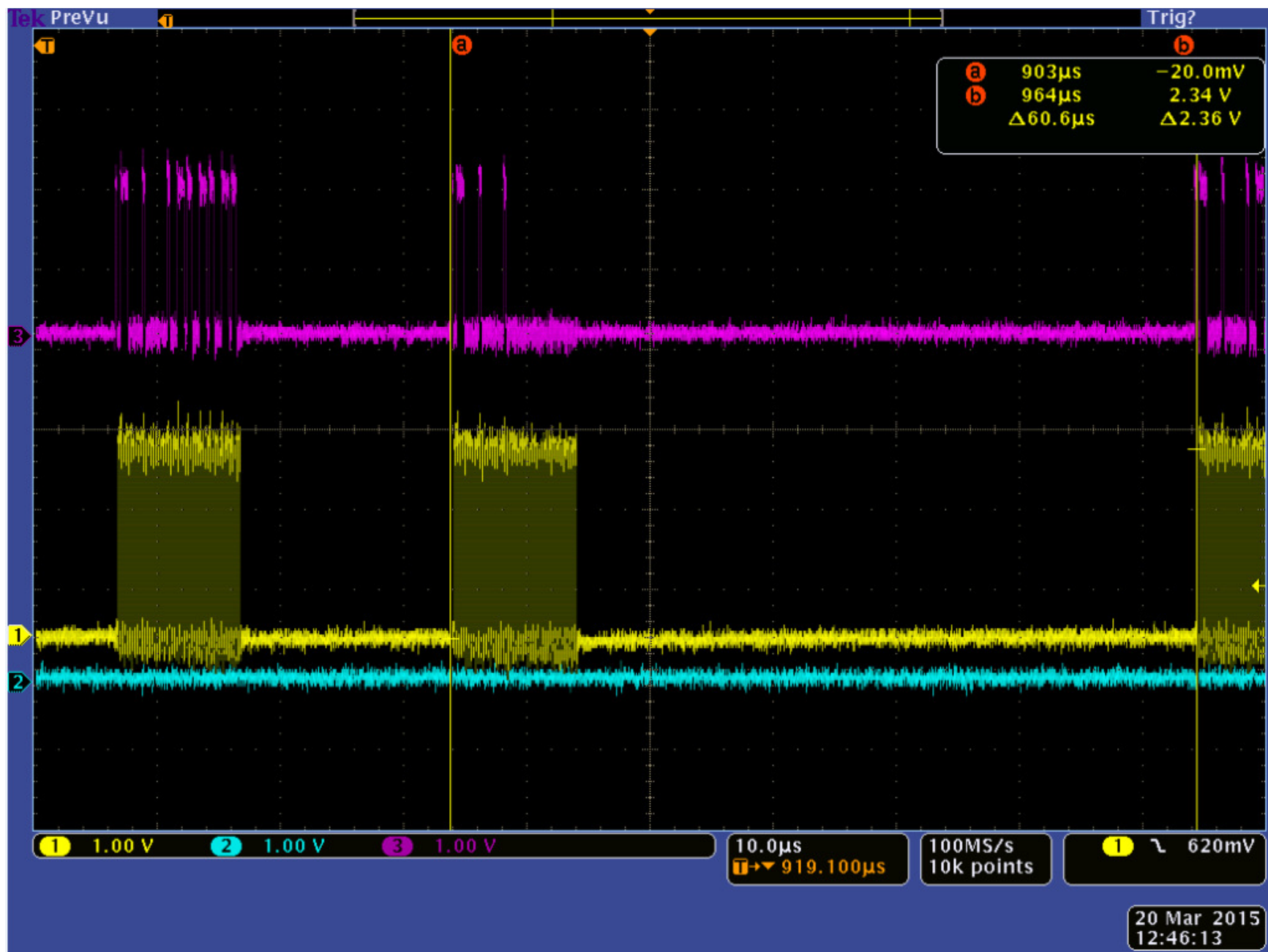
XX can be 3B all drivers ON
XX can be 00 all drivers OFF

Cycling speed is12KHz with signal CLK is 5MHz.

With 33% Duty Cycle:



With 25% Duty Cycle



1. Main GUI for calibration and set up test:

[illegible]

2. GUI to monitor the test setup (CP voltage, DVA ON/OFF, ECAL ON/OFF) before stress, monitor cap values for each drivers, and time completed stress

Instrument Control | Data Output | VSA Output | Graphs

40V_1 40V_2 40V_3 VPI C1 VPI C2 VPI C3

Set HD/Cycle to Complete: 50000000000
No of HD/Cycle Completed: 0
Loop completed: 1

Cycle Count: 0
Previous Time: 12:20:26 PM

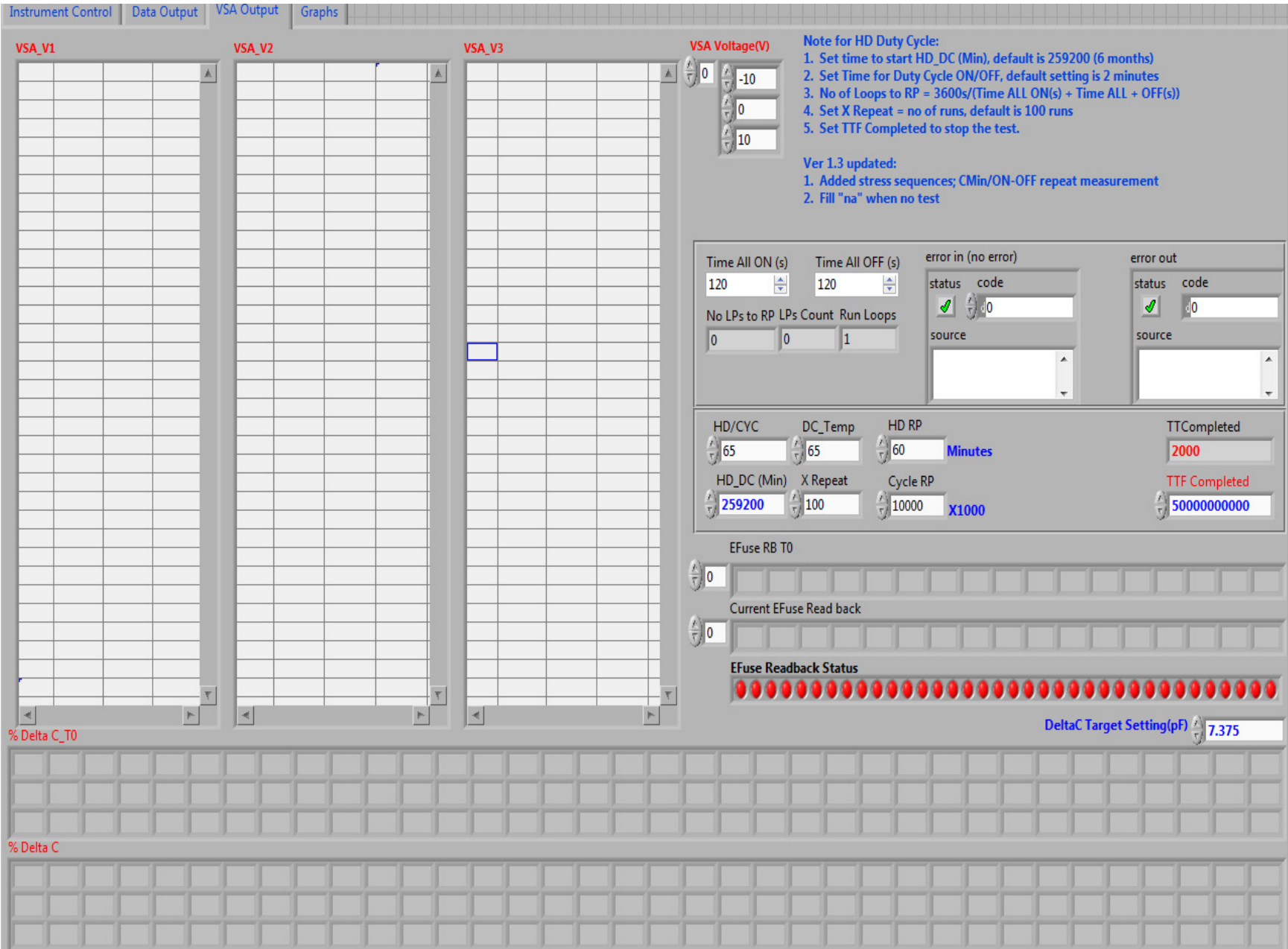
RB Reg for HD
RB Reg for HD/Cycle

IDD_HD/CYC (uA): 164.601255E+0
IDD Stdbby(uA): 2.606990E+0
NOM IDD ON (uA):
NOM IDD OFF(uA):

STATUS
Idle....

ABORT TEST Quit

3. GUI to monitor VSA test, HS check, EFUSE read back and % Delta C change



4. GUI to monitor CMIN changes during the stress

