

WS1050 Package parts 36 DUT Reliability Test Procedures

Introduction:

The purpose of this test procedure is for set up to run Hold Down and Cycle on package parts, toggle 7, WS1050 from 36 DUT board, and this test procedure will be used for internal only.

Hardware and Software requirement:

- a. Hardware:
 1. Agilent 3631A, This PS will be used for VDD, +3.3V
 2. Ke2000 as a DMM for current measurement
 3. Ke2400 for VSA test (positive and negative voltages)
 4. PXI 1033 chassis
 5. NI PXI-7813R, FPGA Card for RFFE and I2C
 6. 4 NI Cables, SHC68-68-RDIO Cable
 7. 36 DUT Board
 8. Several banana cables

- b. Software:

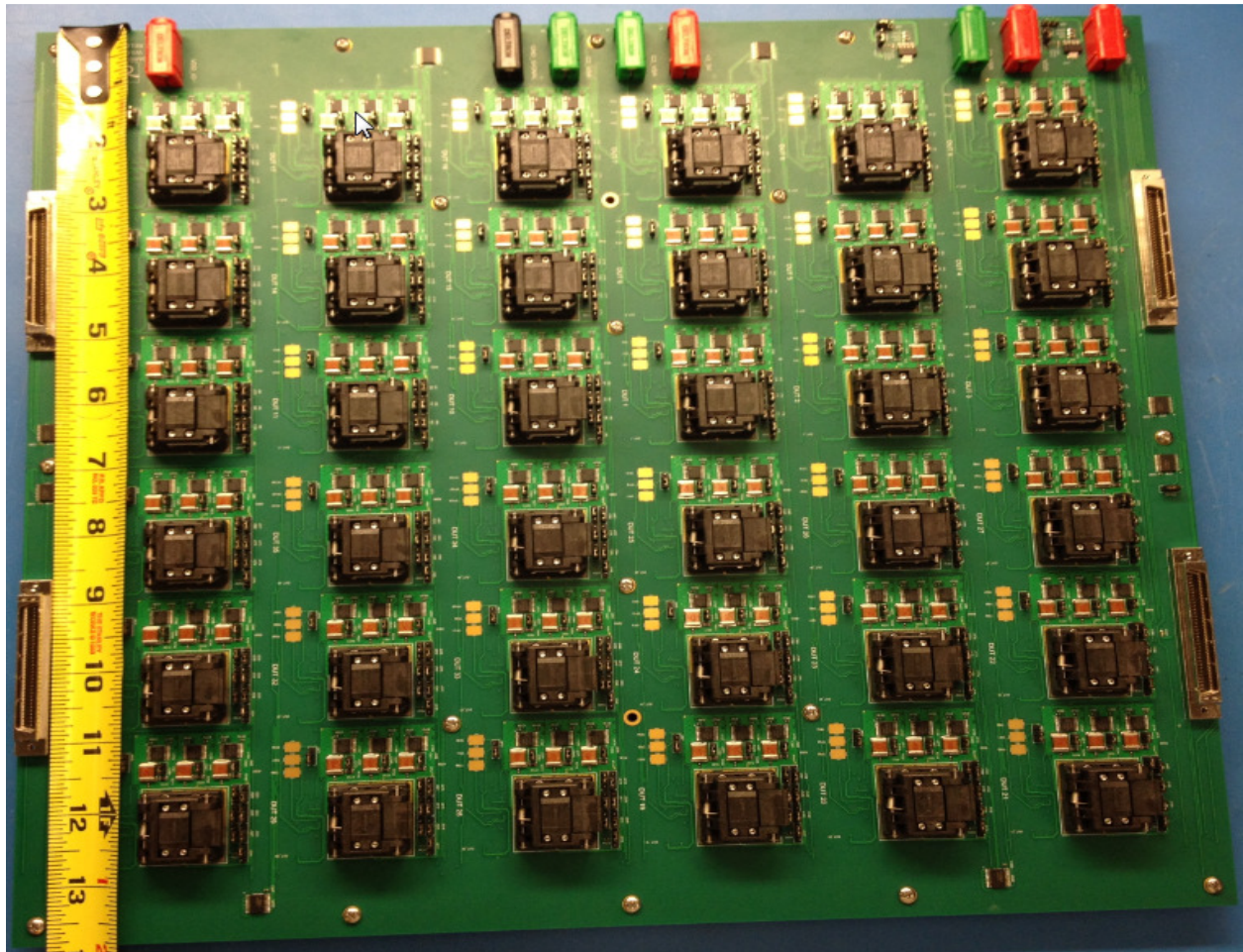
Test program: Executable for WS1050 36 DUT Reliability HD_Cycling Ver1.4

[illegible]

This test program will be found at the link below:

S:\Software_Control\Released\36 DUT Board\WS1050 36 DUT Reliability HD_Cycling
Ver1.4

36 DUT Board:



Test Set up Block Diagram:

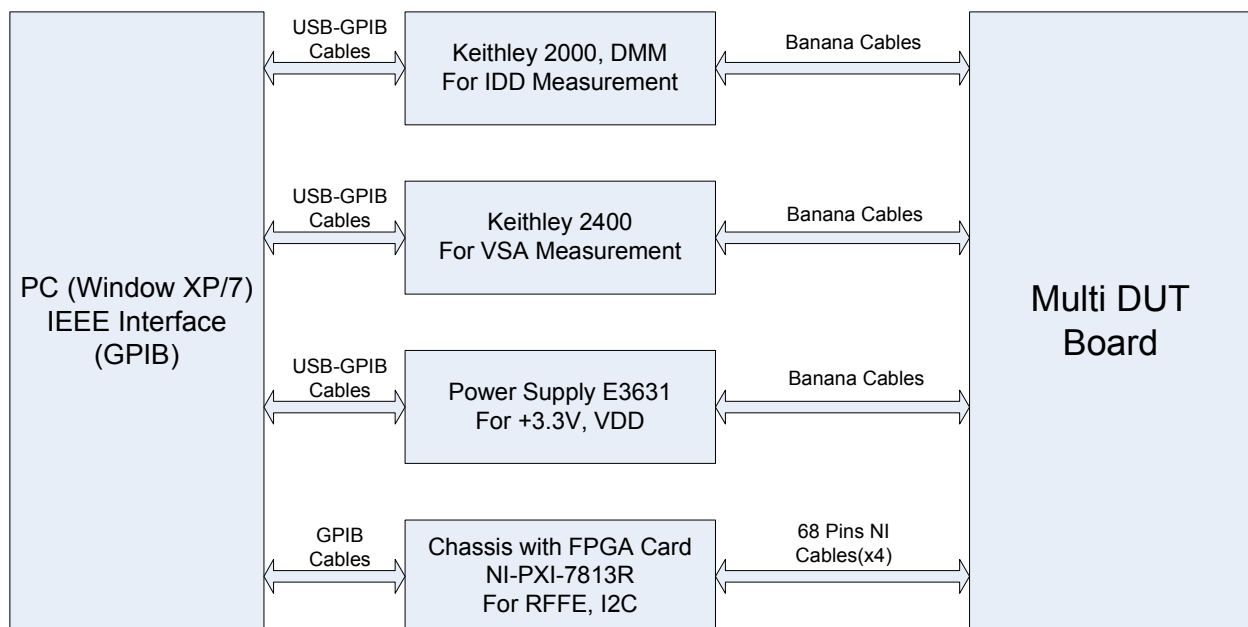

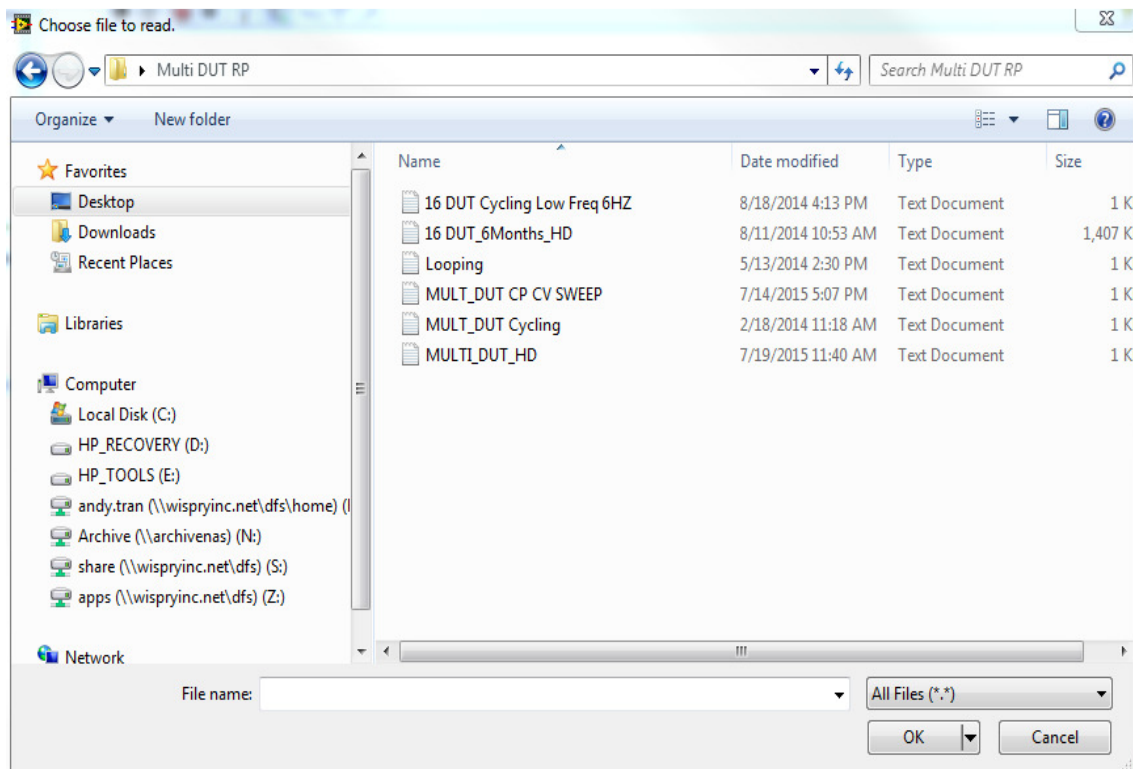


Fig 1. Test Setup Block Diagram

Set up and run Test Program:

1. Set temperatures from the oven/chamber:
Adjust temperatures from the oven/chamber to meet the requirement (25C, 45C, 55C, 65C or 85C)
2. From the labVIEW test program click  this button to run the test program, it will pop up a dialog box to ask for a look up table for read point.



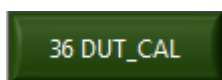
Note: it will depend on what stress you are running to pick the correct file.

For instance:

If you are running cycling, the file will be selected is MULT_DUT Cycling

If you are running Hold Down, the file will be selected is MULT_DUT HD

3. For Calibration Multi DUT, make sure all sockets are empty and the CAP values of 36 DUT will be ~0 for all three banks. If not, click on 36 DUT_CAL button



to zero out the sockets, then click STOP CAL button



to stop the calibration.

Ke2400

GPIO0::3:

PS1 Source

GPIO0::5::INSTR

Ke2000

GPIO0::9::INSTR

36 DUT_CAL

STOP CAL

IDD Brd(uA)

0x80

0x80

0x80

Initialize AD7747

DUT Mask Mode

All

Reset P/S

NO

WS1050/51

1050

Test Sequences

C1_C2_C3

AD7747 Values

	C1 Status	C1 Cap (pF)	C2 Status	C2 Cap (pF)	C3 Status	C3 Cap (pF)	Serial Number	
							DUT	SN
DUT 01							DUT1	1
DUT 02							DUT2	2
DUT 03							DUT3	3
DUT 04							DUT4	4
DUT 05							DUT5	5
DUT 06							DUT6	6
DUT 07							DUT7	7
DUT 08							DUT8	8
DUT 09							DUT9	9
DUT 10							DUT10	10
DUT 11							DUT11	11
DUT 12							DUT12	12
DUT 13							DUT13	13
DUT 14							DUT14	14
DUT 15							DUT15	15
DUT 16							DUT16	16
DUT 17							DUT17	17
DUT 18							DUT18	18
DUT 19							DUT19	19
DUT 20							DUT20	20
DUT 21							DUT21	21
DUT 22							DUT22	22
DUT 23							DUT23	23
DUT 24							DUT24	24
DUT 25							DUT25	25
DUT 26							DUT26	26
DUT 27							DUT27	27
DUT 28							DUT28	28
DUT 29							DUT29	29
DUT 30							DUT30	30
DUT 31							DUT31	31
DUT 32							DUT32	32
DUT 33							DUT33	33
DUT 34							DUT34	34
DUT 35							DUT35	35
DUT 36							DUT36	36

Note: If sockets are not zeros “~0”, click on Initialize AD7747 button

Initialize AD7747 to initial ADI chip, the CAP values will be ~0.45pF for all three banks of 36 DUT. Click on 36 DUT_CAL button to zero out the sockets and click on Stop Cal to stop the calibration.

4. Setup test conditions. This step is a very important step to set up for stressing parts. Therefore, confirm with the people (Dana/Shawn/Mark) whoever requested for this setup.
 - a. Setup with standard stress (cycle): All drivers ON, All Drivers OFF, 25% Duty
Make sure the numbers will be set as same as the boxes below (this number will be set by default when open the test program)

% Duty Cycle		Post CMd Delay	Command
25	No of Cmd	17u s	0702013B3B3B
	2	54u s	070201000000

- b. Setup with special stress (cycle): C1 ON, C1 OFF C2 ON, C2 OFF C3 ON, C3 OFF C1 ON. 33% Duty. Make sure all the numbers will be set as same as the boxes below

% Duty Cycle		Post CMd Delay	Command
33	No of Cmd	18u s	0702013B0000
		18u s	070201003B00
	3	18u s	07020100003B

- c. The front panel below is for more test setup conditions: HD/CYC, E-CAL ON/OFF; DVA ON/OFF; VPI ON/OFF; VSA ON/OFF; HS ON/OFF. Note: CYC, VPI, VSA and HS were setup "ON" by default

% Duty Cycle		Post CMd Delay	Command	Control Panel	
33	No of Cmd	18u s	07020100003B	Verify Socket <input type="checkbox"/> NO	Verify Socket <input type="button" value="NO"/>
		18u s	070201003B00	HD/CYC <input type="checkbox"/> CYC	HD/CYC <input type="button" value="CYC"/>
	3	18u s	0702013B0000	E-CAL <input type="checkbox"/> NO	E-CAL <input type="button" value="NO"/>
Cycle Speed	Cmd To HD		0702013B3B3B	DVA <input type="checkbox"/> NO	DVA <input type="button" value="NO"/>
5.0M Hz	Cmin/Act	Repeat Meas(s)		VPI <input checked="" type="checkbox"/> YES	VPI <input type="button" value="NO"/>
Meas Speed	Act	900		VSA <input checked="" type="checkbox"/> YES	VSA <input type="button" value="NO"/>
1.0M Hz				HS <input checked="" type="checkbox"/> YES	HS <input type="button" value="NO"/>
Freq(Hz)	Set VDD	CP to HD/Cycle			
12K	3.300	CP HDC 40.25V			
CP Setting	Verify CP	CP to Meas			
CP OFF	SEND	CP HDC 40.25V			
		CP VPI			
		CP HDC 35V			
		CP with DVA ON			
		CP HDC 35V			
Real No. From Lookup Table	NO				

5. The front panel below is setup for data output

Lot#	Wafer#	Board#	TMN DC\CAP Data Log File Path
<input type="text"/> WS1050	<input type="text"/> T7-EB	<input type="text"/> BRD5	<input type="text"/> C:\WS1050_36 DUT Data

File Name
 CYC_WS1050_T7_EB_65C_40V_25DC_EMPTY_BRD5_141017_1

Comment
 CYC65C40V Offline FPGA Mode

```

05/19/2014 -- 12:24:35.853::WSVCAP::APP::Application Started
05/19/2014 -- 12:24:37.606::WSVCAP::WSVCAP SHL::WR I2C-REG:0x0A;MASK:
0xFFFFFFFFFFFF;C1 DATA:22:22:22:22:22:22:22:22:22:22:22:22:22:22:22:22:C2 DATA:22:22:22:22:
22:22:22:22:22:22:22:22:22:22:22:22:C3 DATA:22:22:22:22:22:22:22:22:22:22:22:22:22:22:22:
05/19/2014 -- 12:24:37.773::WSVCAP::WSVCAP SHL::WR I2C-ST:0,0,4,1
    
```

Note: The file name will be

Stress_Lot#_Wafer#_Design_Temperature_CPV_Duty cycle_Brd#_yyymmdd_run

6. The session below is to setup for day and time to run stress: We can start to run the test immediately by click on the START TEST button or we can setup date and time to run the test by enter the Start Date and Start Time

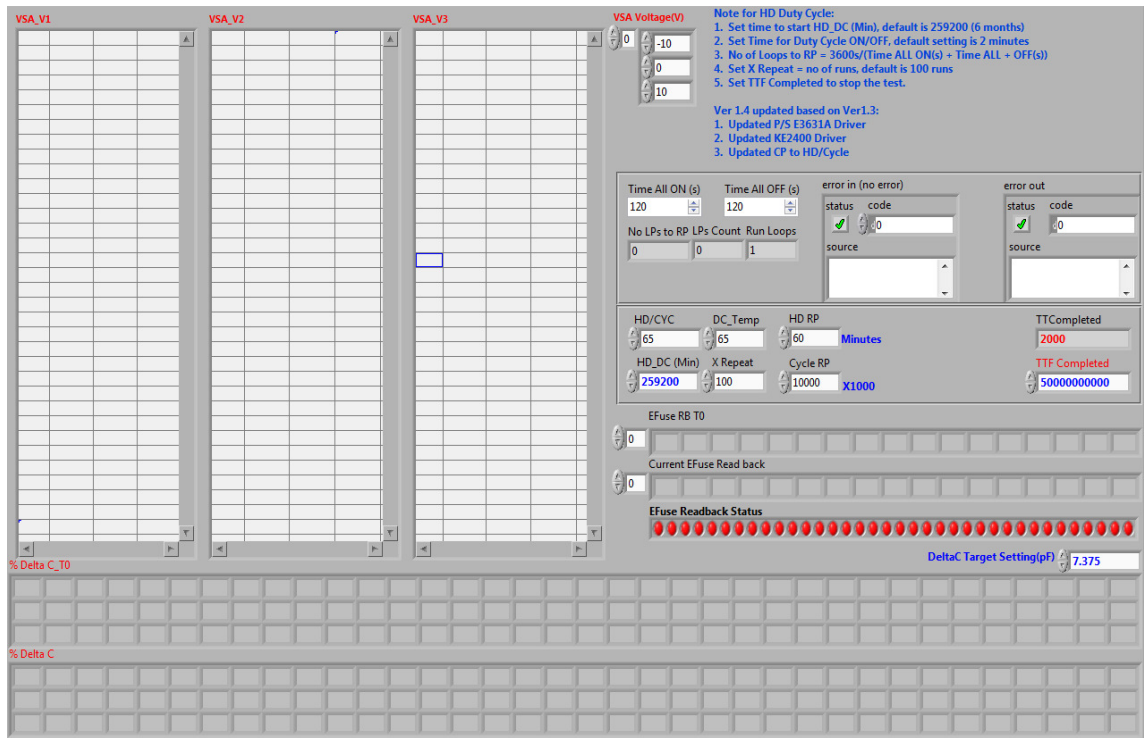
Current Date	Current Time
8/28/2014	0950
Start Date	Start Time
10/21/2014	1542
START TEST	

7. The front panel below will indicate CAP values, and VPI of reading point

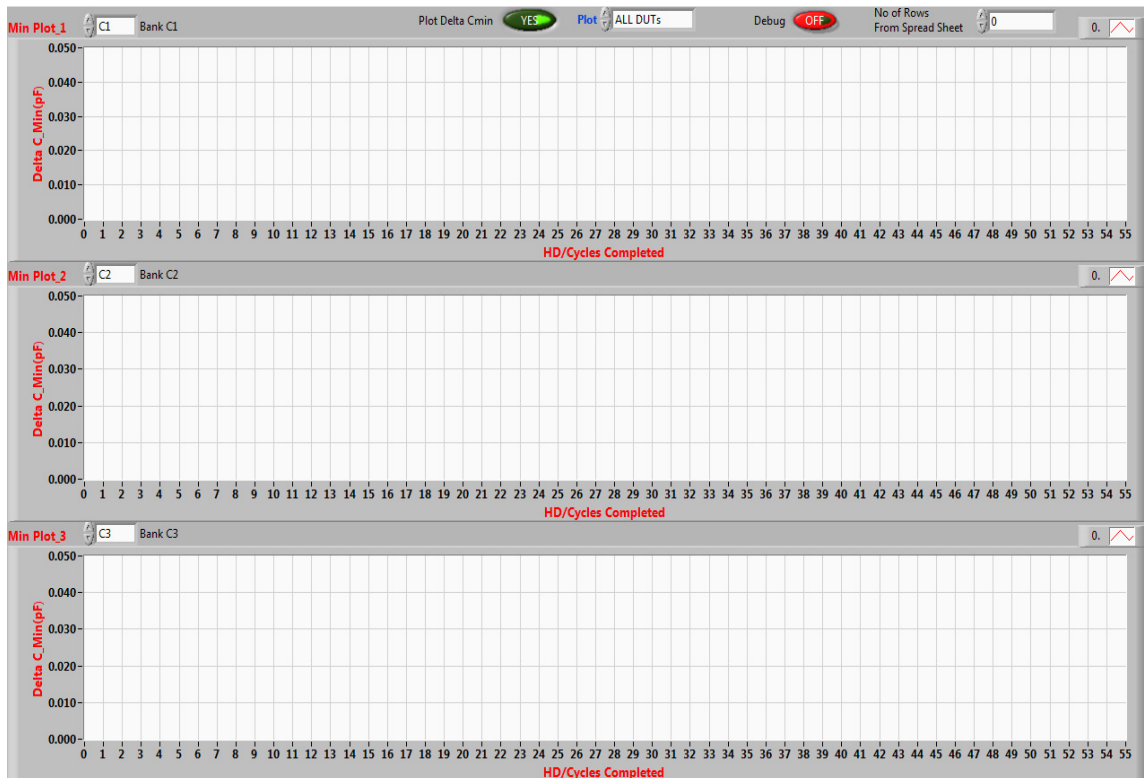
The screenshot displays the HP DesignStart software interface during a test. At the top, there are six empty data tables labeled CAP_C1, CAP_C2, CAP_C3, VPI_C1, VPI_C2, and VPI_C3. Each table has a vertical axis labeled 'Y' and a horizontal axis labeled 'X'. The bottom status bar shows the following information:

- Set HD/Cycle to Complete:** 50000000000
- No of HD/Cycle Completed:** 0
- Loop completed:** 1
- RB Reg for HD:** (empty field)
- RB Reg for HD/Cycle:** (empty field)
- IDD_HD/CYC (uA):** 164.601255E+0
- IDD Stdby(uA):** 2.606990E+0
- NOM IDD ON (uA):** (empty field)
- NOM IDD OFF(uA):** (empty field)
- STATUS:** Idle....
- Buttons:** ABORT TEST, Quit

8. The front panel below will indicate VSA, HS check, EFUSE, % delta C of reading point



9. These graphs will monitor the CMIN changes during the stress



Note:

We can stop the stress by enter the number that will be completed stress

Set HD/Cycle to Complete	No of HD/Cycle Completed
50000000000	0

This box will be found on page 2 (Data Output) of the test program

TTCompleted
2000
TTF Completed
50000000000

This box will be found on page 3 (VSA Output) of the test program.