

**PE-xxxx  
Revision A**

**WS1050 MEMS CYCLING AND HOLD DOWN**

**TEST PROCEDURE**

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## 1. Purpose and Scope

### 1.1 Purpose

This document defines the procedures and requirements for cycling and holding down stresses for MEMS capacitors.

### 1.2 Scope

This procedure applies to the qualification and ongoing production monitoring of all WiSpry products.

## 2. Responsibilities

The Product Engineering function is responsible for assuring compliance to the requirements of this document.

## 3. REFERENCE DOCUMENTS

Document No.	Document Name
PE-0002	Equipment Calibration Procedure

## 4. FORMS

Form No.	Form Name

## 5. DEFINITIONS (Not Applicable)

## 6. EQUIPMENT AND MATERIALS

Equipment consists of:

Item	Model	Manufacturer	Comments
Computer (equipment controller)	PC with Window XP, 7	Any	
Software (equipment controller)	LabView 2012 or Higher		
GPIO-USB-HS	778927-01	National Instruments	
Triple Output Power Supply	E3631A	Agilent/Keysight	w/ GPIO interface
Source Meter	2400	Keithley	w/ GPIO interface
DMM	2000	Keithley	w/GPIO interface
FPGA	PIX-7813R	National Instruments	
PXI Card Chassis	PIX-1033	National Instruments	
DUT boards	Various <sup>1</sup>	---	WiSpry Design
SHC68-68-RDIO Shielded Cable	191667-01	National Instruments	NI Cables

Notes:

<sup>1</sup> WS1050 board is 36 positions (model WS-EVB-165)

## 7. REQUIREMENTS AND PROCEDURES

### 7.1 Basic Hardware, Software, and Environmental Requirements

- Cycling and hold down hardware (boards, cables, connectors, bench equipment) must be able to:
  - Meet the electrical conditions specified in sections 7.2 and 7.3.
  - Meet WiSpry calibration requirements specified in PE-0002.
  - Be sufficiently robust to ensure minimum leakage currents.
- Cycling and hold down software should:
  - Allow for insitu monitoring for stiction events.
  - Meet the electrical conditions specified in sections 7.2 and 7.3.
- Cycling and hold down environmental controls shall:
  - Provide control of temperature and **humidity**.
  - Meet calibration requirements defined in PE-0002.

## 7.2 MEMS Cycling

The cycling conditions for product qualification and ongoing monitoring are:

Stress Condition	Requirement
MEMS Operating Voltage ( $V_{OP}$ )	44 V
$V_{DD}$	3.7 V @ 12 KHz
Temperature	65 °C
Frequency	12 KHz
Duty Cycle	25%
Dual Voltage Actuation (DVA)	OFF
Beam Actuation	All beams cycles simultaneously

## 7.3 MEMS Hold Down

The hold down conditions for product qualification and ongoing monitoring are:

Stress Condition	Requirement
MEMS Operating Voltage ( $V_{OP}$ )	44 V
$V_{DD}$	3.3 V
Temperature	65 °C
Frequency	----
Duty Cycle	100%
Dual Voltage Actuation (DVA)	OFF
Beam Actuation	All beams cycles simultaneously and held for the stress duration

## 7.4 Reject Criteria

For both cycling and hold down, the following conditions define a reject reading:

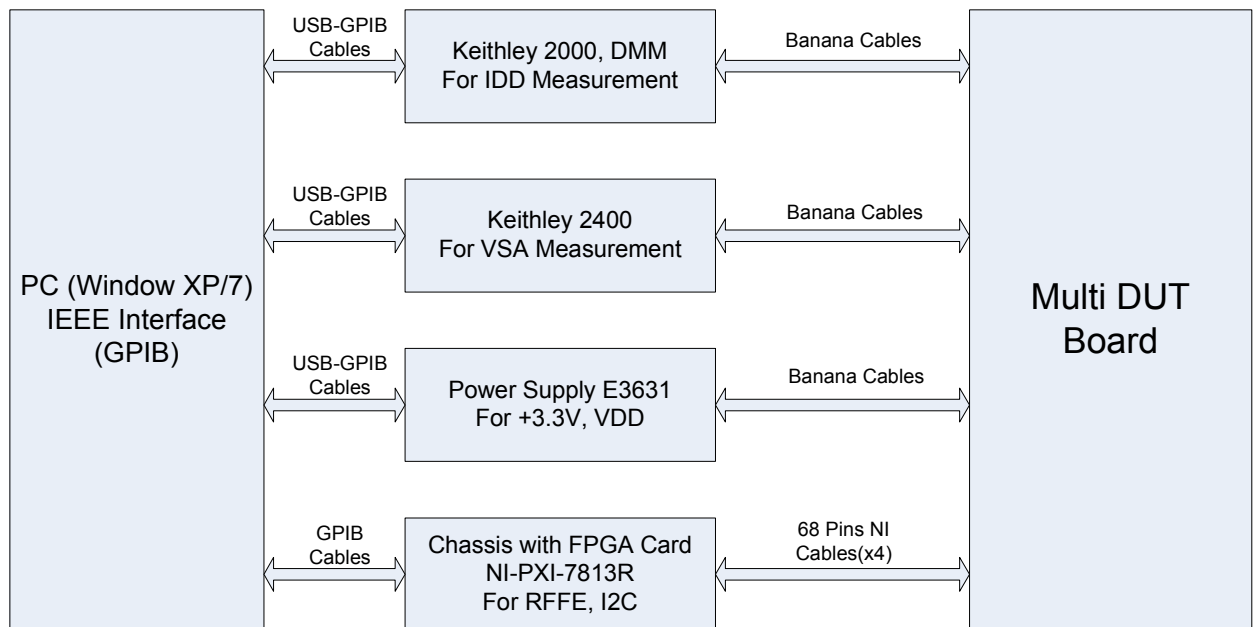
$$C_{OFF} \pm 46 \text{ fF per bank}$$
$$C_{ON} \pm 657 \text{ fF per bank}$$

## 7.5 General Set-up and Handling Guidelines

- Handling recommendations for ESD
- Stabilize oven temperature prior to loading parts, 15 minutes minimum
- Preconditioning of new stress boards (to remove excess moisture absorption), 24 hour bake at 85C
- Optimal method to load boards
- Special software instructions
- Best way to unload parts
- Socket inspection after each run and cleaning/repair as required
- Sample control and storage post stress

## 7.6 Test Set-up Procedure

- Figure 1 shows the test set-up block diagram for WS1050 Reliability Test, Multi DUT.
  - Using banana plug cables to connect all test equipments as in Figure 1.
  - For power supply E3631A, use channel 1 for VDD, channel 2 for +3.3V.



**Figure 1 Test Set-up Block Diagram**

- Figure 2 shows the front panel of the test program (for the WS1050 version 1.4)
- Contact WiSpry Engineering for the latest version of the test program.
- Test programs are located in directory S:\Software\_Control\Released\36 DUT Board

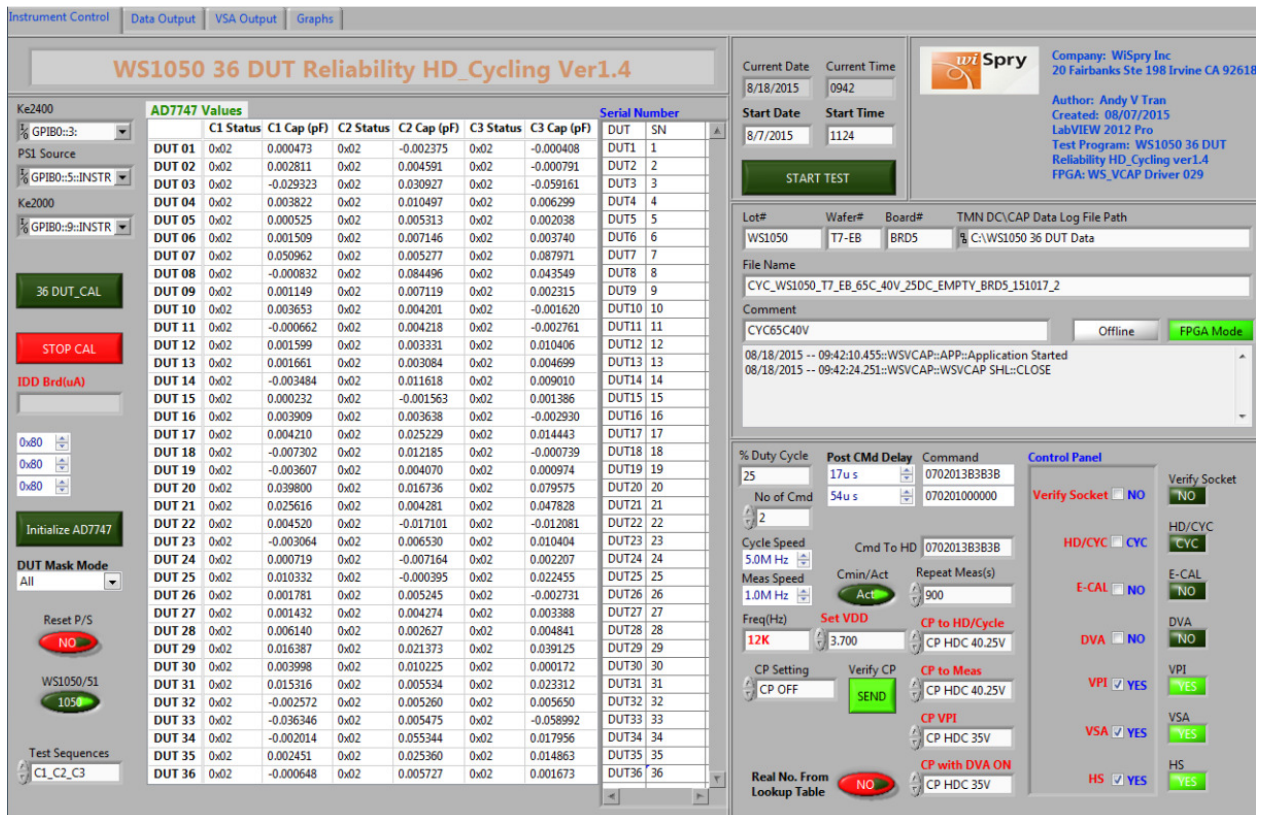

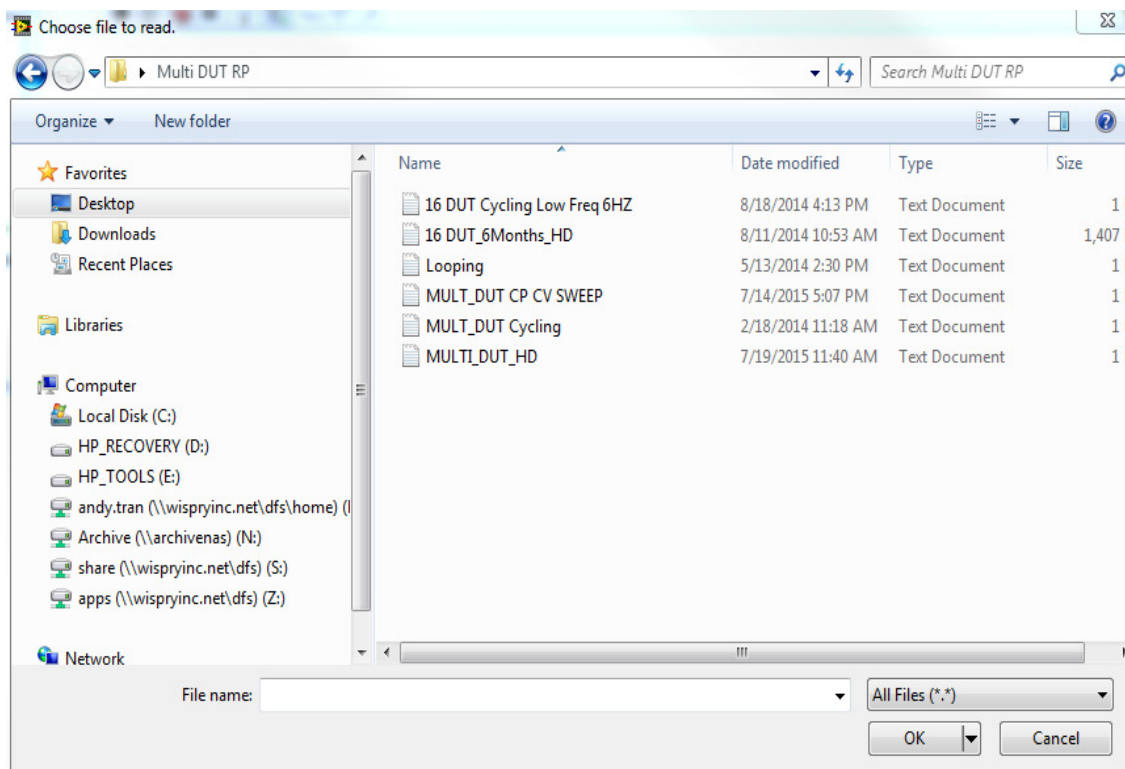


Figure 2

## 7.7 Test Operating Procedure

- Set temperature from oven/chamber
  - Adjust temperatures from oven/chamber to meet the requirement (for example 25C, 45C, 65C)
- Set-up test program
  - From labVIEW test program click  this button at the top left corner to run the test program, it will pop-up a dialog box (Figure 3) below to ask the look up table for read point



**Figure 3**

**Note:**

Selecting the correct file depends on the stress being run;

- Select **MULT\_DUT Cycling** for cycling test
- Select **MULT\_DUT HD** for hold down test



- For calibration (Figure 4): Make sure all sockets are empty and the capacitance values of 36 DUT are around zeros “~0” for all three banks. If not, click on 36 DUT\_CAL button

36 DUT\_CAL

STOP CAL

to zero out the sockets, then click STOP CAL button to stop the calibration.

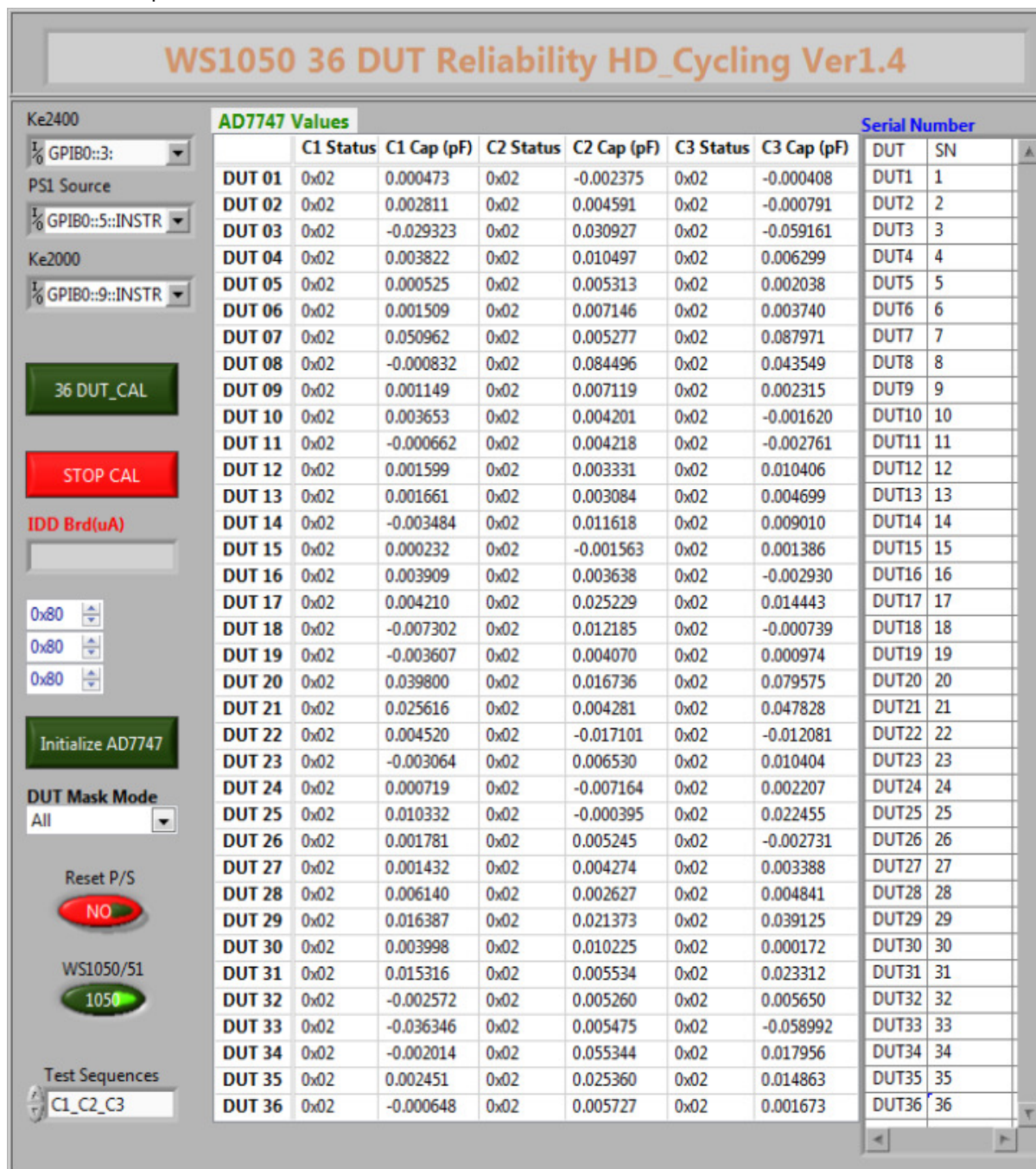


Figure 4

Initialize AD7747

Note: If sockets are not zeros “~0”, click on initialize AD7747 button to initialize the ADI chip, make sure the capacitance values will be less than 1pF (<1pF) for all three banks of 36 DUT, click on 36 DUT\_CAL button to zero out the sockets then click on STOP CAL button to stop the calibration.

- Set-up test condition (Fig. 5): The front panel below was set by default with cycling, DVA OFF, E-CAL OFF, VPI ON, VSA ON, HS (hand shake check) = ON, VDD = 3.7V, cycle speed = 12 KHz, CP stress = 40.25V, CP VPI = 35V.

Figure 5

- | % Duty Cycle |           | Post CMD Delay |  | Command      |  |
|--------------|-----------|----------------|--|--------------|--|
| 25           | No of Cmd | 17u s          |  | 0702013B3B3B |  |
| 2            |           | 54u s          |  | 070201000000 |  |

- | % Duty Cycle | Post Cmd Delay | Command      |
|--------------|----------------|--------------|
| 33           | 18u s          | 0702013B0000 |
| No of Cmd    | 18u s          | 070201003B00 |
| 3            | 18u s          | 07020100003B |

- Cmd To HD 0702013B3B3B

- |   |        |         |                               |
|---|--------|---------|-------------------------------|
| Lot#  | Wafer# | Board#  | TMN DC\CAP Data Log File Path |
| WS1050  | T7-EB  | BRD5    | C:\WS1050 36 DUT Data         |
| File Name   |        |         |                               |
| CYC_WS1050_T7_EB_65C_40V_25DC_EMPTY_BRD5_141017_1   |        |         |                               |
| Comment   |        |         |                               |
| CYC65C40V   |        | Offline | FPGA Mode                     |
| 05/19/2014 -- 12:24:35.853::WSVCAP::APP::Application Started<br>05/19/2014 -- 12:24:37.606::WSVCAP::WSVCAP SHL::WR I2C-REG:0x0A;MASK:<br>0xFFFFFFFFFF;C1 DATA:22:22:22:22:22:22:22:22:22:22:22:22:22:22:22:22:C2 DATA:22:22:22:22:<br>22:22:22:22:22:22:22:22:22:22:22:22:C3 DATA:22:22:22:22:22:22:22:22:22:22:22:22:22:22:22<br>05/19/2014 -- 12:24:37.773::WSVCAP::WSVCAP SHL::WR I2C-ST:0,0,4,1 |        |         |                               |

Note: The file name format will be...

- The test can be set to start immediately by clicking on the START TEST button; alternatively the start date and time can be programmed as shown in Figure 7.

Figure 7

**Note:** The time shall be set at least 30 minutes to wait after loading parts to the board in the oven/chamber. This time is required for the stabilization of the board dwell time at the temperature before to run stress.

- The front panel (Figure 8) displays the capacitance values for every read point.

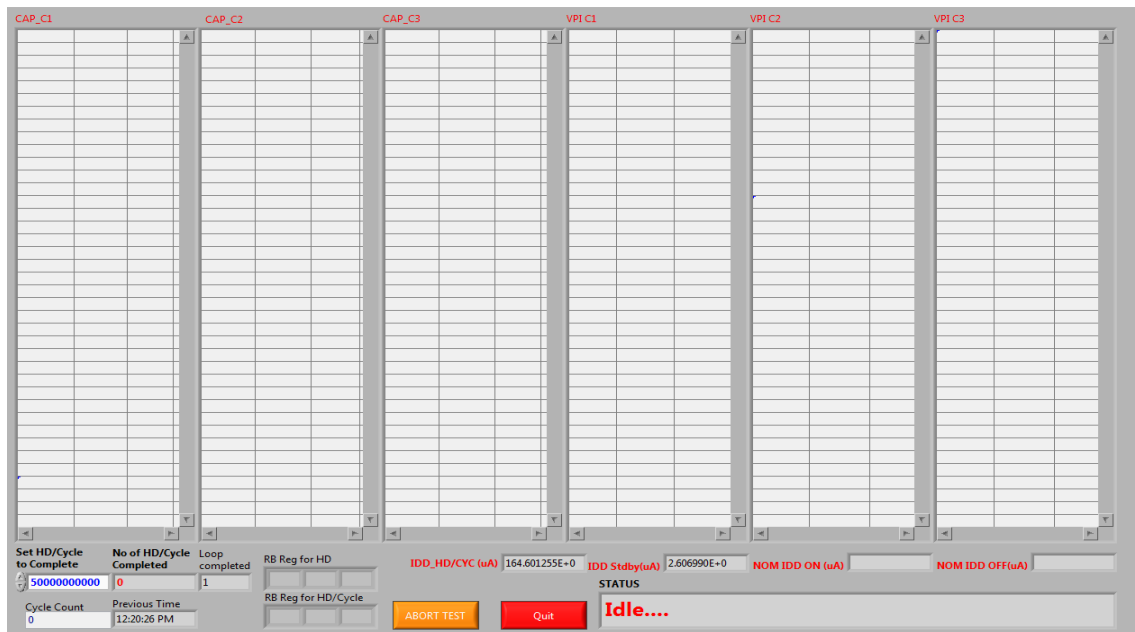
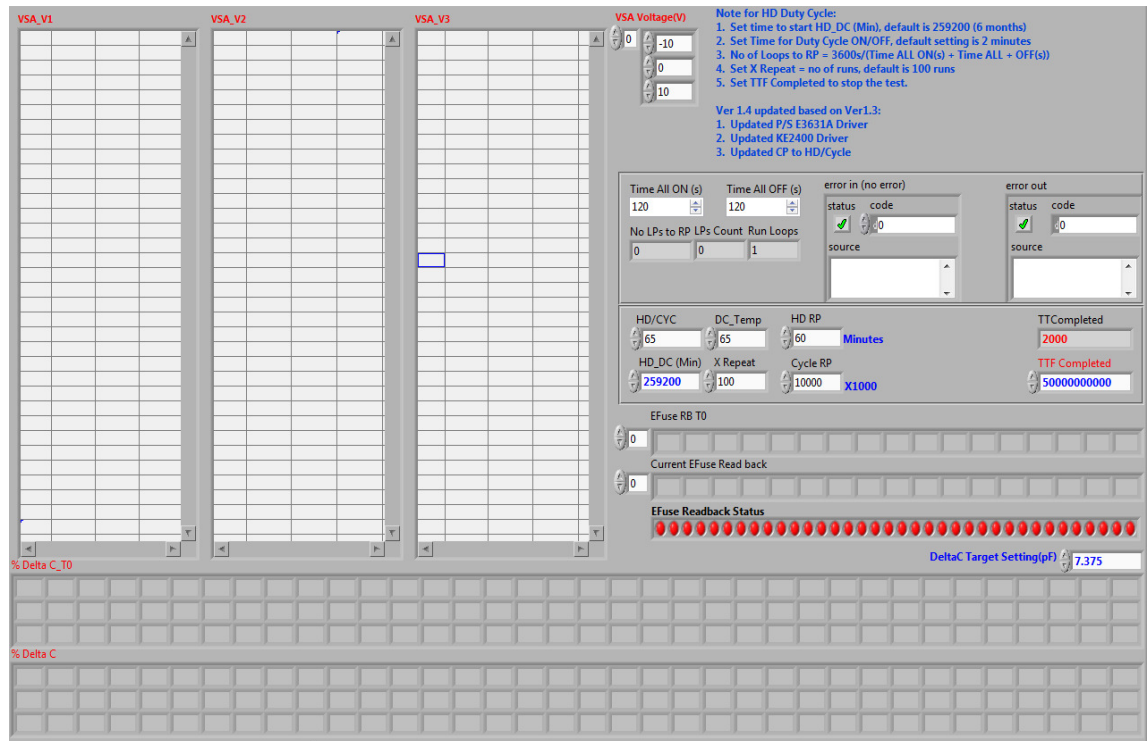


Figure 8

- The front panel (Figure 9) displays VSA, HS check, EFUSE, % Delta CAP for every read point



**Figure 9**

- Figure 10 shows the output results, so that changes in CMIN can be monitored during stress.

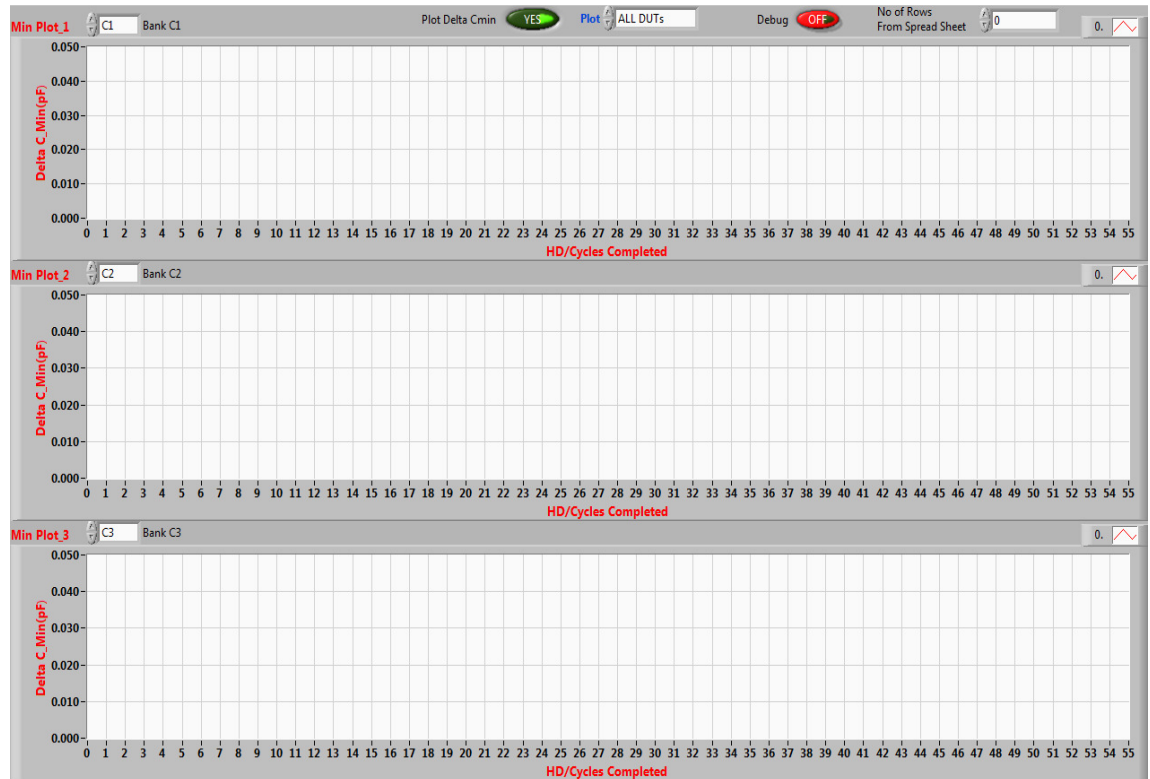


Figure 10

- Stop stress or abort the test: The test can be aborted immediately by click on the ABORT TEST button (Figure 11) or enter the number that will be set to complete the test (5 billion cycles is set by default).

<b>Set HD/Cycle to Complete</b>	<b>No of HD/Cycle Completed</b>	<b>Loop completed</b>	<b>RB Reg for HD</b>	<b>IDD_HD/CYC (uA)</b>	164.601255E+0
5000000000	0	1			
<b>Cycle Count</b>	<b>Previous Time</b>		<b>RB Reg for HD/Cycle</b>	<b>ABORT TEST</b>	<b>Quit</b>
0	12:20:26 PM				

<b>HD/CYC</b>	<b>DC_Temp</b>	<b>HD RP</b>	<b>TTCompleted</b>
65	65	60 Minutes	2000
<b>HD_DC (Min)</b>	<b>X Repeat</b>	<b>Cycle RP</b>	<b>TTF Completed</b>
259200	100	10000 X1000	5000000000

Figure 11



## 8. REVISION HISTORY

Rev	Description	Editor	Date
A	Initial Release	M. Johnson	12-Aug 2015