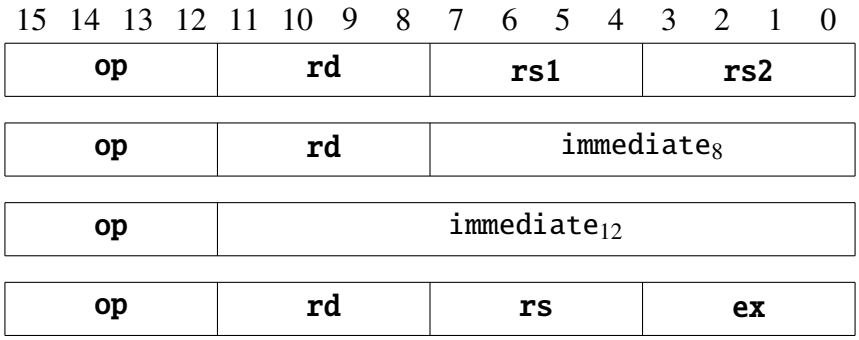
520.225 16 RISC Bit Microprocessor Specifications

Registers: 15 general purpose 16 bit programmer accessible registers **r1** through **r15**, plus constant register **r0** (fixed at zero). The program counter **pc** is an additional register which is not directly accessible, except via branch and jump instructions.

Instruction formats: Four instruction formats:

- A three register format with a 4 bit opcode **op**, a destination register **rd**, and two source registers **rs1** and **rs2**.
- A one register immediate format with a 4 bit opcode **op**, a destination register **rd** and an 8 bit immediate which may be signed or unsigned depending on the instruction.
- A zero register (implied) immediate format with a 4 bit opcode **op** and a 12 bit signed immediate.
- A two register format with a 4 bit opcode **op**, a destination register **rd**, a source register **rs** and a 4 bit opcode extension **ex** (substituting for **rs2**).

The layout of the instruction formats are as follows:



The instruction encodings are shown on the next page.

The three, one and zero register instruction encoding are as follows:

op	Mnemonic	Description
0000	LI	**rd** $\leftarrow$ sext(immediate$_8$)
0001	NOR	**rd** $\leftarrow \neg$**rs1** $\wedge \neg$**rs2**
0010	CLRB	**rd** $\leftarrow$ **rs1** $\wedge \neg$**rs2**
0011	LSL	**rd** $\leftarrow$ **rs1** $<<$ **rs2**
0100	LSR	**rd** $\leftarrow$ **rs1** $>>$ **rs2**
0101	ASR	**rd** $\leftarrow$ sext(**rs1** $>>$ **rs2**)
0110	XOR	**rd** $\leftarrow$ **rs1** $\oplus$ **rs2**
0111	NAND	**rd** $\leftarrow \neg$**rs1** $\vee \neg$**rs2**
1000	AND	**rd** $\leftarrow$ **rs1** $\wedge$ **rs2**
1001	XNOR	**rd** $\leftarrow$ **rs1** $\odot$ **rs2**
1010	LUI	**rd**$(15:8) \leftarrow$ immediate$_8$ $<< 8$
1011	BRA	**pc** $\leftarrow$ **pc** + sext(immediate$_{12}$)
1100	ADD	**rd** $\leftarrow$ **rs1** + **rs2**
1101	SUB	**rd** $\leftarrow$ **rs1** $-$ **rs2**
1110	OR	**rd** $\leftarrow$ **rs1** $\vee$ **rs2**
1111		Two register format instruction

The two register instruction encoding (**op**=1111) are as follows:

ex	Mnemonic	Description
0000	SW	M_{16}[**rs**] $\leftarrow$ **rd**
0001	SB	M_8[**rs**] $\leftarrow$ **rd**$(7:0)$
0010	LW	**rd** $\leftarrow$ M_{16}[**rs**]
0011	LBU	**rd**$(7:0) \leftarrow M_8$[**rs**] **rd**$(15:8) \leftarrow$ 00000000
0100	LBS	**rd** $\leftarrow$ sext(M_8[**rs**])
0101	BZ	**pc** $\leftarrow$ **pc** + **rs** if **rd** zero
0110	JZ	**pc** $\leftarrow$ **rs** if **rd** zero
0111	JAL	**pc** $\leftarrow$ **rs**, **rd** $\leftarrow$ **pc** + 1
1000	NEG	**rd** $\leftarrow -$**rs**
1001	COM	**rd** $\leftarrow \neg$**rs**
1010	SLE	**rd** $\leftarrow$ 1 if **rs** $\leq$ 0, **rd** $\leftarrow$ 0 otherwise
1011	SLT	**rd** $\leftarrow$ 1 if **rs** $<$ 0, **rd** $\leftarrow$ 0 otherwise
1100	SGE	**rd** $\leftarrow$ 1 if **rs** $\geq$ 0, **rd** $\leftarrow$ 0 otherwise
1101	SGT	**rd** $\leftarrow$ 1 if **rs** $>$ 0, **rd** $\leftarrow$ 0 otherwise
1110	SNZ	**rd** $\leftarrow$ 1 if **rs** $\neq$ 0, **rd** $\leftarrow$ 0 otherwise
1111	SZ	**rd** $\leftarrow$ 1 if **rs** $=$ 0, **rd** $\leftarrow$ 0 otherwise