Decoder3to8 Project Status (11/07/2014 - 21:55:30)			
Project File:	DECODER3_to_8.xise	**Parser Errors:**	No Errors
Module Name:	Decoder3to8	**Implementation State:**	Synthesized
Target Device:	xc6slx4-3tqg144	• **Errors:**	No Errors
Product Version:	ISE 14.5	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	8	2400	0%
Number of fully used LUT-FF pairs	0	8	0%
Number of bonded IOBs	11	102	10%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Nov 7 21:55:28 2014	0	0	1 Info (1 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Current	Fri Nov 7 23:34:19 2014

Date Generated: 11/07/2014 - 23:45:16