serial_ip_serial_or_parallel_out_shift_reg Project Status (12/08/2014 - 10:52:04)			
Project File:	Serial_In_Serial_Or_Parallel_Out_8Bit.xise	**Parser Errors:**	No Errors
Module Name:	serial_ip_serial_or_parallel_out_shift_reg	**Implementation State:**	Synthesized
Target Device:	xc6slx4-3tqg144	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	9	4800	0%
Number of Slice LUTs	10	2400	0%
Number of fully used LUT-FF pairs	9	10	90%
Number of bonded IOBs	13	102	12%
Number of BUFG/BUFGCTRL/BUFHCEs	2	16	12%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Dec 8 11:28:26 2014	0	0	7 Infos (7 new)
Translation Report	Out of Date	Mon Dec 8 10:06:56 2014	0	0	0
Map Report	Out of Date	Mon Dec 8 10:07:15 2014	0	0	6 Infos (6 new)
Place and Route Report	Out of Date	Mon Dec 8 10:07:23 2014	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Out of Date	Mon Dec 8 10:07:28 2014			
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Current	Mon Dec 8 11:51:41 2014
Post-Map Static Timing Report	Out of Date	Mon Dec 8 10:09:22 2014

Date Generated: 12/09/2014 - 17:17:50