sine_gen Project Status			
Project File:	sine.xise	**Parser Errors:**	No Errors
Module Name:	sine_gen	**Implementation State:**	Translated
Target Device:	xc3s200-5tq144	**• Errors:**	X 1 Error (0 new)
Product Version:	ISE 14.5	**• Warnings:**	1 Warning (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	24	1920	1%
Number of Slice Flip Flops	21	3840	0%
Number of 4 input LUTs	41	3840	1%
Number of bonded IOBs	17	97	17%
Number of BRAMs	1	12	8%
Number of GCLKs	1	8	12%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Feb 23 14:07:37 2015	0	1 Warning (0 new)	2 Infos (0 new)
Translation Report	Current	Mon Feb 23 14:07:44 2015	X 1 Error (0 new)	0	0
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Mon Feb 23 14:27:21 2015	

Date Generated: 02/23/2015 - 14:28:07