Dlatch_1bit Project Status (11/17/2014 - 14:04:00)			
Project File:	Dlatch_1bit.xise	**Parser Errors:**	No Errors
Module Name:	Dlatch_1bit	**Implementation State:**	Synthesized
Target Device:	xc6slx4-3tqg144	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	1 Warning (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of bonded IOBs	3	102	2%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Nov 17 14:03:59 2014	0	1 Warning (0 new)	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Current	Mon Nov 17 14:07:52 2014

Date Generated: 11/17/2014 - 14:07:53