ShiftRegister_SIPO Project Status (11/10/2014 - 13:36:54)			
Project File:	ShiftRegister_SIPO.xise	**Parser Errors:**	No Errors
Module Name:	ShiftRegister_SIPO	**Implementation State:**	Synthesized
Target Device:	xc6slx4-3tqg144	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	7	4800	0%
Number of Slice LUTs	1	2400	0%
Number of fully used LUT-FF pairs	0	8	0%
Number of bonded IOBs	10	102	9%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Nov 10 13:36:53 2014	0	0	0
Translation Report	Out of Date	Mon Nov 10 07:33:27 2014	0	0	0
Map Report	Out of Date	Mon Nov 10 07:33:34 2014	X 1 Error (1 new)	0	0
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	Mon Nov 10 13:36:06 2014

Date Generated: 11/10/2014 - 13:37:07