

UpDownCounter_8bit Project Status (11/04/2014 - 14:52:48)			
Project File:	UpDownCounter_8bit.xise	Parser Errors:	No Errors
Module Name:	UpDownCounter_8bit	Implementation State:	Synthesized
Target Device:	xc6slx4-3tqg144	• Errors:	No Errors
Product Version:	ISE 14.5	• Warnings:	2 Warnings (2 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)				[-]
Logic Utilization	Used	Available	Utilization	
Number of Slice Registers	8	4800	0%	
Number of Slice LUTs	8	2400	0%	
Number of fully used LUT-FF pairs	0	16	0%	
Number of bonded IOBs	11	102	10%	
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%	

Detailed Reports						[-]
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Tue Nov 4 14:52:47 2014	0	2 Warnings (2 new)	0	
Translation Report						
Map Report						
Place and Route Report						
Power Report						
Post-PAR Static Timing Report						
Bitgen Report						

Secondary Reports			[-]
Report Name	Status	Generated	
ISIM Simulator Log	Current	Tue Nov 4 15:01:23 2014	

Date Generated: 11/04/2014 - 15:07:38