topmodule Project Status (02/14/2015 - 14:37:22)			
Project File:	square_wave_gen.xise	**Parser Errors:**	No Errors
Module Name:	topmodule	**Implementation State:**	Synthesized
Target Device:	xc3s200-5tq144	• **Errors:**	No Errors
Product Version:	ISE 14.5	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	55	1920	2%
Number of Slice Flip Flops	33	3840	0%
Number of 4 input LUTs	88	3840	2%
Number of bonded IOBs	6	97	6%
Number of GCLKs	2	8	25%
Number of DCMs	1	4	25%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Feb 14 14:37:21 2015	0	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Sat Feb 14 14:37:12 2015	

Date Generated: 02/14/2015 - 14:37:22