clock_generator Project Status (12/06/2014 - 22:09:45)			
Project File:	Clock_Generator_Final.xise	**Parser Errors:**	No Errors
Module Name:	clock_generator	**Implementation State:**	Synthesized
Target Device:	xc6slx4-3tqg144	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	6 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	5	4800	0%
Number of Slice LUTs	7	2400	0%
Number of fully used LUT-FF pairs	0	12	0%
Number of bonded IOBs	5	102	4%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Dec 6 22:09:43 2014	0	6 Warnings (0 new)	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	Sat Dec 6 17:15:39 2014

Date Generated: 12/06/2014 - 22:09:45