Dff_8bit_syncroclr Project Status (11/03/2014 - 18:44:09)			
Project File:	Dff_8bit_fallingedge_synchroclr.xise	**Parser Errors:**	No Errors
Module Name:	Dff_8bit_synchroclr	**Implementation State:**	Synthesized
Target Device:	xc6slx4-3tqg144	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	2	2400	0%
Number of fully used LUT-FF pairs	0	2	0%
Number of bonded IOBs	18	102	17%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Nov 3 18:44:07 2014	0	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**

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