top Project Status (03/11/2015 - 14:57:46)			
Project File:	vga.xise	**Parser Errors:**	No Errors
Module Name:	top	**Implementation State:**	Programming File Generated
Target Device:	xc3s200-5tq144	• **Errors:**	No Errors
Product Version:	ISE 14.5	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	33	3,840	1%	
Number of 4 input LUTs	26	3,840	1%	
Number of occupied Slices	40	1,920	2%	
Number of Slices containing only related logic	40	40	100%	
Number of Slices containing unrelated logic	0	40	0%	
Total Number of 4 input LUTs	74	3,840	1%	
Number used as logic	26			
Number used as a route-thru	48			
Number of bonded IOBs	3	97	3%	
Number of BUFGMUXs	2	8	25%	
Number of DCMs	1	4	25%	
Average Fanout of Non-Clock Nets	2.29			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Mar 11 15:16:12 2015	0	0	0
Translation Report	Current	Wed Mar 11 15:16:29 2015	0	0	0
Map Report	Current	Wed Mar 11 15:16:32 2015	0	0	3 Infos (0 new)
Place and Route Report	Current	Wed Mar 11 15:16:36 2015	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed Mar 11 15:16:39 2015	0	0	6 Infos (0 new)
Bitgen Report	Current	Wed Mar 11 15:16:43 2015	0	0	2 Infos (0 new)

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Current	Wed Mar 11 15:18:51 2015	
Post-Synthesis Simulation Model Report	Current	Wed Mar 11 15:16:20 2015	

Post-Place and Route Simulation Model Report	Current	Wed Mar 11 15:18:45 2015
WebTalk Report	Current	Wed Mar 11 15:16:43 2015
WebTalk Log File	Current	Wed Mar 11 15:16:44 2015

Date Generated: 03/11/2015 - 15:22:44