

Dff_8bit_AsynchClr Project Status (11/11/2014 - 15:15:11)			
Project File:	Dff_8bit_AsynchClr.xise	Parser Errors:	No Errors
Module Name:	Dff_8bit_AsynchClr	Implementation State:	Synthesized
Target Device:	xc6slx4-3tqg144	• Errors:	No Errors
Product Version:	ISE 14.5	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	Used	Available	Utilization
Number of bonded IOBs	18	102	17%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Detailed Reports [-]					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Tue Nov 11 15:15:09 2014	0	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	Status	Generated
ISIM Simulator Log	Out of Date	Tue Nov 11 07:59:50 2014

Date Generated: 11/11/2014 - 15:15:11