CS M51A and EE M16 Summer 2016 Section 1

Logic Design of Digital Systems

Dr. Yutao He

Verilog Lab #2 - Design of Combinational Systems

Due: July 31st, 2016

(1) Name: _____
Last First

Student ID: _____

Signature: _____

(2) Name: _____
Last First

Student ID: _____

Signature: _____

Date: _____

Result	
Correctness	
Creativity	
Report	
Total Score	

Verilog Lab #2 Project Requirement

Dr. Yutao He

Due: 7/31/2016

1 Objectives

The second project is to build a combinational circuit for a real-world application by applying systematically the concepts and techniques covered in the class, and walking through the whole cycle of designing digital systems, from the high-level specification to the final implementation. It basically consists of two steps:(1) the pencil-and-paper design, and (2) the implementation with Verilog by means of the CAD software Vivado.

2 Project Description

2.1 The High-Level Specification

The circuit to be built is a *BCD-to-seven-segment display decoder* that is used extensively to drive LED (Light-Emitting Diode)-based display devices such as billboards.

The structure of a seven-segment LED device and its interface with the decoder to be designed are shown in Figure 1. It is easily seen that any decimal number from zero to nine can be displayed with this device simply by turning some segments **on** (shaded), while leaving others **off** (unshaded).

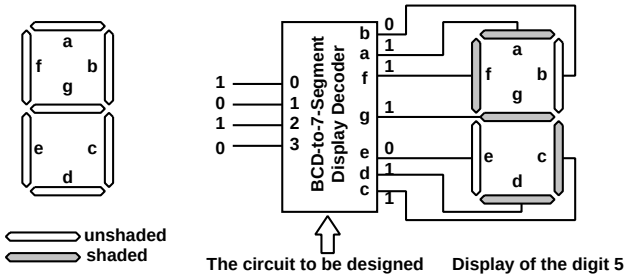

Figure 1: The Structure of a Seven-Segment Display Device

The complete display patterns for one-digit decimal numbers are specified in Table 1.

Decimal No.	a	b	c	d	e	f	g
0	ON	ON	ON	ON	ON	ON	OFF
1	OFF	ON	ON	OFF	OFF	OFF	OFF
2	ON	ON	OFF	ON	ON	OFF	ON
3	ON	ON	ON	ON	OFF	OFF	ON
4	OFF	ON	ON	OFF	OFF	ON	ON
5	ON	OFF	ON	ON	OFF	ON	ON
6	ON	OFF	ON	ON	ON	ON	ON
7	ON	ON	ON	OFF	OFF	OFF	OFF
8	ON	ON	ON	ON	ON	ON	ON
9	ON	ON	ON	ON	OFF	ON	ON

Table 1: The Seven-Segment Display Logic Specification

Given the above specification, in this project you are to build a circuit which takes a decimal digit, decodes it according to the specified logic, and generates the corresponding outputs. In addition, your circuit must also meet the following requirements:

1. **Encoding scheme of inputs**: You must use the BCD (Binary-Coded-Decimal) code to encode one decimal digit as specified in Table 2:

2. **Encoding scheme of outputs**: The on/off encoding scheme of outputs is specified in Table 3.

3. **Implementation**: The system must be implemented with a *two-level NOR-NOR network*.

4. **Cost**: Let us define the *cost* of the system as the number of NOR gates in the circuit. The system must be designed with minimal cost.

Extra Credits

Extra credits will be given to those of you who will take your design and implement it successfully on the Mojo FPGA (Field Programmable Gate Array) development board.

Decimal No.	BCD Code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Table 2: The Input Encoding Scheme

Segment State	Binary Code
ON	1
OFF	0

Table 3: The Output Encoding Scheme

2.2 Project Policy and Team Sign-Up

To reduce your workload while encouraging effective and responsible teamwork, you MUST work in **groups of two** on this project. Any one of your current classmates in CS M51A and EE M16 Section 1 can be your partner. Each member of your group should assume reasonable quota of the load. You must sign up on-line by midnight July 24th, 2016 at *http://bit.ly/csm51aprojteam*.

3 Report Outline

You are required to submit only one report that provides complete documentation of your project including the detailed design worksheets. As in all technical writing, its purpose is to communicate your work with your colleagues in an efficient and professional way so that your design can be continuously upgraded and maintained even if you are no longer around. As a result, the report should be clear, concise, and complete and should contain the following parts:

(1) *Title Page*

It is provided and you just need to fill in your information in the blanks.

(2) *Abstract*

This is the brief high-level description of the project.

(3) *The Switching Functions of the Circuit*

It is part of the design work for you to obtain the binary-level specification for the function of the circuit in the form of switching expressions and the schematic. This section should present both minimal switching expressions in NOR-NOR form and the schematic of the circuit.

(4) *The Verilog Code of the Circuit*

The Verilog file (with extension .v) you write is the implementation of the circuit. You should include its printout in your report with your names and student IDs on it.

(5) *The Simulation Result*

You have to demonstrate that your implementation behaves as specified by showing the correct simulation result. In particular, the result (in the forms of Timing Diagram) should include the displays for a complete set of decimal numbers (from zero to nine). Include in your report the Timing Diagram wth enough information on it so that one of your colleagues who does not know anything about your project could understand easily which function you are trying to implement by just reading the Timing Diagram.

(6) *The Design Review*

This section summarizes your experiences and lessons throughout the project. It should be no more than one page and may include topics such as what you have learned, problem encountered during the implementation and the solutions you came up with, the approach you used, the most important aspects of the project for you, where you spent most of your time, and suggestions you would like to make.

(8) *Appendix - The Detailed Design Worksheet*

This section must include the complete set of worksheets from the pencil-and-paper design. Please scan and combine them with other

parts of your report. Hand-written form is perfectly fine yet it must include:

8.1 inputs and outputs of the system.

8.2 encoding schemes of inputs and output.

8.3 truth tables.

8.4 minimization procedure by means of either K-map or Quine-McCluskey method.

8.5 transformation procedure.

8.6 final minimal expressions of the output functions in terms of both switching expressions and the schematic.

4 Project Submission

You should submit one zipped file named with "xx.zip" via the on-line submission link that will be avalable by 7/30. The zipped file should consist of three separate files:

1. The pdf file of your report. It must be named as "xx.pdf" where xx is your Student ID, that is, your report should be called *xx.pdf*;
2. The Verilog file of your circuit implementation. It should be named as *csm51a_proj2.v*.
3. The testbench file. It should be named as *csm51a_proj2_tb.v*.

5 Project Deadline

The report is due by midnight (11:59:59pm) on July 31st (Sunday), 2016. The deadline must be observed strictly and late submissions will be subject to penalty.