

# Axi reference guide xilinx

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**What is AXI in FPGA?** The Advanced eXtensible Interface (AXI) is designed for FPGAs based on AMBA as a protocol for communication between blocks of IP. Here are some of the important features of an AXI interface: It supports burst transactions with only start address issued. There are different phases for the data and addresses.

**What is the use of AXI protocol?** AXI is a burst-based protocol, meaning that there may be multiple data transfers (or beats) for a single request. This makes it useful in the cases where it is necessary to transfer large amount of data from or to a specific pattern of addresses.

**What is the full form of AMBA AXI?** Advanced eXtensible Interface (AXI) AXI, the third generation of AMBA interface defined in the AMBA 3 specification, is targeted at high performance, high clock frequency system designs and includes features that make it suitable for high speed sub-micrometer interconnect: separate address/control and data phases.

**What is AXI memory?** The AXI Memory Initialization core autonomously writes an initial value to all specified address locations after power-up and following each soft reset. This prevents spurious ECC errors that can occur when accessing an uninitialized memory.

### **How to use AXI?**

**Why use AXI?** The AXI protocol includes transaction identifiers, and there is no restriction on the completion of transactions with different ID values. This means that a single physical port can support out-of-order transactions by acting as several logical ports, each of which handles its transactions in order.

**Why is AXI better than ahb?** AXI provides several advanced features like burst transactions, separate read and write channels, and support for multiple outstanding transactions. AHB also provides some of these features, but not all. APB is a simpler protocol and does not have these features.

**Does PCIe use AXI?** The AXI PCIe® Gen 3 Subsystem core provides an interface between the AXI4 interface and the Gen 3 PCI Express (PCIe) silicon hard core. The AXI4 PCIe sub-system provides full bridge functionality between the AXI4 architecture and the PCIe network.

**What is QoS in AXI?** The AMBA 4 AXI protocol brings in quality of service (QoS) signaling on the AXI bus to address the challenges imposed by bandwidth and latency requirements of various IP in a SoC.

**Is AXI byte addressable?** The AXI address from the AXI master is a TRUE byte address. The AXI shim converts the address from the AXI master to the memory based on AXI SIZE and memory data width. The LSBs of the AXI byte address are masked to 0, depending on the data width of the memory array.

**What is deadlock in AXI?** The deadlocks may occur in the AXI protocol due to how the AXI supports out-of-order transactions. We take the example in Figure 2.2 again now, slaves 1 and 2 are both assigned tasks via ID 1 and 2, and T1 must be serviced before T3, T2 must be serviced before T4.

**What is the frequency of AXI?** The recommended frequency for the AXI interface is up to 200 MHz. For the maximum frequency numbers achieved on the SelectIO PHY interface, see Table: Hardware Testing Configuration with a SelectIO FPGA interface in Verification, Compliance, and Interoperability .

**Is AXI synchronous?** "The AXI protocol uses a single active LOW reset signal, ARESETn. The reset signal can be asserted asynchronously, but de-assertion must be synchronous with a rising edge of ACLK.

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## **What does AXI stand for Xilinx?**

**Is AXI open source?** The UVVM AXI4-lite has also been upgraded to allow independent channels. This means UVVM now provides free and open source VHDL verification models for AXI4, AXI4-lite and AXI4-stream. UVVM provides a lot of different VHDL verification components and Bus functional models, - all for free and open source.

**How to verify AXI protocol?** In this AMBA AXI verification the properties to be verified are i)System connectivity during read and write cycle, ii)Transaction routing and iii)finally the Data integrity. In the system connectivity checking test, the system integration is monitored by the corresponding acknowledgement signals.

**What is AXI interconnect?** The AXI Interconnect IP connects one or more AXI memory-mapped Master devices to one or more memory-mapped Slave devices.

**Why is AXI faster than ahb?** AXI has completely independent channels for read/write, which enables full duplex mode of data transportation. That is to say read and writes can take place simultaneously, giving 2x boost over AHB in any circumstances.

**What is the basics of AXI?** In its most basic configuration, the AXI protocol connects and facilitates communication between one master and one slave device. As expected, the master initiates and drives data requests, while the slave responds accordingly.

**What is AXI memory-mapped?** The memory-mapped system is a common technique to access I/O and memory in processor systems. AXI protocol is a memory-mapped communication scheme among IPs in an embedded system. AXI protocol divides IP ports into two groups: Masters and Slaves.

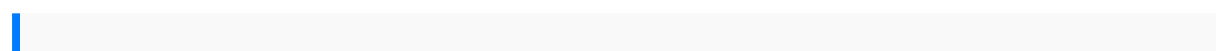
**What is the function of AXI machine?** AXI is able to find faults such as opens, shorts, insufficient solder, excessive solder, missing electrical parts, and mis-aligned components. Defects are detected and repaired within short debug time.

**What is the difference between PCI and AXI?** While AXI protocol supports transmission of parallel Read and Write Requests, and Read Completion on the

same direction, PCI Express protocol supports transmission of only a single type of packet in any given moment. The choice of what packet to transmit has direct impact on overall system performance.

**What is the AXI GPIO?** The AXI GPIO provides a general purpose input/output interface to the AXI (Advanced eXtensible Interface) interface. This 32-bit soft IP core is designed to interface with the AXI4-Lite interface.

**What is the difference between AHB and AXI?** AXI is suitable for high-performance applications like video processing, networking, and graphics. AHB is used for mid-range applications like microcontrollers.



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