



CORES TG – July 23 2020

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Outline

- CV32E40P status
- CV32E40P Verification Plan reviews
- CV32E20 – discussion start
- CVA6 feature & parameter discussion – part 1
- CV64A/CV32A status

CV32E40P issues (1/2)

- Open issue have been labeled
- Label overview: <https://github.com/openhwgroup/cv32e40p/labels>
- Issue template

Bug For bugs in the RTL, Documentation, Verification environment or Tool and Build system.	Open
Task For any task except bug fixes.	Open
Question For general questions.	Open
Enhancement For feature requests and enhancements.	Open

- Filtering

https://github.com/openhwgroup/cv32e40p/issues filter	#	Comment
is:issue is:open	57	Open
is:issue is:open -label:status:resolved	48	Non-closed
is:issue is:open -label:status:resolved label:component:rtl label:type:bug -label:waived:cv32e40p	16	RTL bugs

CV32E40P issues (2/2)

- 16 RTL bugs
 - label:param:fpu 8
 - label:param:pulp_xpulp 7
 - Other 1
- Other main issue category
 - Manifests, FuseSoc
- Asking for contributors to fix these 8 FPU, 7 xPULP, and 1 fence.i issues
 - Send email to Davide Schiavone davide@openhwgroup.org within 2 weeks, otherwise we need to volunteer you 😊

Code not running with fpnew in verilator	Component:RTL	Good First Issue	PARAM:FPU	Type:Bug
#308 opened on Apr 17 by mmatzev				
Incorrect F Extension Result Calculation - FADD, FSUB, FMUL, FMADD, FNMADD, FMSUB, FNMSUB	Component:RTL		PARAM:FPU	Type:Bug
#175 opened on Sep 30, 2019 by shetalani				
Incorrect F Extension Result Calculation - Dynamic Rounding Mode	Component:RTL		PARAM:FPU	Type:Bug
#174 opened on Sep 30, 2019 by shetalani				
Illegal Instruction Exception not Raised - FS Field	Component:RTL	Good First Issue	PARAM:FPU	Type:Bug
#170 opened on Sep 27, 2019 by shetalani				
Illegal Instruction Exception not Raised - Dynamic Rounding Mode	Component:RTL		PARAM:FPU	Type:Bug
#169 opened on Sep 27, 2019 by shetalani				
Decoder bug for casting instruction FP to INT	Component:RTL		PARAM:FPU	Type:Bug
#83 opened on Jun 25, 2019 by OTTG				
Don't support FCVT.WU.S and FCVT.S.WU?	Component:RTL		PARAM:FPU	Type:Bug
#65 opened on Mar 22, 2019 by hyf6661669				
FP to Int / Int to FP conversions always signed	Component:RTL		PARAM:FPU	Type:Bug
#48 opened on Sep 21, 2018 by stmach				
pv.cplxmul.(r/i)(/,div2/div4/div8) incorrect functionality	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#407 opened 7 days ago by DavidM-EMUS				
Re-introduce Hardware Loop functionality	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#406 opened 7 days ago by Silabs-ArjanB				
pv.cplxconj decoding and tracing	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#372 opened on Jun 17 by Silabs-ArjanB				
Wrong (none) bypass usage by pv.cplxconj	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#363 opened on Jun 11 by Silabs-ArjanB				
Prefetch buffer issue when IRQ arrived on last instruction of the HW loop body	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#197 opened on Nov 13, 2019 by yaronbe1				
HW Loop Rd after Wr error	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#189 opened on Nov 3, 2019 by yaronbe1				
Change the address of some custom CSRs to be in the range reserved for such CSRs	Component:RTL		PARAM:PULP_XPULP	Type:Bug
#142 opened on Sep 4, 2019 by Silabs-ArjanB				
tracer out of order for half-word aligned fence.i	Component:RTL		Type:Bug	
#329 opened on May 8 by eroom1966				

CV32E40P Verification Plan reviews



- Volunteers?
- Deadline July 31

Directory	Vplan	Status	Reviewer(s)
Base Instruction Set	Counters	Needs update	Paul Zavalney (Silabs)
	RV32I	Ready for Review	
	RV32C	Ready for Review	Arjan Bink (Silabs)
	RV32M	Ready for Review	Arjan Bink (Silabs)
	RV32Z	Ready for Review	Arjan Bink (Silabs)
	Exceptions	Ready for Review	John Martin (EM Micro)
custom_circuitry	prefetch unit	Needs capture	
debug-trace	Debug	Reviewed	Paul Zavalney (Silabs), Vitor Sato (NXP)
	External Debugger	Out of scope	
interrupts	none	Needs capture	
privileged_spec	CSRs	Needs capture	
	Privileged Instructions	Needs capture	
	Modes	Out of scope	
physical_interfaces	Sleep Unit	Needs capture	
	Configuration and Control	Needs capture	
	APU	Out of scope	
	OBI	Ready for Review	Arjan Bink (Silabs)
xpulp_instruction_extensions	bit_manipulations	Not certain	
	general_alu	Not certain	
	Immediate-branching	Not certain	
	hwloop	Not certain	
	packed-simd	Not certain	
	Pulp-cluster	Not certain	
	Xpulp-postinc-loadstore	Not certain	

CV32E20 – Not on roadmap yet - initial

- Proposal to kick start discussion
- Goal
 - Low cost RISC-V
 - Embedded Controller class
- Fork of Ibex and (mostly) simplify
- CV32E20 key features
 - RV32[I|E][M]C[B]
 - 2-stage pipeline
 - M-mode
 - PMP
 - CLINT or CLIC
 - OBI
- Compared to Ibex
 - Remove
 - User mode (TBD)
 - Cache
 - Security features
 - NMI
 - Branch prediction
 - Configurable latency multiplier
 - Branch prediction
 - Add
 - CLIC
 - Fence.i interface
 - Interruptable DIV/DIVU/REM/REMU
- To be discussed
 - Atomics
 - User mode

CVA6 Parameters

- RV64(32)GC - (IMAFD)Cxsmallfloat
- AXI5 interface
- 64/32 XLEN
- SV32/SV39 VM
- PMPs
- PMAs (non-idempotent, cacheable, executable)
- Number of Scoreboard entries
- ASID width
- Number of commit ports
- RVF/RVD on-off
- Write-back/write-through cache
- CLINT/PLIC spec
 - <https://github.com/pulp-platform/clint>
 - https://github.com/pulp-platform/rv_plic
- Dromjao Co-simulation
- Notes
 - FPU not yet supported for XLEN 32
 - MMU not yet supported for XLEN 32

Critical Tasks for CVA6

- Move documentation to RTD and enhance
- Fix CI!
- Maintenance PRs/Issues – Who?
- Move to fusesoc
 - I expect quite some effort due to the missing manifest files in the dependencies
 - Maybe a fusesoc/Bender bridge?
 - Allocate engineering resources?

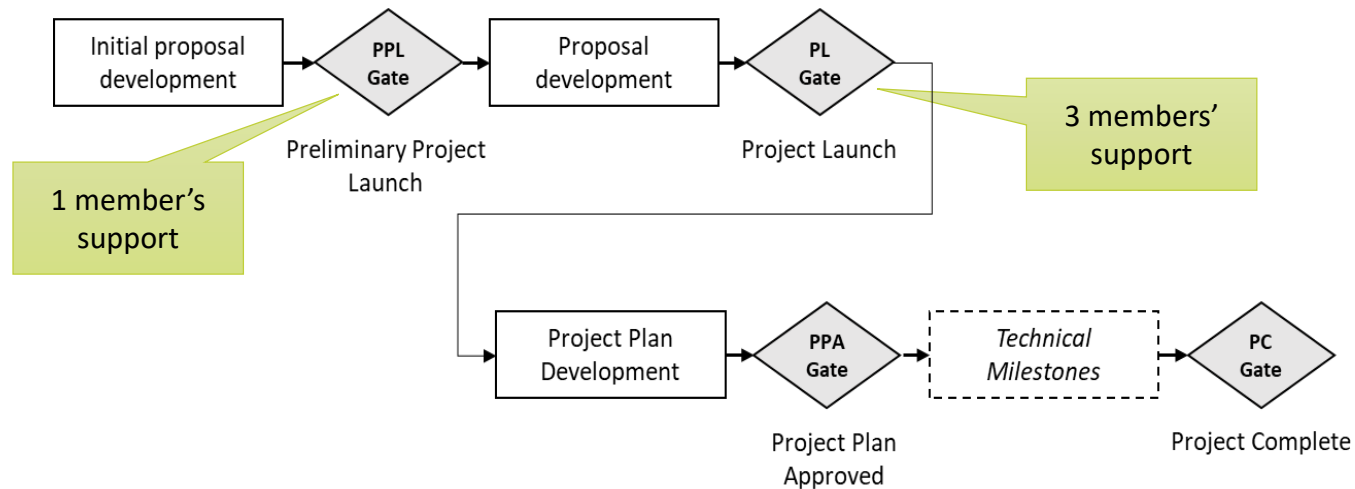
SDK/Linux image?

Future:

- Super-scalar/OoO?
- Cache coherence

CV32A6

- Pull request by Thales of the 32-bit only version of CV64A6
 - MMU and FPU not yet compatible
- CVA6 projects will have to be vetted through the new project process (not yet ratified) defined by the Technical WG.
 - Need to refine the development plan to pass the various gates (ex: tools, resources, milestones, contributions...)



Thank you!