NXP CORE PROPOSAL: A CORE-V CV32E2

RISC-V

OPENHW GROUP™ PROVEN PROCESSOR IP and CORE-V™

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NXP | SECURE CONNECTIONS FOR A SMARTER WORLD

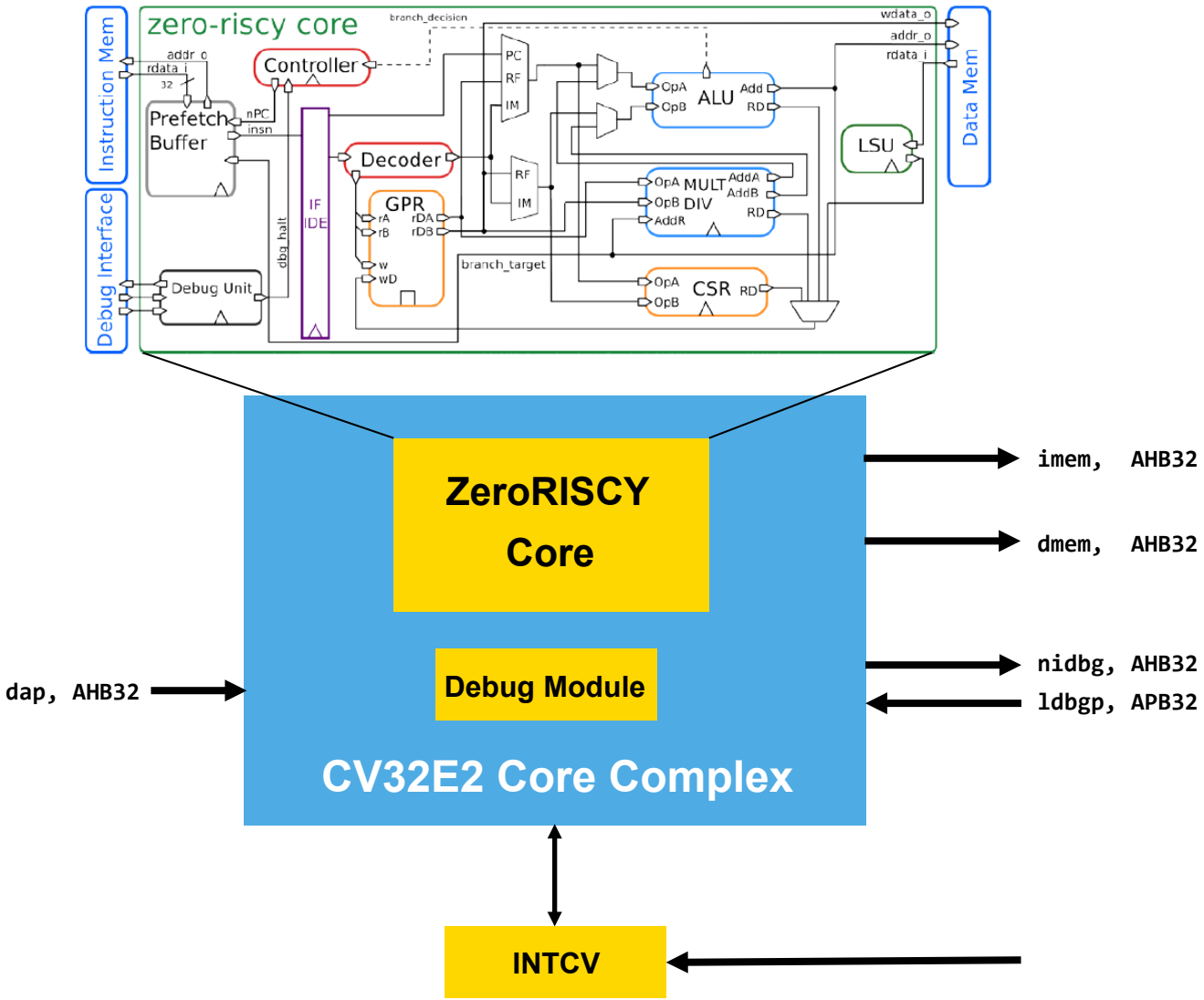
BASIC PROPOSAL

- NXP is considering “contribution” of our productized ETH-Zurich PULPino ZeroRISCY core
  - Current status is this proposal is being considered, but ***nothing has been approved or committed***
  - Trying to assess the potential interest in this core within OpenHwGroup
    - Internally, we continue to see significant interest in this class core
      - Ultra low-end 32-bit programmable processing element, often for use in embedded subsystem designs
      - Low cost, low power core implementation in a “traditional” MCU configuration
  - Need to better understand the estimated resourcing requirements, both people and duration
    - RTL reworking (e.g., port name changes), verification support, updated documentation
    - Other expected tasks?
- Remaining Agenda
  - History of this Core within NXP
  - CoreComplex Interfaces
  - Hardware PPA Metrics
  - More Details on the Debug Architecture

HISTORY OF THIS CORE WITHIN NXP

- Originally used as one of the RISC-V cores of the VEGA MCU test silicon
  - Downloaded the ETH-Zurich PULPino ZeroRISCY core
  - VEGA taped out in June 2018 as RV32M1
  - Included in VEGAboard released in December 2018 (https://open-isa.org/)
- Embedded the ZeroRISCY core within a “CoreComplex”
  - CoreComplex includes ZeroRISCY core + DebugModule (DM) + 3x AHB32 master bus interfaces
    - Bus interfaces to be detailed later, but implementation includes multiple 32-bit AHB interconnects
    - Debug functionality is runtime-selectable between legacy PULPino definition or ratified RISCV.org 0.13.2 spec
    - Interrupt Controller (INTCV) is typically instantiated outside the CoreComplex
  - CoreComplex has been designed into multiple “sockets” within NXP
    - Multiple products taped out with this core in multiple process technology nodes
    - Additional sockets are currently in development or being “explored”
    - Both configurations of general-purpose register file (GPRs) used: 31 x 32b DFFs, 15 x 32b DFFs (RV32E)
  - Very few RTL changes made to the original ZeroRISCY core design
    - A few minor bus fixes
    - Added some missing illegal instruction decodes, added support for ld/st bus errors

CV32E2 CORE COMPLEX INTERFACES




```
cv32e2_core_complex (

// 32-bit AHB master bus interfaces
    imem_h<signal>,     // ahb32 core instruction memory
    dmem_h<signal>,     // ahb32 core data memory
    nidbg_h<signal>,    // ahb32 non-invasive debug

// 32-bit AHB slave bus interface
    dap_h<signal>,      // ahb32 debug access port

// 32-bit APB slave bus interface
    ldbgp_p<signal>,    // apb32 legacy debug access port

// miscellaneous interfaces: interrupt controller, power
    <misc_signals>

);
```

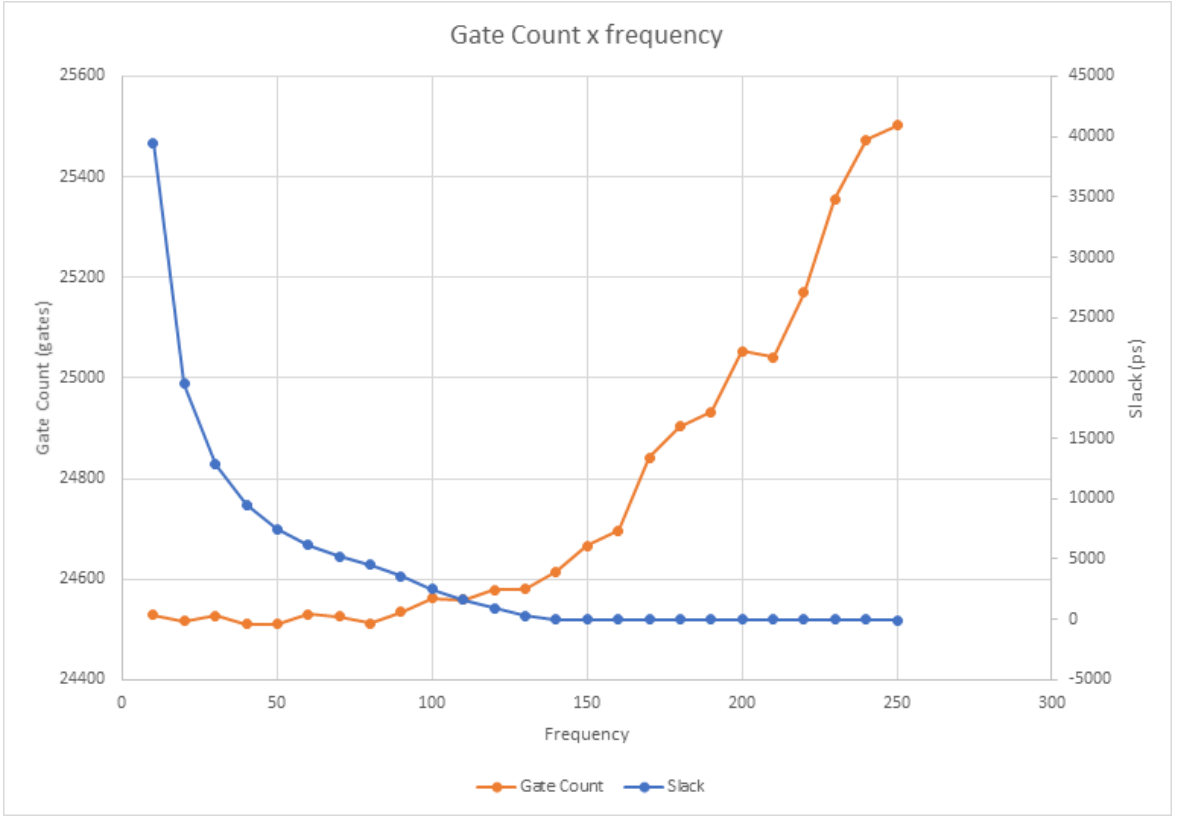
NXP IMPLEMENTATION PPA METRICS

- Module & Submodule Gate Counts
  - 28-nm FDSOI process code, Fmax = 80 MHz

Module	Submodule	Kgates
zeroriscy_core (rv32e)		22.3
	id_stage_i	7.9
	ex_block_i	4.9
	if_stage_i	4.1
	debug_unit_i	2.1
	cs_registers_i	1.7
	load_store_unit_i	1.5
	core_clock_gate_i	0.0
debug		4.9
bus_gaskets		0.5
core_complex (rv32e)		27.7
core_complex (rv32imc)		35.5

- Critical timing paths
  - #1: Reg-to-Outputs, DFF + 44 gate levels + output + setup
  - Arc: **debug_unit_i** > rreq > **id_stage_i** > raddr_b_i[*] > rdata_b_o[*] > **ex_block_i** > alu_i/operand_b_i[*] > alu_adder_result_ex_o[*] > **if_stage_i** > branch_addr_i[*] > **debug_unit_i**/debug_rdata_o[*]
  - #2: Reg-to-Reg, DFF + 53 gate levels + DFF
  - Arc: **debug_unit_i** > rreq > id_stage_i > raddr_b_i[*] > rdata_b_o[*] > **ex_block_i** > alu_i/operand_b_i[*] > comparison_result_o > **id_stage_i** > branch_decision_i > **if_stage_i** > halt_if_i > prefetch_buffer_i/ready_i > rdata_Q_reg

- Early Size vs Fmax curve for ZeroRISCY
  - Notice ‘compressed’ gate count axis, also total timing slack
- 28-nm FDSOI process node
- Familiar “hockey stick” curve, modest in % growth



MORE ON DEBUG ARCHITECTURE AND IMPLEMENTATION

- Debug logic is accessed via a 32-bit AHB slave port connection: Debug Access Port
  - A “filtered” version of this bus is sourced as a 32-bit AHB master for non-invasive memory debug
- Due to “backward compatibility” requirements, the debug architecture “dynamically” supports both riscv.org ratified debug 0.13.2 spec (via Debug Module {DM}) + earlier PULPino debug definition
  - Debug module used is selected based on 1st debug programming model reference after reset
    - Select either riscv.org debug or PULPino debug; remains in effect until the next reset
  - Logic complexity and size could be reduced slightly by only supporting the riscv.org 0.13.2 debug architectural definition
    - The “DM” module size is ~4.2 Kgates
  - OpenOCD driver developed & used in multiple internal FPGA and other debug environments
- NXP has two different interrupt controllers (INTCV) available, each supporting 32 IRQs
  - No programmable priorities in “lite” version; priorities based on input bit number; size = 2.9 Kgates
  - Standard version supports 8 programmable priority levels, equivalent priorities use input bit number to resolve pending IRQ; size = 4.5 Kgates

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