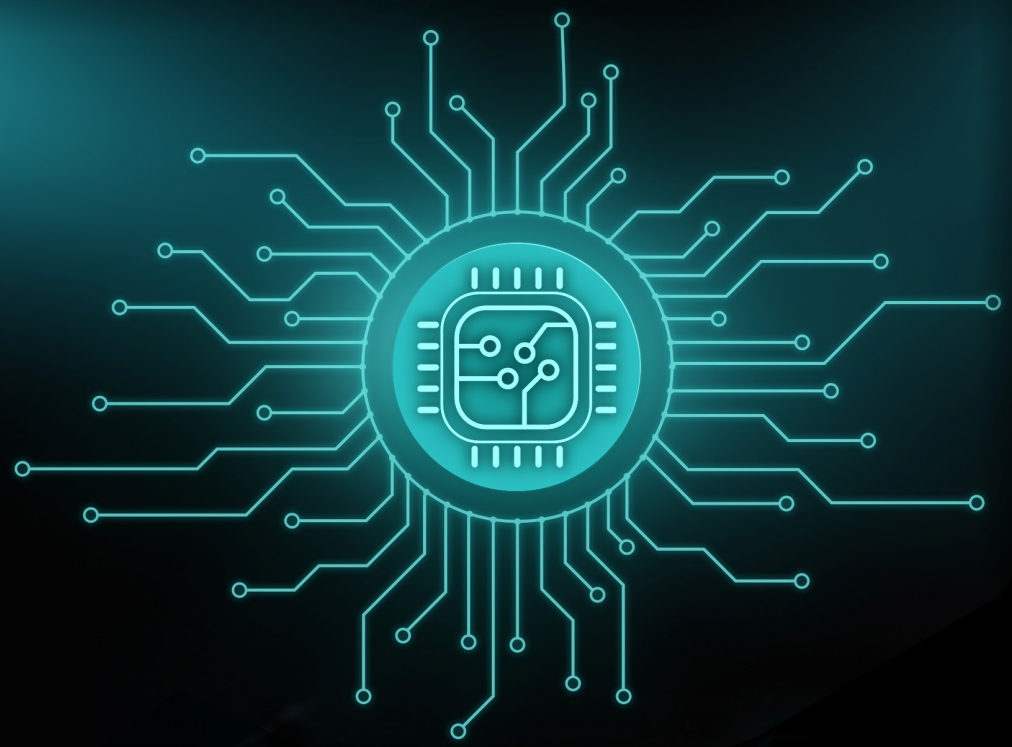

Axiomise Formal Verification Final Update

CVE4

3 DECEMBER 2020

Agile formal verification for RISC-V

GROUP OPENHW™ PROVEN PROCESSOR IP

ULTRA formalISA® Predictable RISC-V formal verification

axiomise® predictable formal verification

Results updated on 3 Dec 2020

master 89fbbd1 Merge pull request #596 from davideschiavone/fix_dc_shell_mult

```
//------------------------------------------------------------------------------------------------------------
//--  formalISA generated log file using Cadence JasperGold 2020.09p001 64 bits for Linux64 3.10.0-327.el7.x86_64
//--  Printed on: Thursday, Dec 3, 2020 03:06:45 pm GMT
//--  Working Directory: /home/xxx/
//--  COPYRIGHT AXIOMISE LIMITED, 2019
//------------------------------------------------------------------------------------------------------------
```

```
================================================================
SUMMARY
================================================================
    Total Tasks           : 1
    Total Properties      : 27332
          assumptions     : 202   (146 disabled)
           - approved     : 0                   ( 0.0% )
          assertions      : 5770  (1160 disabled)
           - proven       : 381                 ( 6.6% )
           - marked_proven: 0                   ( 0.0% )
           - cex          : 4226                ( 73.3% )
           - ar_cex       : 0                   ( 0.0% )
           - undetermined : 4     (3 disabled)  ( 0.1% )
           - error        : 0                   ( 0.0% )
          covers          : 21360 (1428 disabled)
           - unreachable  : 132                 ( 0.6% )
           - covered      : 20694 (896 disabled)( 96.9% )
           - ar_covered   : 0                   ( 0.0% )
           - undetermined : 0                   ( 0.0% )
           - error        : 0                   ( 0.0% )
```

Check Categories	Assertions & Covers
RV32IC ISA checks	Exhaustively Proven
Exceptions, Interrupts, Debug	Exhaustively Proven
Illegal Instructions	Exhaustively Proven
ISIDE, DSIDE	Exhaustively Proven
X-checks	Exhaustively Proven
Deadlocks	Exhaustively Proven

Results updated on 3 Dec 2020

master 89fbbd1 Merge pull request #596 from davideschiavone/fix_dc_shell_mult

	Check Categories	Status	Done	Last updated
1.	Processor coverage targets	Manual Review against published ISA	Yes	3 Dec 2020
2.	Assertion coverage	List of Pass/Fail obtained from Cadence JasperGold®	Yes	3 Dec 2020
3.	Checker completeness	Axiomise methodology	Yes	3 Dec 2020
4.	Over-constraint detection	Axiomise methodology	Yes	3 Dec 2020
5.	Property-driven design coverage	Using Cadence JasperGold®	Yes	3 Dec 2020
6.	Scenario coverage	Axiomise ISA Coverage Analyzer®	Yes	3 Dec 2020