CVA6
Project Launch (PL gate)

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OPENHW GROUP™
PROVEN PROCESSOR IP

Introduction

- Preliminary Project Launch (PPL gate) approved on 2020-09-28
  - core-v-docs/CVA6 preliminary project proposal.md at master · openhwgroup/core-v-docs · GitHub

- Time to have our Project Launch (PL):
  - Resources joining Thales and OpenHW staff
  - More OpenHW bandwidth after CV32E40P RTL freeze

- This PL presentation:
  - Additional details that complete the PPL document
  - Switched to slides for more visual content

Main evolutions (vs. PPL)

- Spun-off projects:
  - LLVM support
    - Can be run in a standalone fashion as CVA6 sticks to RISC-V ISA
  - Core-v-verif
    - Common environment for future CORE-V cores
- Features
  - Considering the addition of a coprocessor interface
    - To be standardized among CORE-V cores
    - FPU could connect to this interface but would presumably be kept internal (and optional) for performance
  - Added RVFI interface

Documentation

- Clarified document structure
  - Document names can evolve
  - Main documents below
- Core:
  - Specification
    - Identifies features agreed upon
    - "What" defined as requirements with identifiers
    - Main input for design and verification work
    - Some sections can be short (references to RISC-V ISA, AXI specs…)
    - Best example: Open Bus Interface
  - Users' guide
    - Includes the specification
    - For CVA6 integrators and users: HW, SW, ASIC, FPGA… viewpoints
    - Need it soon enough
  - Design document
    - Explains the "How": design choices…
    - Not prescriptive, written during or after the design. Useful for next projects.
    - Best example: ARIANE pipeline

Input to

Input to

- Verification
  - Verification Environment Specification
    - User-manual for the verification environment (testbenches, testcases, verification components, etc.)
    - Description of the testbench structure and theory of operation.
    - Best examples: lowRISC IBEX Documentation and the core-v-verif Verification Strategy.
  - Design Verification Plan
    - DVplan, Verification Plan, Vplan: same meaning
    - Feature-by-feature listing of the Device Under Test
      - and a description of how it will be verified
      - and how we know when it is verified (coverage).
    - Examples in: https://github.com/openhwgroup/core-v-docs/tree/master/verif/CV32E40P/SimulationVerificationPlan

Verification

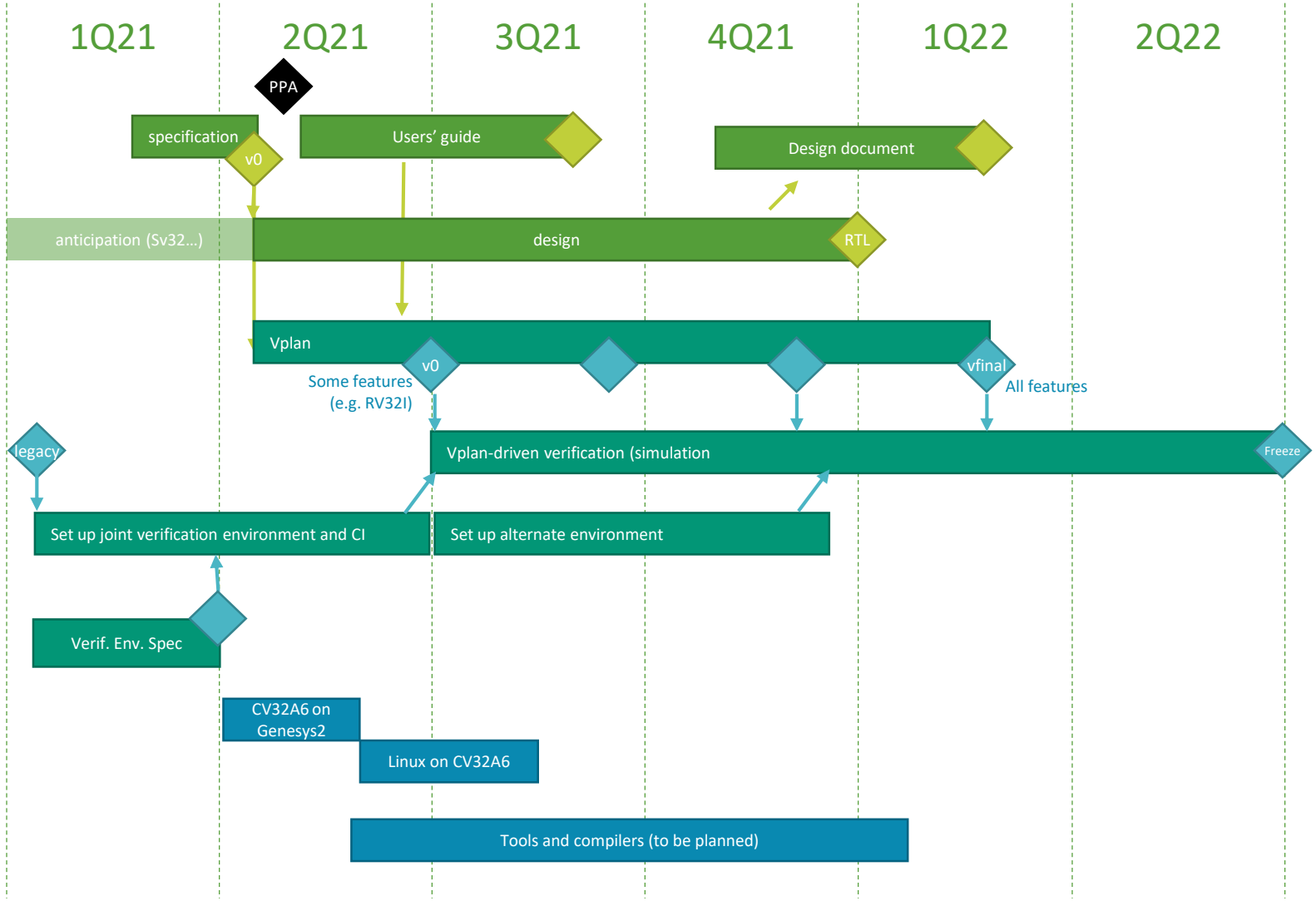
- Two verification environments supported:
  - “Reference” environment with Imperas ISS, UVM step and compare…
  - “Alternative” “sustainable” open-source environment with Spike ISS and Verilator support
- Current gap:
  - CV64A6 verified in Travis environment (ETHZ legacy)
  - CV32A6 verified in Thales-originated bench (https://github.com/openhwgroup/core-v-verif/tree/master/cva6
  - Delays for commits
  - Commit to “legacy” CV64A6 sometimes break CV32A6
  - Some 2020 commits have introduced significant CoreMark decrease
- Priority: set up a joint testbench/CI/commit process
  - Mike has already started ☺

Resources and tasks

- Thales TRT in 2021
  - Jérome: CVA6 TPL, coordinate specification
  - Sébastien:
    - Add Sv32 support (CV32A6), port to Genesys2, support Linux on CV32A6
    - FPGA frequency/resources optimizations
  - Emeric (part time): make WT cache more robust, add a few features
- Thales India: recent hires of senior engineers
  - Pranay: add FPU support to CV32A6, investigate modularity, FPU optimization for FPGA
  - Ranjan (expected e/o March): verification
  - Anjali: toolchain, Linux in cooperation with Sébastien
- Thales INVIA:
  - Fix CV32A6 bugs
  - Coprocessor interface
  - CVA6 LLVM
  - Help transition from CV32A6 testbench
- OpenHW staff
  - Mike:
    - Coordinate verification
    - Verification environment specification
    - Started working on testbench
  - Gianmarco: MEng and PhD student
    - Focus on design
    - First steps could be on documentation
    - Contribution yet to decide
      - Maybe performance/resource optimization for ASIC&FPGA
  - Florian:
    - ?
- Other members?

More verification resources wanted!

Master planning



Actual duration will depend on the available resources.

Focus on some critical and short term tasks. Detailed planning with all tasks (as in PPL) deferred to PPA gate.

Coordination until the PPA gate

- CVA6 meetings every 2 weeks
  - Cross-TG: Specification, verification
  - Participants:
    - CVA6 contributors, including involved OpenHW staff
    - OpenHW chairs and members welcome
- Dedicated technical meetings when needed
- Reporting to task groups and TWG (short)

Thank you!