A 12bit 100MS/s S/H Circuit for Pipeline ADC

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Abstract

A 1.2V, 12bit, 100MS/s sample and hold (S/H) circuit designed for a pipeline analog-to digital converter is presented in this project. The S/H circuit employs capacitor flip-around architecture and a gain-boosted folded cascode operational amplifier is designed as the core part of the whole circuit. And in order to ensure the accuracy and linearity, a linear input buffer and bootstrapped switches are added to the circuit. The circuit is implemented in 0.13μm CMOS technology. According to the simulation results, the spurious free dynamic range (SFDR) of this S/H circuit is 79.31dB, the signal to noise and distortion ratio (SNDR) is 74.84dB and the effective number of bits (ENOB) is 12.14.

Key Words: Sample and hold circuit; gain-boosted operational amplifier; input buffer; bootstrapped switch.

Introduction

With the high-speed development of communication and wireless technology, the demands on analog-to-digital converters (ADCs) are increasing as well. Considering its high speed, high precision and low power consumption, pipeline ADC is playing an important role in wireless communication applications. The core structure of a pipeline ADC is shown in Fig.1 [1]. The pipeline ADC normally consists of an input buffer, a sample and hold S/H circuit, several stage circuits and a backend flash.

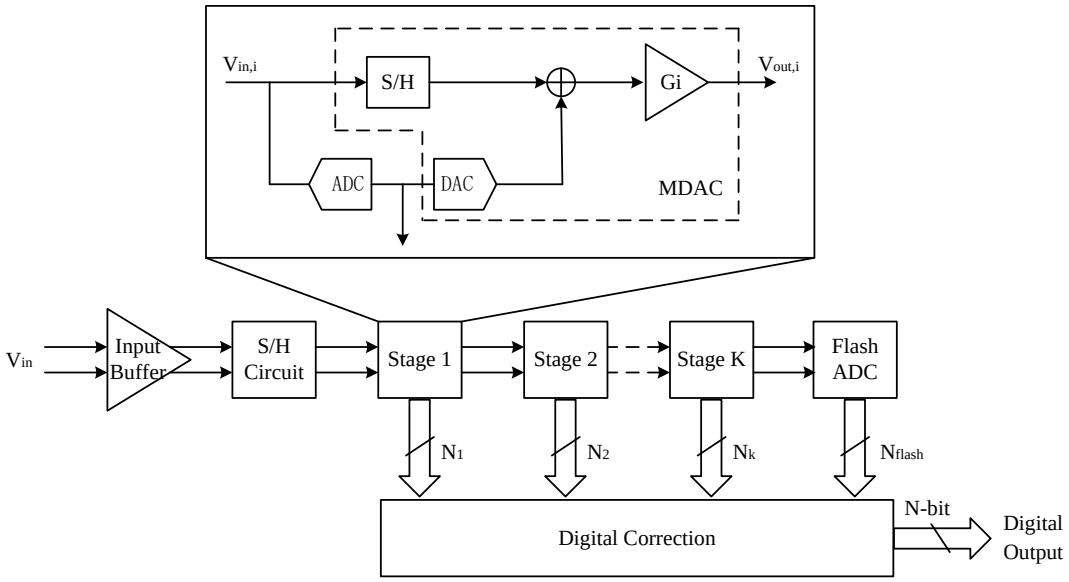


Fig.1 The core structure of a pipeline ADC.

Since a signal should to be sampled and stored before processed by a discrete-time system, the S/H circuit acts as the first stage in the pipeline ADC [2]. The precision and speed of the S/H circuit decide the performance of the whole pipeline ADC. An appropriate S/H circuit can avoid skewing during signal sampling and reduce most dynamic errors of high frequency input signals. In this way, designing a precise and high-speed S/H circuit can bring great improvement on the performance of pipeline ADC.

The operational amplifier is the core part of the S/H circuit. However, designing an amplifier with high gain and wide bandwidth is difficult. A fully differential high-dynamic range gain-boosted technology was proposed in 2000 [3], which achieved a high DC-gain of >84dB with a bandwidth of >30MHz. In this design, the S/H circuit contains a nested gain-boosted differential folded cascode amplifier, of which the DC-gain is around 80dB and the bandwidth is above 300MHz.

In this design, a 12bit 100MS/s S/H circuit is proposed using 0.13μm CMOS technology. The supply voltage is 1.2V. With small size and low power consumption, the S/H circuit can achieve 79.31dB SFDR, 74.84dB SNDR and 12.14 ENOB for a 10MHz input signal and 100MS/s sampling rate.

S/H circuit topology

S/H circuit is responsible for sampling the input analog signal and holding the sampling result for a short time. In other words, the mission of S/H circuit is to complete the discretization of continuous analog signal. Since S/H circuit is the first stage of pipeline ADC, the speed and precision of S/H circuit constrain the performance of whole pipeline ADC.

The simplest S/H circuit consists of a MOS switch and a capacitor, as shown in Fig.2. During sampling phase, the switch is on, sampling capacitor begins to charge and the output follows input signal. While during the holding phase, the switch is off and the output voltage remains at a fixed level.

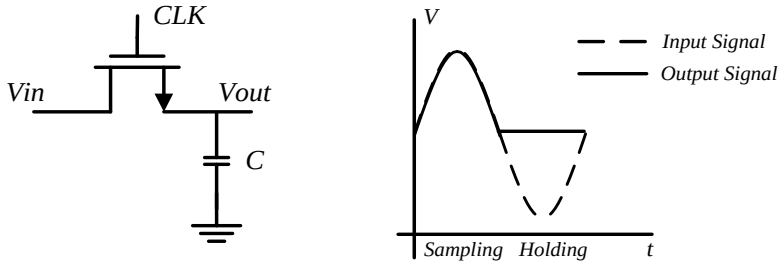


Fig.2 A simple S/H circuit and the waveform.

However, this simple S/H circuit cannot achieve the goals in practical applications. Two kinds of S/H circuit architecture are widely used in pipeline ADC, charge-transferring architecture and flip-around architecture [4].

The charge-transferring S/H circuit is shown in Fig.3. During the sampling phase, clock ϕ_1 and ϕ_{1p} are high level and ϕ_2 is low, and the differential input signals are sampled into sampling capacitors C_s. During the holding phase, ϕ_2 turns high and ϕ_1 and ϕ_{1p} turn low. The amplifier and feedback capacitors C_f form a negative feedback

loop. Charges on sampling capacitors C_s are transferred to feedback capacitors C_f and the circuit stays in holding state.

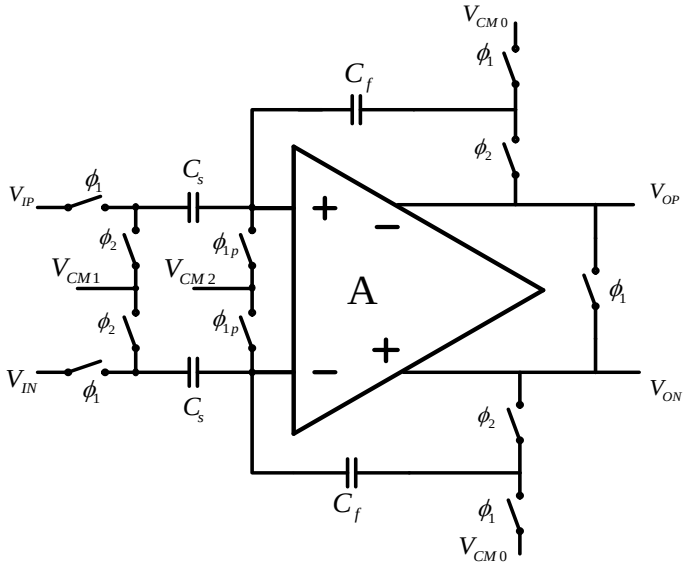


Fig.3 The charge-transferring S/H circuit.

The flip-around S/H circuit is shown in Fig.4. During the sampling phase, ϕ_1 and ϕ_{1p} are high level and ϕ_2 is low, and the circuit works exactly the same as the charge-transferring architecture. The inputs of operational amplifier are connected to the common mode voltage V_{CM}. During the holding phase, ϕ_2 is high and ϕ_1 and ϕ_{1p} are low, and the sampling capacitors C_s flip around. The top plate of sampling capacitor is connected to the input of the amplifier, while the bottom plate is connected to the output of the amplifier. The output is fixed at the point where the sampling phase finished. Therefore, the holding function is realized.

Compared to the charge-transferring structure, the flip-around S/H circuit is the better choice in this design. First, there is only one pair of capacitors used in the flip-around structure, which can avoid the capacitor mismatch error. Second, the feedback factor for the flip-around structure is ideally 1, while in the charge-transferring circuit

the feedback factor is ideally 0.5. Therefore, to achieve the same closed-loop bandwidth, the GBW of the charge-transferring circuit must be twice as much as that of the flip-around circuit. Besides, during the sampling phase, the thermal noise in charge-transferring circuit is higher than that in flip-around circuit as well.

Considering its low noise and low consumption, the flip-around circuit is chosen in this design.

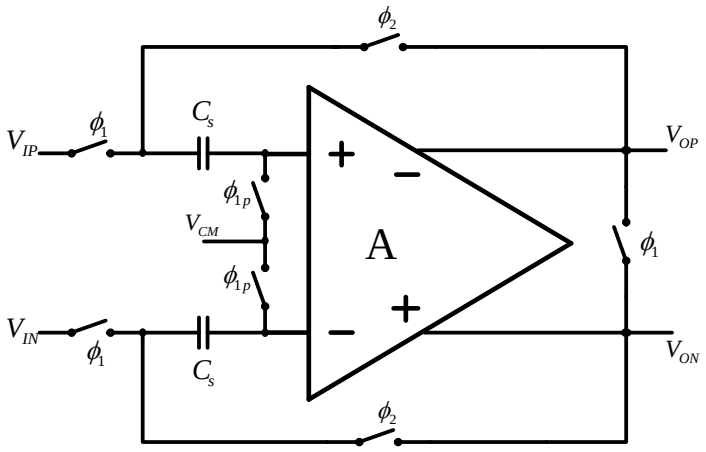


Fig.4 The flip-around S/H circuit.

S/H Circuit Figures of Merit

There are a large number of figures of merit for specifying the performance of one S/H circuit. These specifications can be divided into three categories, static parameters, frequency domain dynamic parameters, and time domain dynamic parameter. In this design, we mainly focus on three frequency domain dynamic parameters to judge the performance of the S/H circuit [5].

(a) Signal-to-Noise-and-Distortion Ratio

Signal-to-noise-and distortion ratio (SNDR) is the ratio of the input signal power to the total power of all other spectral components. The expression of SNDR is

$$SNDR = 10\log_{10}\left(\frac{\text{Signal Power}}{\text{Noise and Distortion Power}}\right) \quad (1)$$

For an M-point FFT of a sine wave test, if the fundamental is in frequency bin m with amplitude A_m, the SNDR can be calculated as:

$$SNDR = 10\log_{10}\left[A_m^2\left(\sum_{k=1}^{m-1} A_k^2 + \sum_{k=m+1}^{M/2} A_k^2\right)^{-1}\right] \quad (2)$$

SNDR reflects the ratio of the input signal to the sum of noise and distortion. It combines another two dynamic parameters, signal-to-noise (SNR) and total harmonic distortion (THD). Therefore, SNDR is an essential parameter to judge the performance of the S/H circuit.

(b) Effective Number of Bits

Effective number of bits (ENOB) is simply the SNDR expressed in bits rather than decibels. It represents the actual precision of the circuit at some input frequency and sampling rate. ENOB can be calculated as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{3}$$

(c) Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the input signal to the peak spurious or peak harmonic component. It can be expressed as:

$$SFDR = 10\log_{10}\frac{\text{Signal Power}}{\text{Largest Spurious/Harmonic Power}} \tag{4}$$

SFDR is an essential parameter in some applications. It represents the smallest value of signal that can be distinguished from a large interfering signal.

The Input Buffer

In this design, an input buffer is used to improve distortion, reduce the kick-back from the sampling capacitor and make it easier to drive. Despite it may increase the power and bring noise, a highly linear buffer can provide the low impedance required to achieve the targeted high linearity.

The traditional input buffer are implemented as a source follower as shown in Fig. 5, which consists of a MOS device and a current source. A major problem of this circuit is that there is nonlinearity caused by the current variation through the MOS device. This problem will cause the device parameters to change with the input signal and lead to distortion. The nonlinearity in the output can be approximated as

$$\frac{\Delta V_o}{V_o} \cong \frac{\frac{\Delta g_m}{g_m}}{1+g_m Z_L} \tag{5}$$

where V_o is the buffer output voltage, g_m is the trans-conductance of the device *M1*, Z_L is the load impedance. From Eq. (5), it is clear to see that the distortion will improve if $\Delta g_m / g_m$ decreases or the load impedance or trans-conductance increases. The traditional solution to improve the distortion is to increase the current of M1, which makes $\Delta g_m / g_m$ small enough to achieve the desired linearity. However, this approach brings high power consumption and increases the device parasitics.

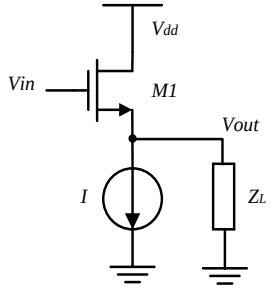


Fig.5 A traditional source follower.

To solve this problem, a buffer linearization technique has been proposed [6], as shown in Fig.6. A replica load *C'* is added to inject a current i_L into the output node of the follower, which is approximately equal to the current pass through the load. In this circuit, the source of *M2* can be considered as a virtual ground due to its high tans-conductance. And *M3* device, as a current source, can force most of its current to the output node due to its large output resistance. Therefore, it keeps the current through *M1* constant and improves the linearity.

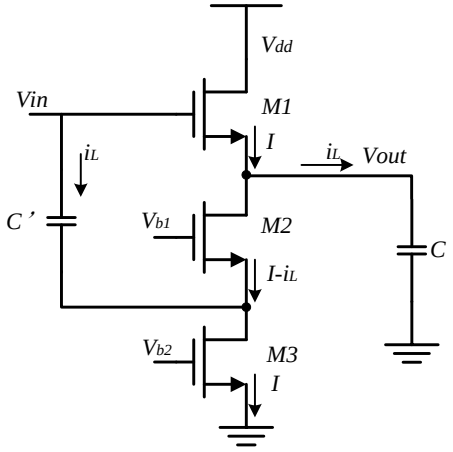


Fig.6 The modified source follower.

The fully differential input buffer used in this design is shown in Fig.7.

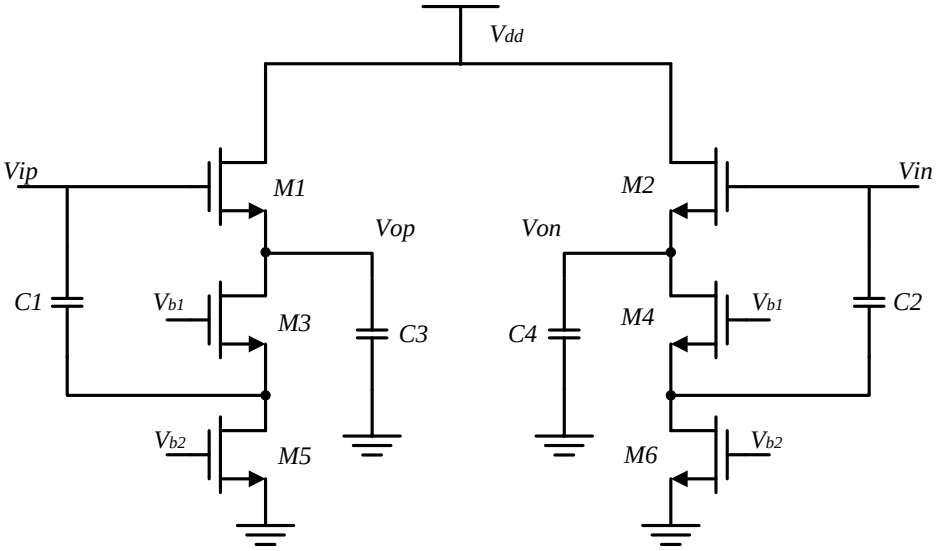


Fig.7 The fully differential input buffer.

Operational Amplifier

Operational amplifier is the core part of the S/H circuit which determines the performances of the S/H circuit and whole pipeline ADC. The operational amplifier is required to have high DC-gain, high GBW, fast transmitting speed, wide output voltage swing, as well as low noise, low power consumption and small chip area.

(a) Estimations of the performance of the amplifier

There are static and dynamic error existed in the practical design. The static error is caused by limited gain of the amplifier. The dynamic error is caused by limited GBW and some other factors. Here, we define the static error as ε_s. For the flip-around S/H circuit, the feedback factor (β) is assumed as 1,

$$\varepsilon_s = \frac{1}{1+A} \tag{6}$$

where A is the DC gain. And ε_s must be less than 1/2 LSB,

$$\varepsilon_s \le \frac{1}{2} LSB = \frac{1}{2} \cdot \frac{V_{FS}}{2^N} \tag{7}$$

where V_{FS} is the input signal range and N is the number of bits. In this design, N=12 and the input signal range from -0.6V to 0.6V. According to Eq. (7), we can calculate the requirement of A.

$$A > 76.7\text{dB} \tag{8}$$

For the dynamic error, assume that the operational amplifier is a single pole system. As a single pole system, there is:

$$A(s) = \frac{A}{1+s/\omega_0} \tag{9}$$

Then,

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1+\beta A(s)} = \frac{\frac{A}{1+\beta A}}{1+\frac{s}{(1+\beta A)\omega_0}} \tag{10}$$

The first order system response can be expressed as:

$$V_{out}(t) = k(1-e^{-\frac{t}{\tau}})V_{in} \tag{11}$$

where $k = \frac{A}{1+\beta A}$, $\tau = \frac{1}{\beta A \omega_0} = \frac{1}{2\pi\beta \cdot GBW}$.

Define the dynamic error as ε_d, we have,

$$\varepsilon_d = e^{-\frac{t}{\tau}} \le \frac{1}{2} LSB \tag{12}$$

In this project, the sampling rate is 100MHz, which means the period is 10ns. Therefore, the sampling time is 5ns, so we can set 4ns as set up time and 1ns as slew time. From Eq. (12), we can work out that $GBW \geq 351.4$MHz.

Requirements of the amplifier are summarized in Table I.

TABLE I. REQUIREMENTS OF THE OPERATIONAL AMPLIFIER

Supply power	DC gain	GBW	Phase margin	Load
1.2V	76.7dB	351.4MHz	>60°	4pF

(b) The structure of the operational amplifier

There are four principal topologies of operational amplifier, telescopic cascode, folded cascode, two-stage op amp and gain boosting amp. Table II presents important attributes of each op amp topology [7].

TABLE II. COMPARISONS OF FOUR TOPOLOGIES

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

The DC-gain of a normal single-stage telescopic or folded cascode amplifier is about 50-60dB. And the bandwidth of the two-stage amplifier is not high enough. Hence, in this design we choose the gain-boosted amplifier, whose gain and bandwidth can satisfy the requirements at the same time. Compared to the telescopic architecture, the folded cascode architecture has higher output swing. Despite this comes at the cost of higher power dissipation, lower voltage gain, lower pole frequencies and higher noise, the inputs and outputs of folded-casode amplifier can be shorted together and the choice of the input common-mode level is easier. In this way, we choose the folded cascode architecture as the core part of the gain-boosted amplifier.

The schematic of the operational amplifier in this design is shown in Fig.8.

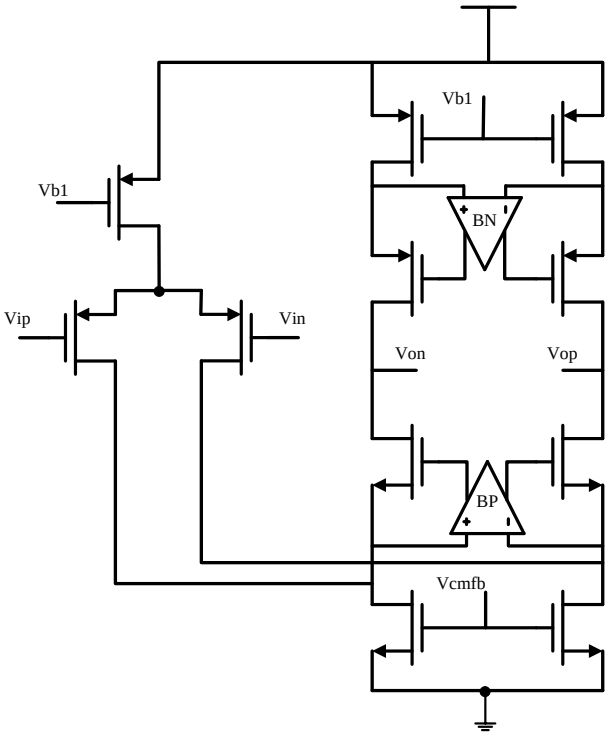


Fig.8 The gain-boosted op amp in this design.

The core amplifier employs PMOS transistors as input differential pairs due to the lower parasitic capacitance. Besides, PMOS transistors can also provide a higher non-dominant pole which helps improve the phase margin.

In Fig.9, a Bode plot is shown for the relationship between the gain and GBW of core amplifier and auxiliary amplifiers [8]. The first-order roll-off of auxiliary amplifier (ω_2) should be larger than the first-order roll-off of whole amplifier (ω_1). This is equivalent to the condition that the GBW of the auxiliary amplifier (ω_4) has to be larger than the first-order roll-off of the core amplifier, but it can be much lower than the GBW of whole amplifier (ω_5). A proper range of ω_4 is $\beta\omega_5<\omega_4<\omega_6$, where ω_6 is the second pole of whole amplifier and β is the feedback factor.

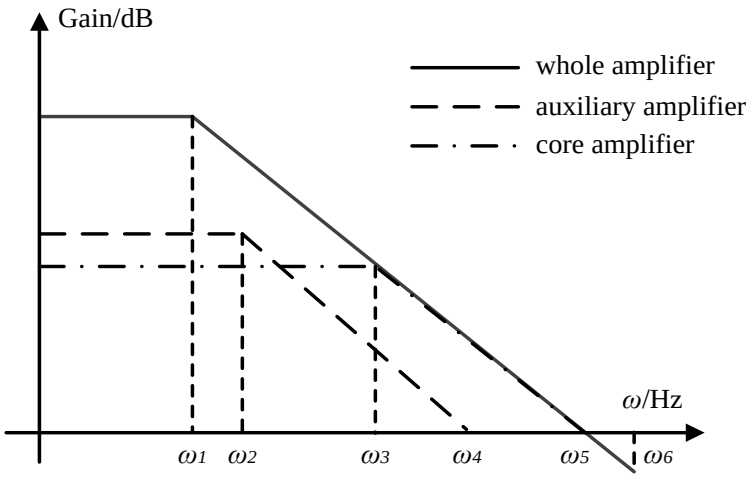


Fig.9 The Bode plot of core amp, auxiliary amp and whole amp.

In this design, similar to the core amplifier, folded-cascode structure is chosen to design auxiliary amplifiers BN and BP as well. The NMOS type gain boosting amplifier, BN is shown in Fig.10. The BP boosting amplifier is the same as the NMOS type except that PMOS differential input pairs are used in BP.

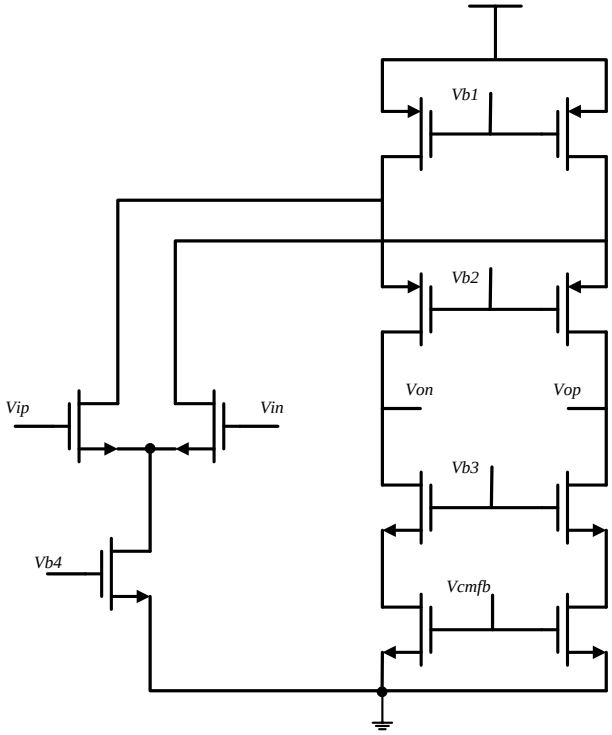


Fig.10 The auxiliary amplifier BN in this design.

Common-mode Feedback Circuit

In high-gain fully-differential amplifiers, the output CM level is quite sensitive to device properties and mismatches, and it cannot be stabilized by differential feedback. Therefore, a common-mode feedback network (CMFB) must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents in the amplifier. There are two kinds of CMFB circuits widely used, switched capacitor common mode feedback circuit (SC-CMFB) and continuous time common mode feedback circuit (CT-CMFB).

The CT-CMFB has high speed, but the input range is limited. Thus, CT-CMFB can work for the auxiliary amplifier circuit, which only has small voltage swing. The SC-CMFB has significant savings on power consumption and little constrain to the output swing of the amplifier, so SC-CMFB is chosen for the core amplifier.

The CT-CMFB used in the auxiliary amplifiers is shown in Fig.11 [9].

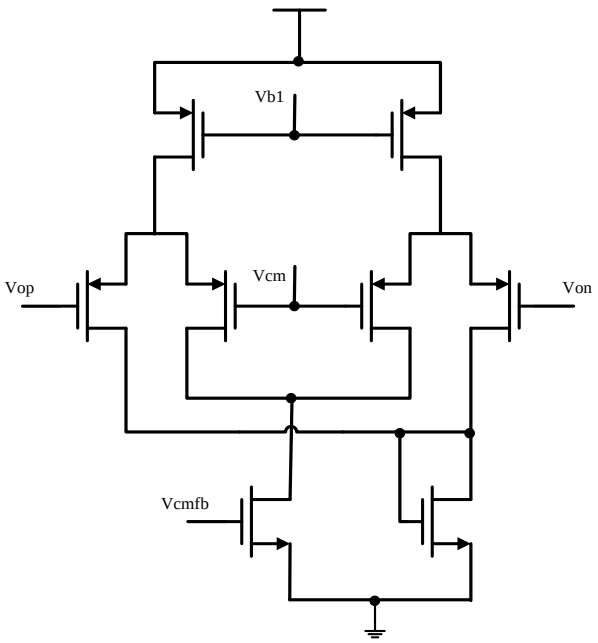


Fig.11 The CT-CMFB used in this design.

A regular SC-CMFB is shown in Fig.12. ϕ_1 and ϕ_2 are two-phase non-overlapping clock signals. ϕ_1 is sampling phase and ϕ_2 is holding phase. V_{CM} is common mode voltage, V_{BIAS} is input bias voltage. When ϕ_1 is high, the total charge amount on C_1 and C_2 is:

$$Q_1 = (V_{OP} - V_{CMFB}) \cdot C_2 + (V_{ON} - V_{CMFB}) \cdot C_2 + 2(V_{CM} - V_{BIAS}) \cdot C_1 \tag{13}$$

When ϕ_2 is high, the total charge amount on C_1 and C_2 is:

$$Q_2 = (V_{OP} - V_{CMFB}) \cdot (C_1 + C_2) + (V_{ON} - V_{CMFB}) \cdot (C_1 + C_2) \tag{14}$$

Because of the conservation of charge, $Q_1 = Q_2$,

$$\begin{aligned} &(V_{OP} - V_{CMFB}) \cdot C_2 + (V_{ON} - V_{CMFB}) \cdot C_2 + 2(V_{CM} - V_{BIAS}) \cdot C_1 \\ &= (V_{OP} - V_{CMFB}) \cdot (C_1 + C_2) + (V_{ON} - V_{CMFB}) \cdot (C_1 + C_2) \end{aligned} \tag{15}$$

Solving Eq. (15),

$$V_{CMFB} = \frac{V_{OP} + V_{ON}}{2} - V_{CM} + V_{BIAS} = V_{out,CM} - V_{CM} + V_{BIAS} \tag{16}$$

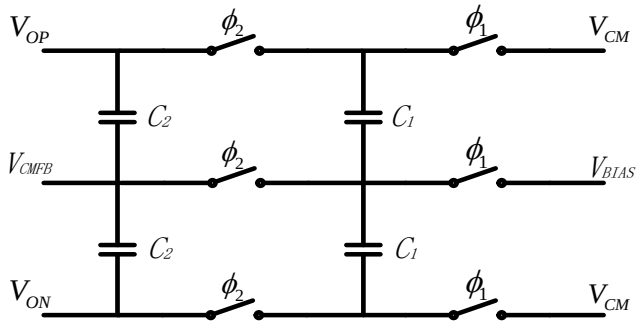


Fig.12 A regular SC-CMFB circuit.

From Eq. (16) we can see that, V_{CMFB}, as the feedback controlling signal, makes the output $V_{out,CM}$ sense and compare with a reference voltage V_{CM} and finally makes them equal.

However, a problem of the traditional structure is that the total loading on differential output varies during different phases. When ϕ_1 is high, the loading is C_2,

while when ϕ_2 is high, the loading turns to (C_1+C_2). To solve this problem, we use an improved version of the SC-CMFB circuit [10], as shown in Fig.13. An extra set of capacitors C_1 and an extra set of switches are added to the original circuit. In this way, the total loading on the differential output is (C_1+C_2) during every clock phase.

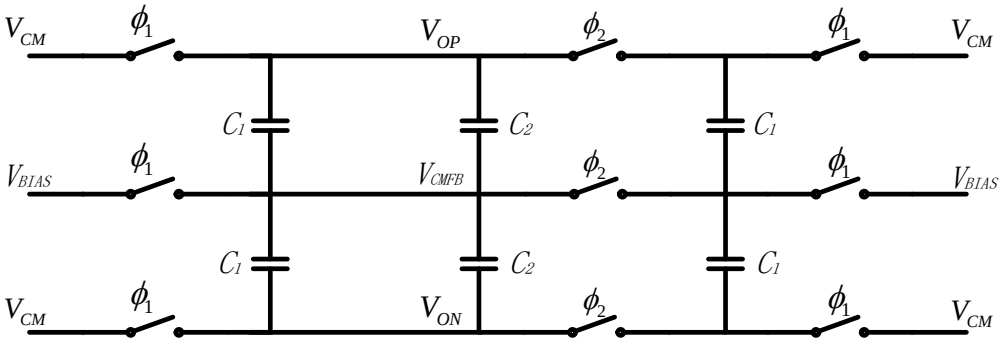


Fig.13 The SC-CMFB used in this design.

Bootstrapped switch

Normally, MOS devices are used as switches in switched capacitor circuit. However, the nonlinearity between on-resistance of switch and voltage may lead to distortion when following continuous-time signal. The on-resistance of NMOS and PMOS can be represented as (17) and (18), respectively.

$$R_{on\_NMOS} = r_{ds,NMOS} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N \left(V_{DD} - V_{in} - V_{tn}\right)} \tag{17}$$

$$R_{on\_PMOS} = r_{ds,PMOS} \approx \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_P \left(V_{DD} - V_{in} - \left|V_{tp}\right|\right)} \tag{18}$$

From above, we can see that: First, when the supply voltage is decreased, the on-resistance will increase because the overdrive voltage is decreased. Second, the on-resistance is related to the input signal, which may lead to distortion.

To solve this problem, bootstrapped switch is designed to replace the simple MOS switch. Bootstrapped switch makes the gate voltage of the MOS switch follow the input signal. By this means, the overdrive voltage will be unrelated to the input signal and become a constant number.

The bootstrapped switch used in this project is shown in Fig.14 [11]. *M1*, *M2*, *C1* and *C2* form a clock multiplier. During the off phase, it enables *M3* to unidirectionally charge *C3*. *C3* acts as a battery across the gate and source of *M12* during the on phase. A single phase clock, *CLK*, controls the whole circuit. When *CLK* goes low, the circuit works at off phase, *M9* and *M10* discharge the gate of *M12* to ground. At the same time, the supply voltage V_{dd} charges the capacitor *C3* by *M3* and *M4*. *M7* and *M11* isolate the

switch from *C3* while it is charging. When *CLK* turns high, *M6* pulls down the gate voltage of *M7*, allowing charge from capacitor *C3* to flow onto the gate of *M11* and *M12* which turns them on. *M11* enables *M12* to track the input signal shifted by V_{dd}. The gate-source voltage will become constant regardless of the input signal, which helps reduce the nonlinear distortion from the on-resistance of switch.

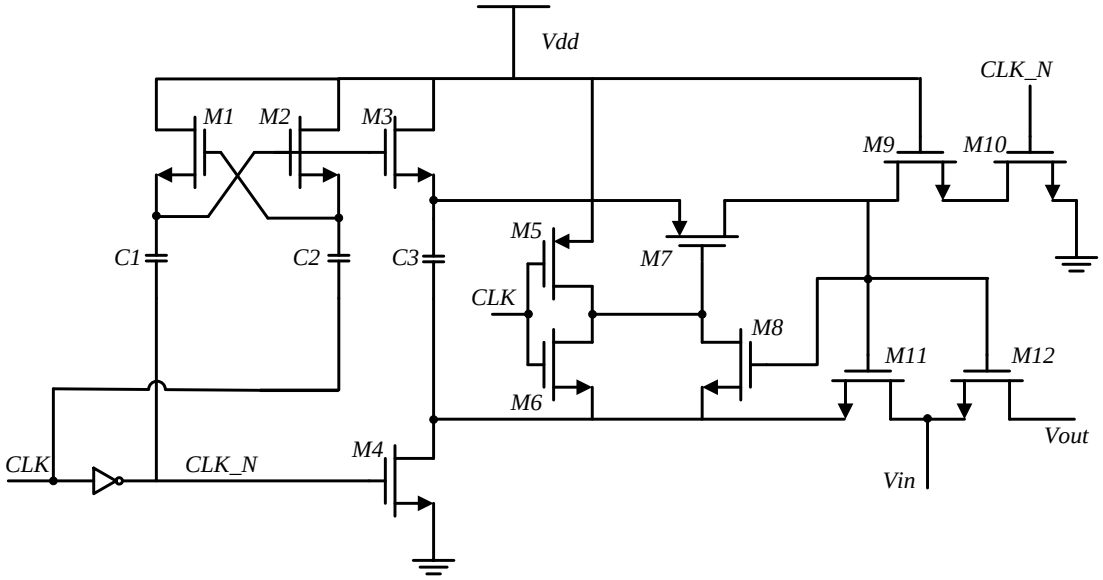


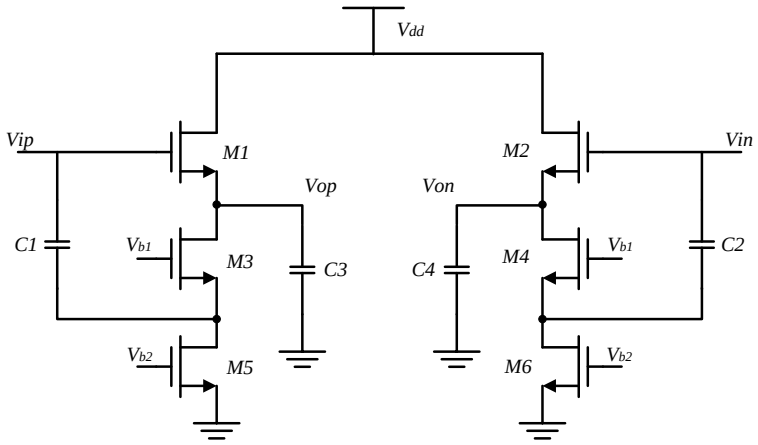
Fig.14 The bootstrapped switch used in this design.

Simulation results

The whole S/H circuit is implemented in a standard 0.13μm CMOS technology. The supply voltage (V_{dd}) is 1.2V. The simulation platform used in this design is Cadence Virtuoso Spectre Simulator. The simulation results of each part of the circuit are listed below.

(a) Simulation results of the input buffer

The schematic of the differential input buffer is shown in Fig.15. The frequency of input signal is 10MHz. Fig.16 is the DFT output spectrum. We can see from the graph that the SFDR is 73.37dB, which is enough for this design.



Vb1=600mV Vb2=350mV

L=300nm W1=W2=96um W3=W4=48um W5=W6=24um

C1=C2=C3=C4=1pF

Fig.15 The schematic of the input buffer.

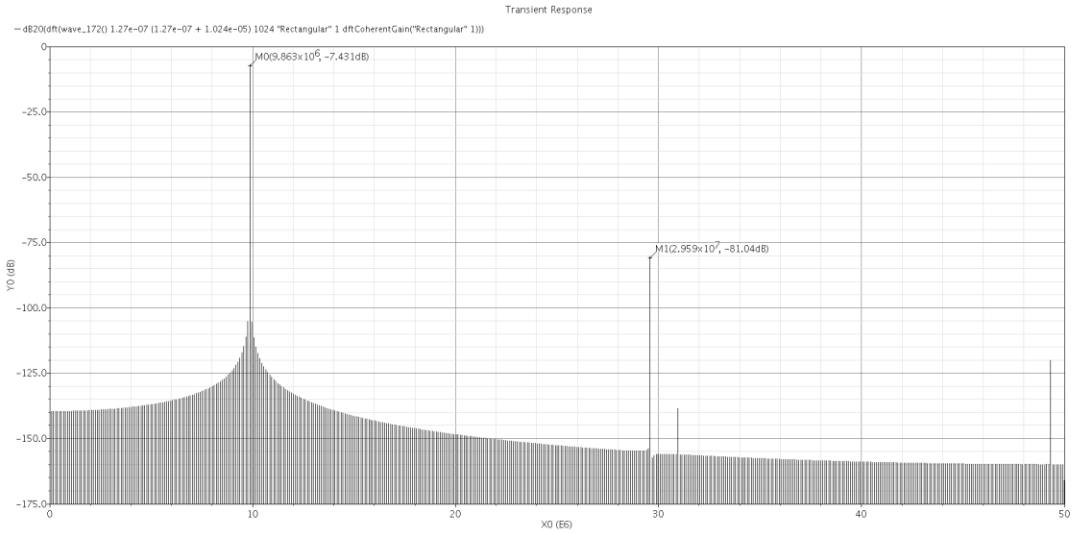
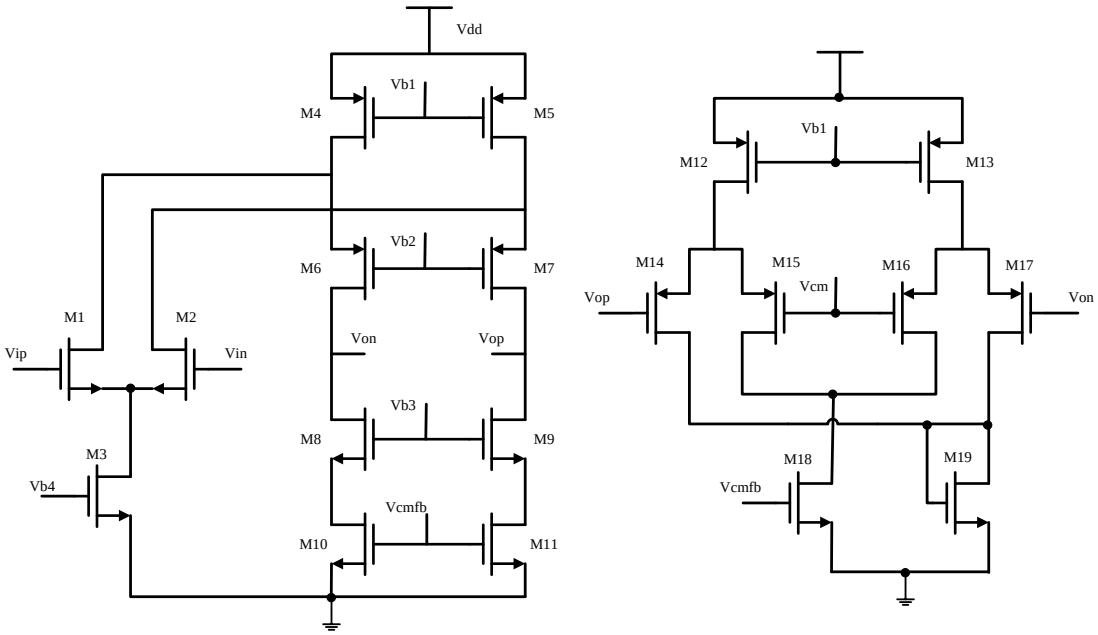


Fig.16 The output spectrum of the input buffer.

(b) Simulation results of the operational amplifier

The simulations of the operational amplifier include the tests of two auxiliary amplifiers, BN and BP, and the whole amplifier. Fig.17, Fig.18 and Fig.19 show the schematics and the values of devices. And Fig.20, Fig.21 and Fig.22 show the AC response of each amplifier, respectively.



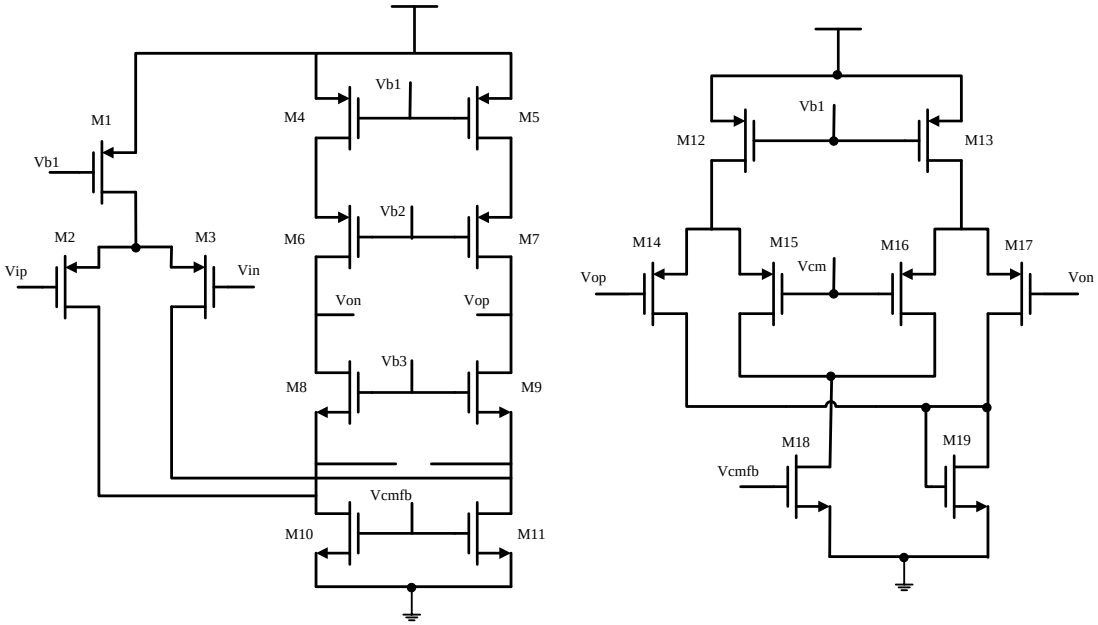
Vb1=740mV Vb2=550mV Vb3=600mV Vb4=400mV Vcm=600mV

L=300nm W1=W2=36um W3=24um W4=W5=150um W6=W7=120um

W8=W9=W10=W11=36um W12=W13=100um W14=W15=W16=W17=90um

W18=W19=24um

Fig.17 The schematic of BN.



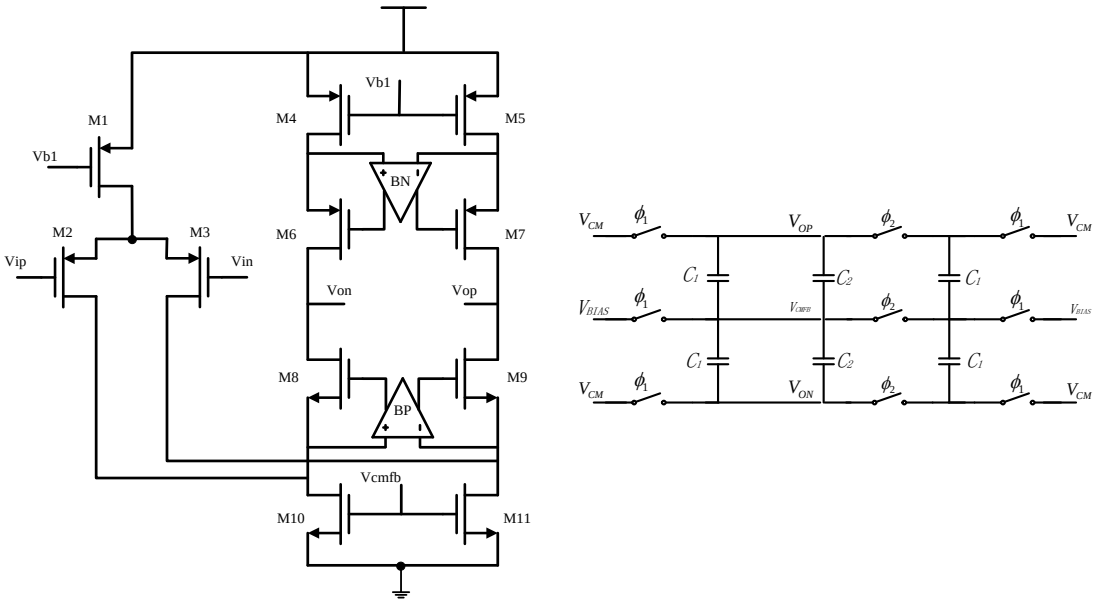
Vb1=740mV Vb2=550mV Vb3=600mV Vcm=600mV

L=300nm W1=90um W2=W3=120um W4=W5=W6=W7=120um

W8=W9=72um W10=W11=36um W12=W13=90um W14=W15=W16=W17=90um

W18=W19=18um

Fig.18 The schematic of BP.



Vb1=740mV Vcm=600mV Vbias=400mV

L=300nm W1=240um W2=W3=200um W4=W5=W6=W7=180um

W8=W9=72um W10=W11=72um C1=0.1pF C2=1pF

Fig.19 The schematic of the whole amplifier.

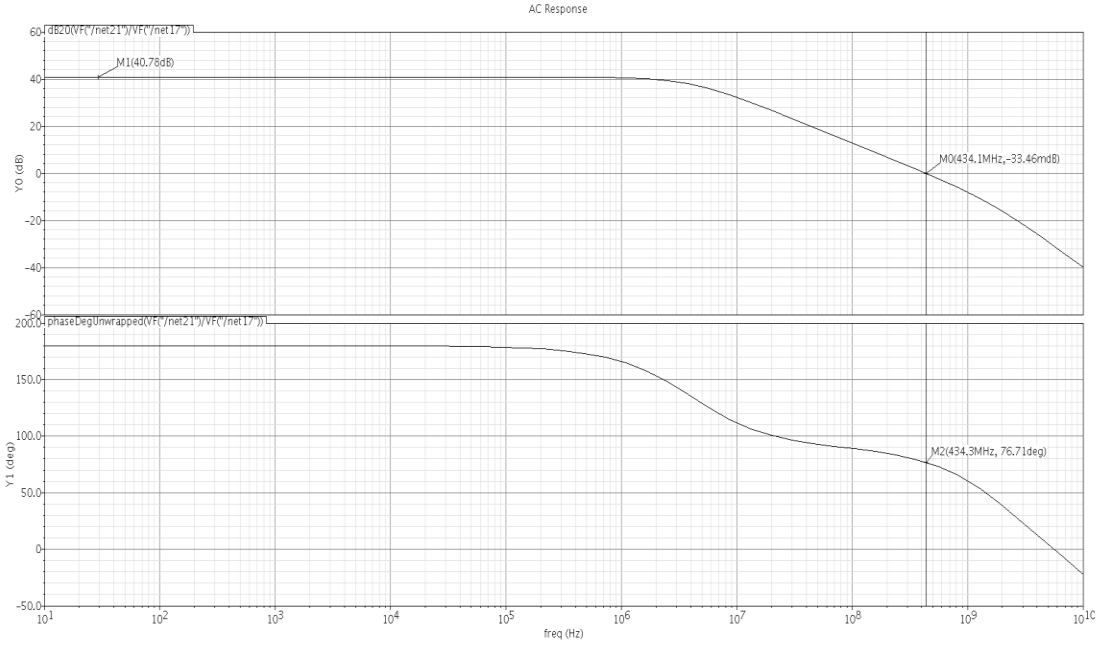


Fig.20 The AC response of BN.

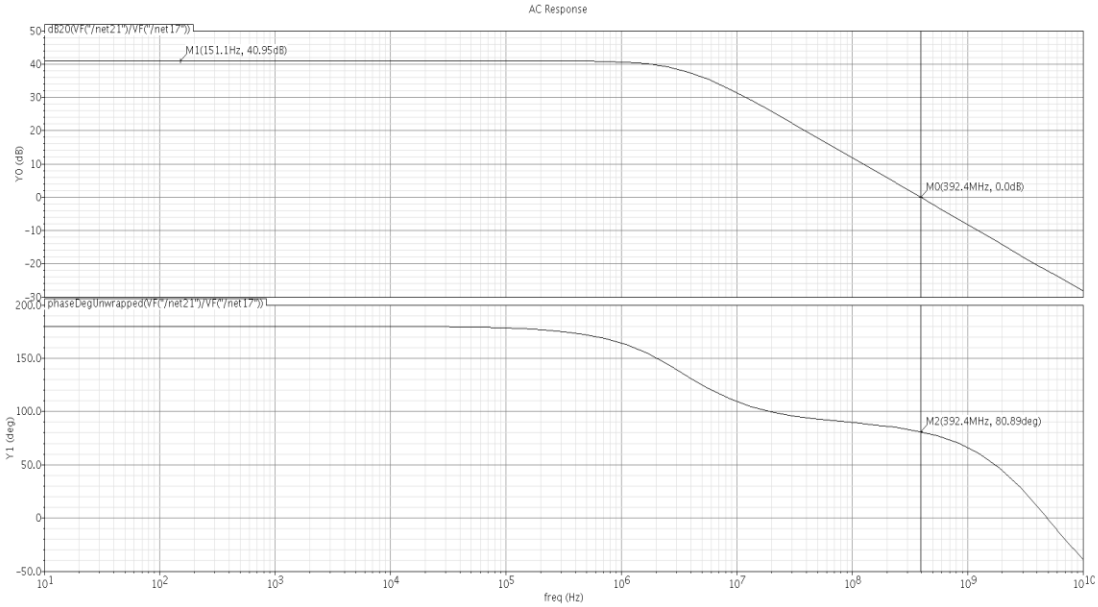


Fig.21 The AC response of BP.

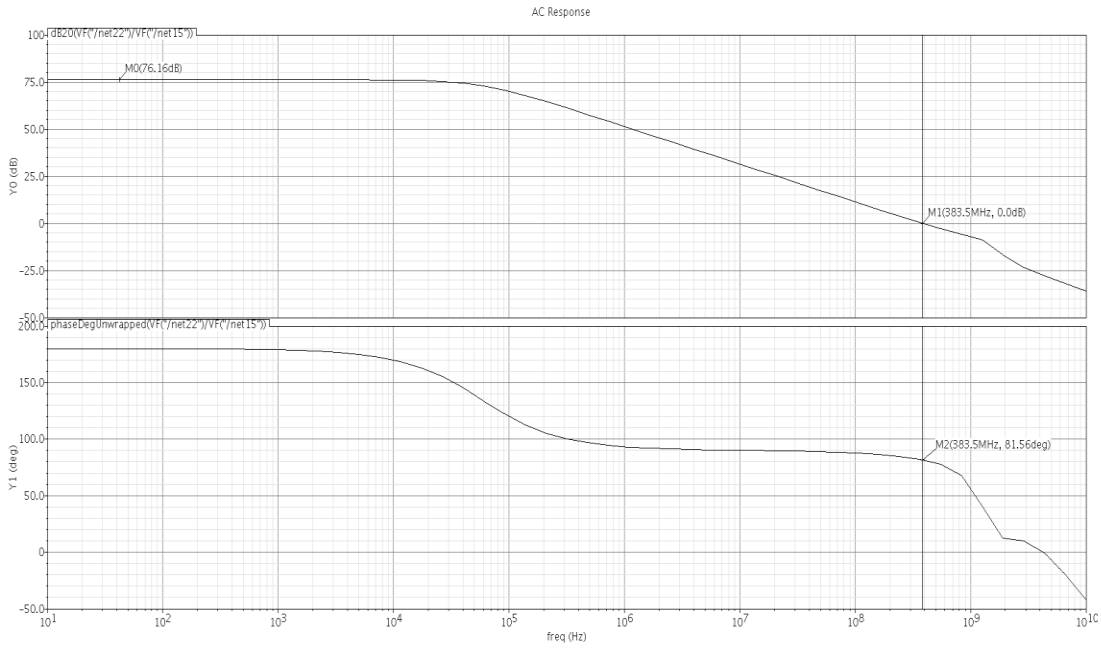
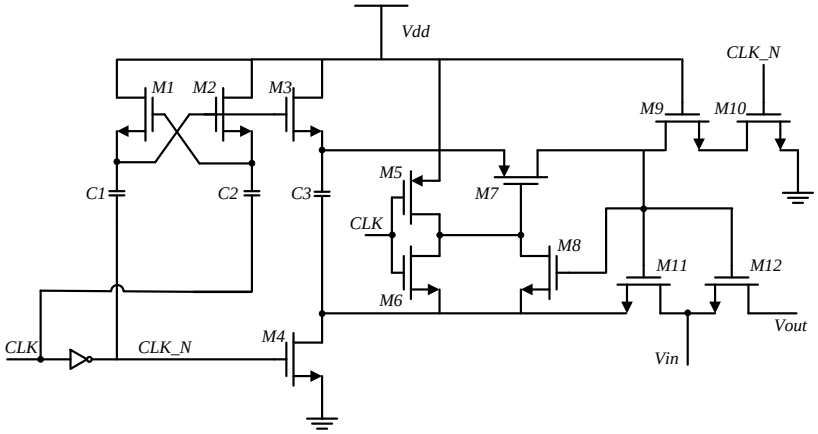


Fig.22 The AC response of the whole amplifier.

From Fig.20, Fig.21 and Fig.22, we can see that the DC-gain of BN is 40.78dB, the GBW is 434.3MHz, and the phase margin is 76.71 °. The DC-gain of BP is 40.95dB, the GBW is 392.4MHz, and the phase margin is 80.89 °. While the DC-gain of the whole amplifier is 76.16dB, the GBW is 383.5MHz, and the phase margin is 81.56 °. The GBW of BN and BP are both higher than that of the whole amplifier, and lower than its second pole. So the GBW of auxiliary amplifiers meet the requirement between auxiliary amplifiers and whole amplifier. Besides, the phase margin of each part is above 60 °, which also satisfy the requirement.

(c) Simulation results of the bootstrapped switch



C1=C2=C3=1pF

L_{PMOS}=L_{NMOS}=120nm W_{PMOS}=18um W_{NOMS}=6um

Fig.23 The schematic of the bootstrapped switch.

The schematic of the bootstrapped switch is as shown in Fig. 23. Fig.24 is the transient response of the gate voltage of M12 when the input signal is a 10MHz, $0.5V_{p\text{-}p}$ sine waveform. And Fig.25 is the transient response of the gate-source voltage (v_{gs}) of M12. From the results, we can see that v_{gs} is keeping constant basically when the switch is on, which means v_{gs} is independent from the input signal. Therefore, the bootstrapped switch achieves the function and has a high linearity.

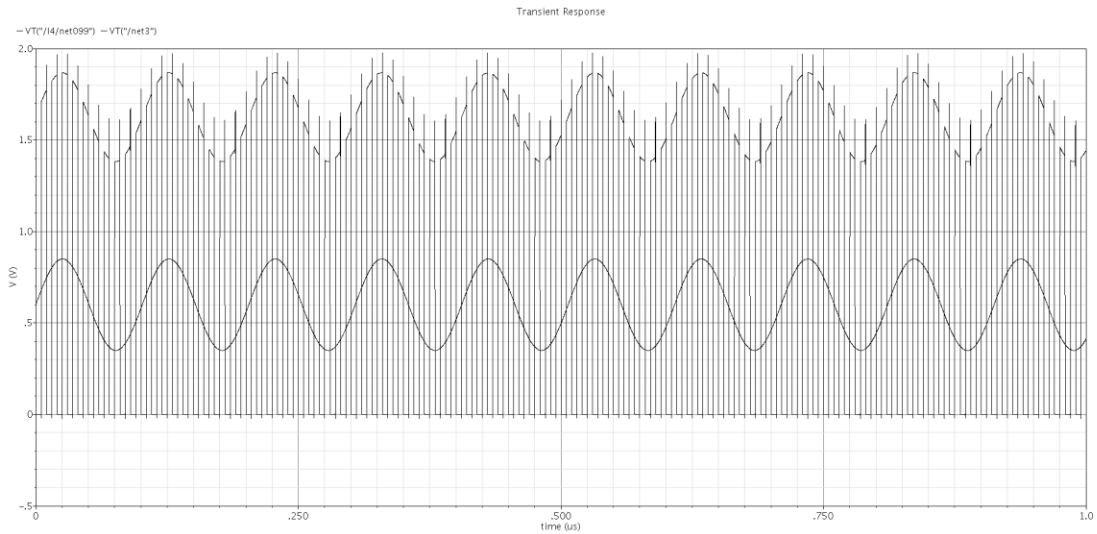


Fig.24 The transient response of the gate voltage of M12.

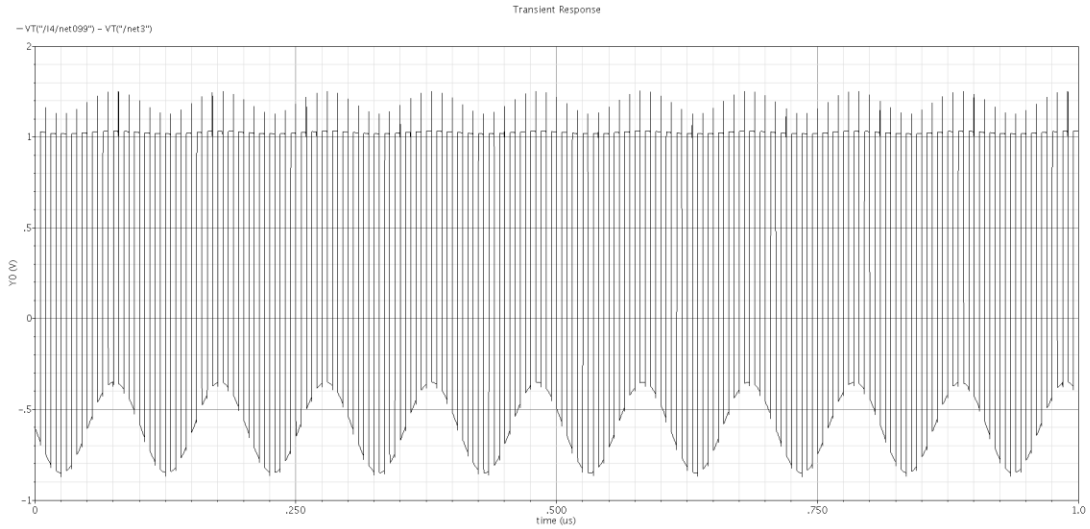


Fig.25 The transient response of the gate-source voltage (v_{gs}) of M12.

(d) Simulation results of the S/H circuit

In this design, the period of clock is 10ns. Sampling phase and holding phase each takes half of period, 5ns. The supply voltage is 1.2V. The input signal is a 10MHz, 1V_{pp} sine waveform. The sampling capacitor is 1pF. Fig.26 (a) is the transient response of the output and a two-period output result is shown in Fig.26 (b). Fig.27 is the DFT output spectrum. The measured results are summarized in Table III.

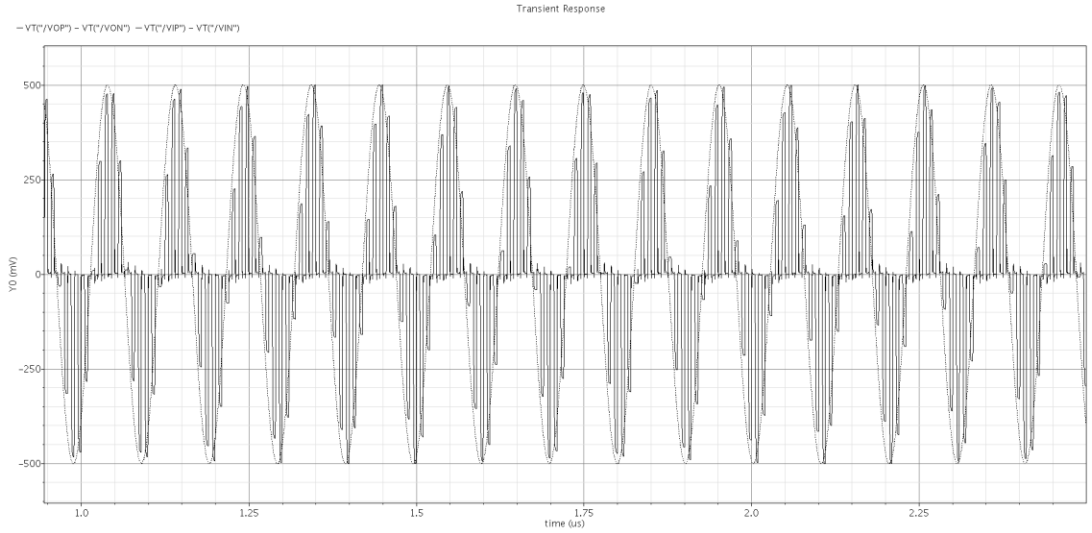


Fig.26 (a) The transient output of the S/H circuit.

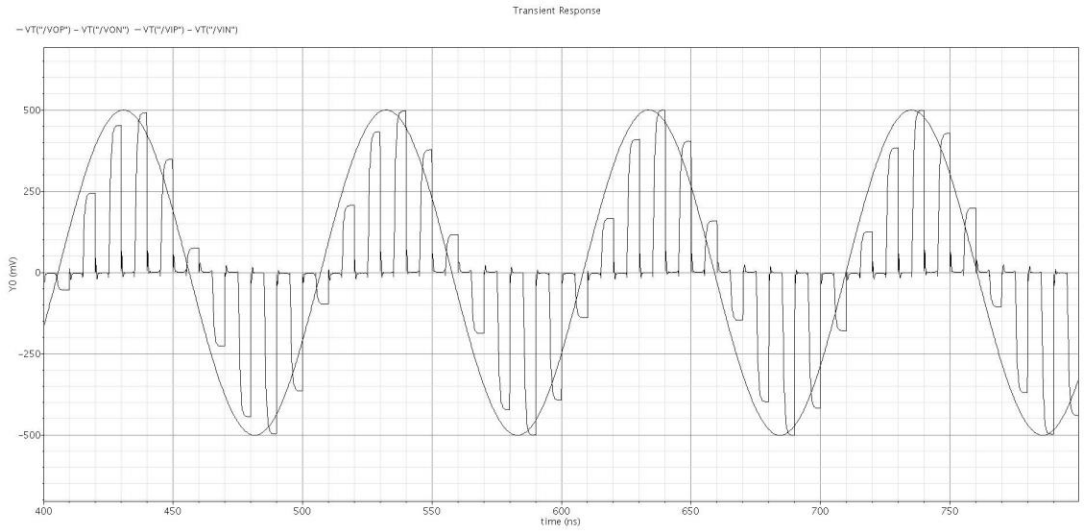


Fig.26 (b) Two-period output result.

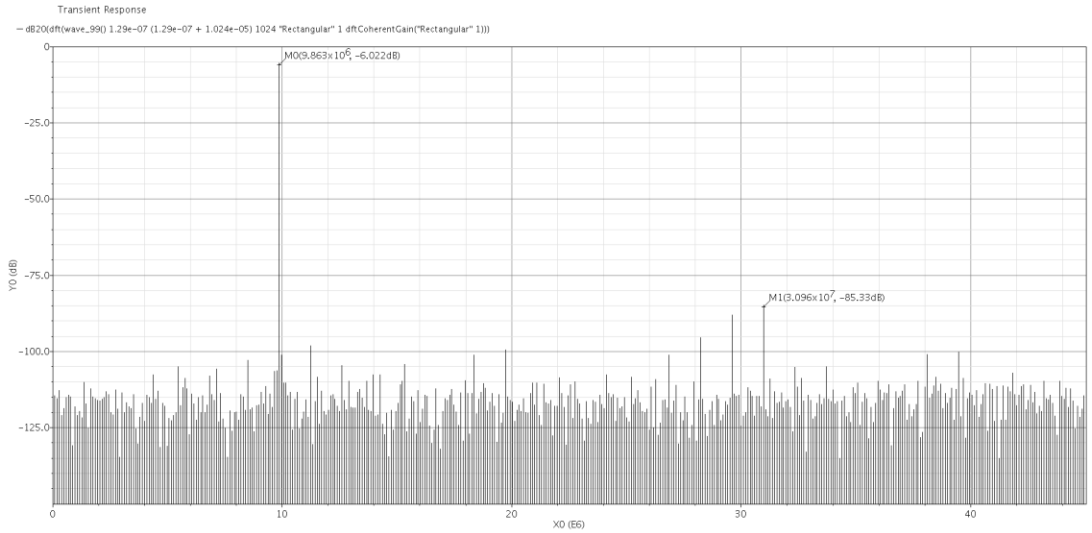


Fig.27 The output spectrum of the S/H circuit.

TABLE III. SUMMARY OF THE MEASURED RESULTS

Parameter	Value
Supply Voltage	1.2V
Input Signal Frequency	10MHz
Input Range	1Vpp
Sampling rate	100MS/s
SFDR	79.31dB
SNDR	74.84dB
ENOB	12.13

From Fig.25, we can see that the transient response is exactly the same as expected. From Table III, we can see that SNDR, SFDR and ENOB all meet the requirement as well.

A comparison table is listed in Table IV. Compared to some other recent work, we

can see that this design has a good balance of precision and speed.

TABLE IV. COMPARISON WITH OTHER S/H CIRCUITS

Specifications	[12]	[13]	[14]	This work
Technology	0.18μm	0.9μm	0.18μm	0.13μm
Resolution	10bit	--	16bit	12bit
Sampling Rate	100MS/s	120MS/s	100MS/s	100MS/s
SFDR	85.4dB	84dB	101.7dB	79.31dB
Supply Voltage	1.8V	1.2V	1.8V	1.2V

Conclusion

In this design, a 12-bit 100MS/s S/H circuit has been proposed. The circuit include an input buffer with high linearity, a gain-boosted folded-cascode operational amplifier with a DC-gain of about 80dB and more than 350MHz bandwidth, and a bootstrapped switch. The whole circuit is implemented using 0.13μm CMOS technology with a supply voltage of 1.2V. The simulation results show that the S/H circuit can achieve high speed, high linearity and meet the practical requirements. This design can be used as an appropriate first stage of a pipeline ADC.

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