Using DRAM with memory refresh is extremely difficult. Digilent provided a sample implementation that makes it somewhat easier to use DRAM by adding a SRAM interface. A big advantage is that the interface is a typical SRAM bus interface without using AXI4.

The zip file contains the sources implementing an audio recorder. The demo files include a SRAM to DDR interface and the audio recorder. The SRAM to DDR specifications is in the zip file and on the web. The audio recorder details is also included are on the web. The project creates 8 banks of memory with each bank containing 8 megabytes or 64 megabytes total. The total available memory is actually 128Mbytes. The high order address bit to the DRAM is set to zero.

A number of changes had to be made to get the sample design working. First all the IP cores had be updated to Vivado 19. The memory controller IP core was designed for a Artix-7 speed grade 1. The core had to be reconfigured for speed grade 3, the chip in Nexy4.

Project instructions

1. Download the zip file from the 6.111 Athena site
2. Unzip and create a new Vivado project
3. Add Verilog sources from [sources_1/hdl] and the constraints from [constrs_1]
4. Finish and create the project
5. In the "Sources" window add the following IP from [sources_1/ip]:
    a. From clk_wiz_0: clk_wiz_0.xci (the other files will be regenerated)
    b. From mig_7series_0: mig_7series_0.xci (the other files will be regenerated)
    c. From xadc_wiz_0: xadc_wiz_0.xci (the other files will be regenerated)
6. Compile and load the bitstream.
7. Attached the mic setup from Lab 5A and plug in the headphones.

Control buttons [short version]

- BTNC press to record/playback
- BTND stop. To erase, press for 2 seconds
- BTNR select one of 8 banks.