# Clocks for Altera DE-Series Boards

*For Quartus II 15.0*

## 1 Core Overview

Most digital circuits are sequential and therefore require at least one clock, while many use multiple clocks of varying frequencies and/or varying phase alignments. Circuits implemented in FPGAs are no different. Therefore, for use in the FPGA, the Altera® DE-series boards include an on-board oscillator which generates a 50 MHz clock. This clock is connected to one or more pins on the FPGA called `CLOCK_50`, `CLOCK2_50` and so on, depending on the number of connections to the FPGA for the particular DE-series boards.

The 50 MHz clocks can be used directly to clock the registers in the FPGA. However, sometimes different clocks are desired either internally to run the circuit faster or slower, or externally for particular peripherals. The SDRAM, Audio CODEC and VGA DAC chips on the DE-series boards require specific clocks. These additional clocks can be generated using specific circuits in FPGAs called phase-lock loops (PLLs). PLLs have many parameters, so to make them easier to use, a suite of three IP cores is provided. These IP cores are described in more detail below.

## 2 Functional Description

The three provided IP cores produces almost identical circuits. A generic block diagram of the cores is shown in Figure 1. They all require an input reference clock and reference reset, which should be connected to input clock and reset pins on the FPGA. The cores all produce output clock(s) and a reset. The differences between the cores are the number of output clocks and their associated frequencies. The following subsections describe each of the three IP cores. The output reset, named `reset_source`, should be connected as the reset to components or modules that use the PLL's output clocks.

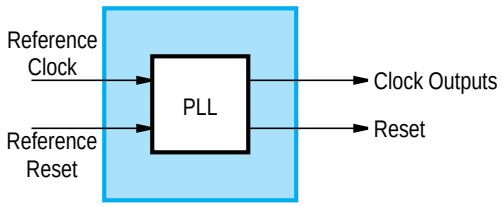


Figure 1. High-level block diagram of the cores.

### 2.1 System and SDRAM PLL

The SDRAM chips on the DE-series board are typically used as part of an embedded system that includes a processor and other components. In this system, the SDRAM chip requires a clock of the same frequency as the rest of the

embedded system but with a specific phase shift. A phase shift refers to the difference in timing of clock edges of two clocks with identical frequencies. The various SDRAM chips of the different DE-series boards require a different phase shift. To simplify matters, this *System and SDRAM PLL* core can generate a system clock at an arbitrary frequency of the user's choosing and create a matching SDRAM clock with the appropriate phase shift for the selected board.

### 2.2 Video PLL

The VGA DAC, video in ADC and Terasic®'s video peripherals, the 5 MP camera and LCD modules, all require clocks with specific frequencies. The video in ADC requires a 27 MHz clock, however this is provided by a second on-board oscillator. Therefore, the clock for the on-board video in chip is not including in this IP core. The clocks for the other video components must be created by a PLL within the FPGA. The 5 MP camera requires a 25 MHz clock. Depending on which LCD module is being used either a 25 MHz, a 33 MHz or a 40 MHz clock is necessary. The clock required by the VGA DAC depends on the desired frame resolution. This *Video PLL* core can be used generate all of these clocks.

### 2.3 Audio PLL

The Audio PLL core can set its output clock to one of the following frequencies: 11.2896, 12.0, 12.288, 16.9344 and 18.432 MHz. These frequencies are required by the audio CODEC chip for different sampling rates. See the audio chip's datasheet (pages 38 - 42) for more information regarding sampling rates and their associated clock frequencies.

## 3 Instantiating the Cores

These three IP cores can be used as part of a system using Altera's Qsys System Integration Tool software or instantiated directly in HDL after being generated using IP Catalog and Qsys. Designers should use the cores' configuration wizards to specify the desired settings. The available configurations for each of the cores are shown in Figures 2, 3 and 4, respectively, and are described in detail in the subsections below. The available configurations are fully enabled for the DE-series boards which have Cyclone V devices or newer. Some configurations are disabled for boards with older devices.

## 3.1 System and SDRAM PLL

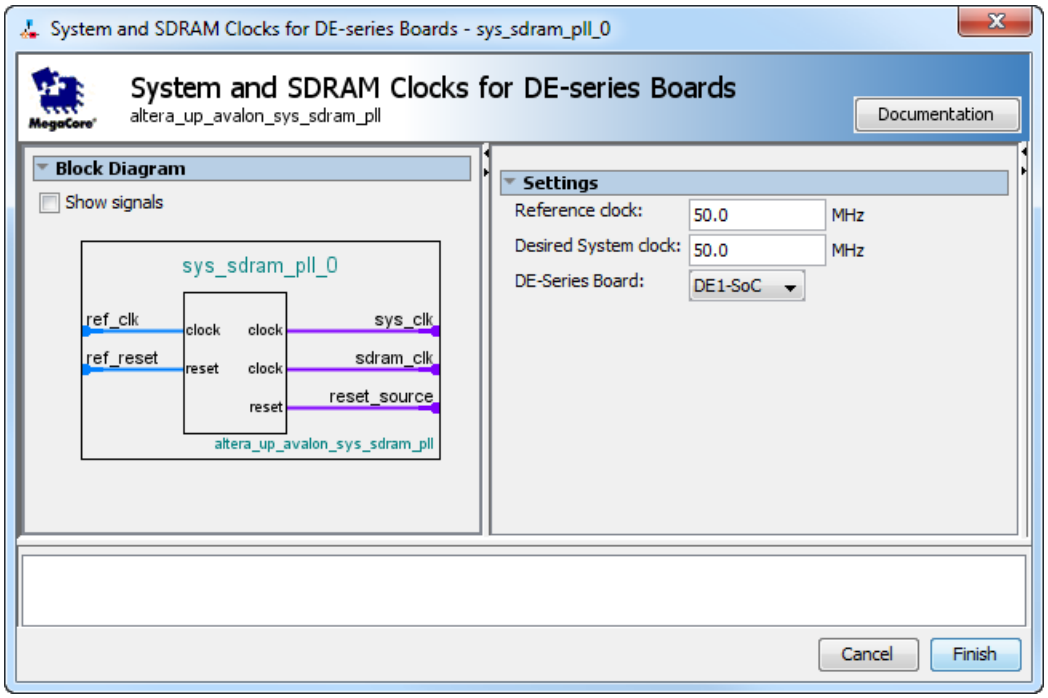


Figure 2. System and SDRAM PLL Configuration Wizard.

- **Reference clock** — allows users to specify the reference clock frequency. Currently, all DE-series boards have a 50 MHz clock input that is normally used as the reference clock.
- **Desired system clock** — allows users to specify the desired clock frequency for their system. Note, that a user's circuit may not be able to run at the desired frequency if too high a number is choosen. The user will have to verify timing by using Altera's TimeQuest analyzer. For more information, on how to setup timing constrainst for clocks and checking that timing was met, please refer to the Using TimeQuest Timing Analyzer tutorial on the Altera University Program website.
- **DE-Series Board** — allows users to specify the target board. This is required to set the correct phase shift for the SDRAM's clock.

## 3.2 Video PLL

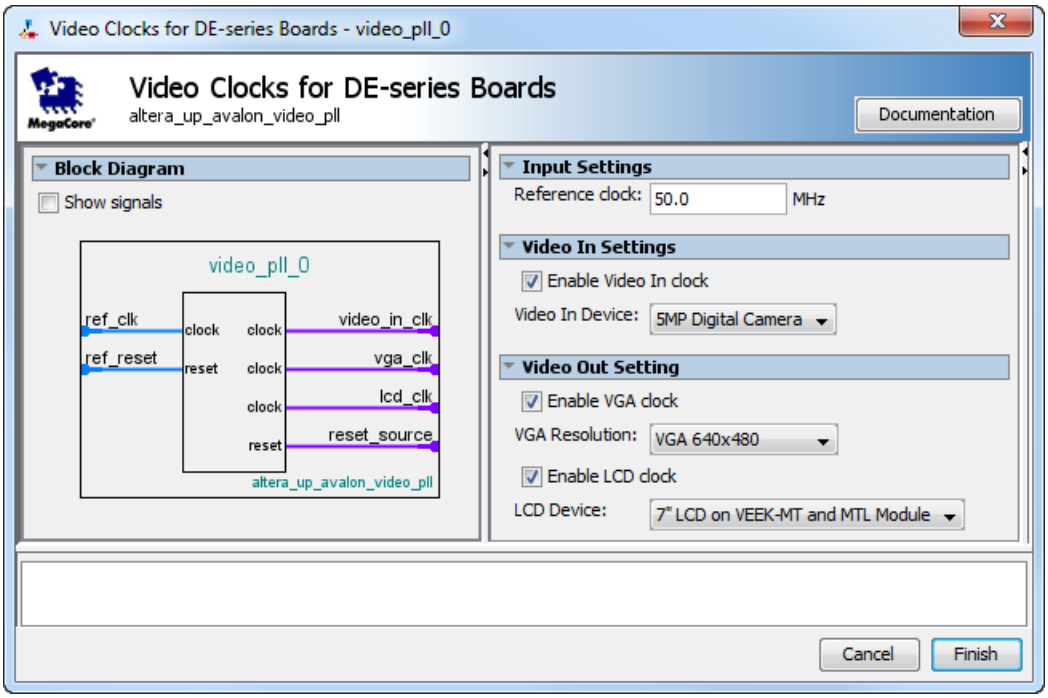


Figure 3. Video PLL Configuration Wizard.

- **Reference clock** — allows users to specify the reference clock frequency. Currently, all DE-series boards have a 50 MHz clock input that is normally used as the reference clock.
- **Enable Video In clock** — allows users to specify whether to generate the clock for the video-in device.
- **Video In Device** — allows users to specify which video-in device is being used. Currently, the only options are none and the 5MP digital camera.
- **Enable VGA clock** — allows users to specify whether to generate the clock for the on-board VGA DAC.
- **VGA Resolution** — allows users to specify the desired VGA resolution. This must correspond to the selection made when using the VGA Controller IP core.
- **Enable LCD clock** — allows users to specify whether to generate the clock for the LCD.
- **LCD Device** — allows users to specify which LCD is being used.

The number of output clocks for the Video PLL depends on the user's selections and can vary from one clock up to three clocks.

## 3.3 Audio PLL

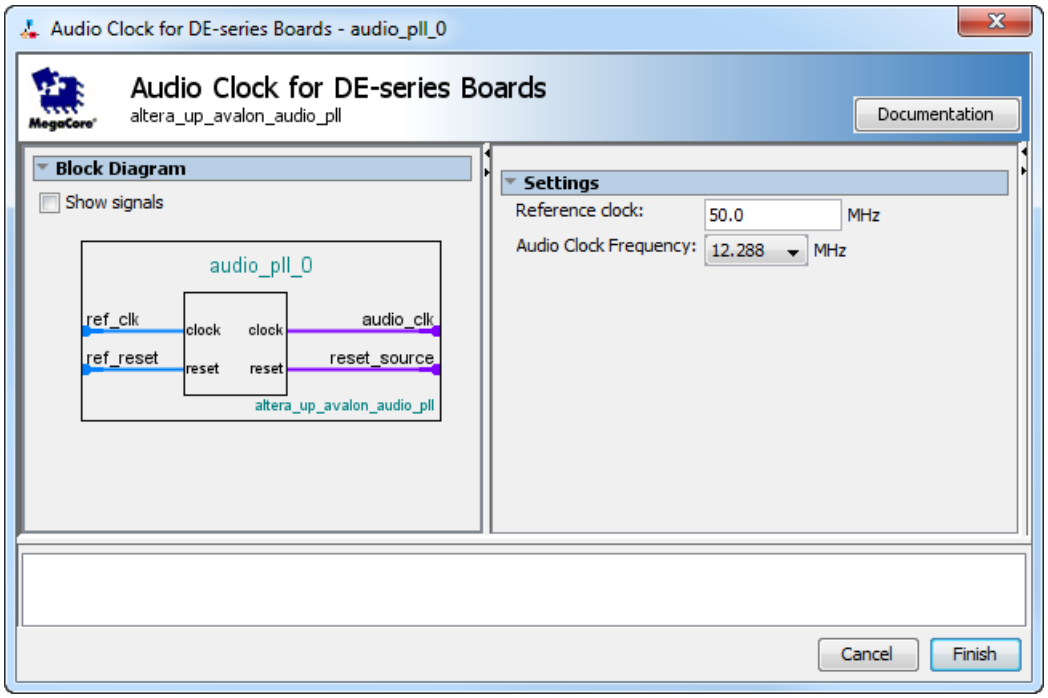


Figure 4. Audio PLL Configuration Wizard.

- **Reference clock** — allows users to specify the reference clock frequency. Currently, all DE-series boards have a 50 MHz clock input that is normally used as the reference clock.
- **Audio clock frequency** — allows users to specify the required audio clock frequency as determined by the sampling rate of the audio CODEC.