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HW#9

Chapter 11

```
1.      LDR         R2,[R0],2
Loop:   SUBS        R1,R1,2
        BEQ         Done
        LDR         R3,[R0],2
        SSUB16      R12,R3,R2
        SEL         R2,R2,R3
        B           Loop
Done:   MOV         R0,R2
        BX          LR
int16_t SIMD_FindMin(int16_t a[], int32_t n){
        int16_t Min=a[0];
        for(i=0,i<n,i++){
                if(a[i]<Min){
                        Min=a[i];
                }
        }
return Min;
endl;
}
3.loop: CBZ         R1,done
        LDR         R3,[R0]
        UBFX        R12,R3,0,8
        ADD         R12,R12,R2
        BFI         R3,R12,0,8
        UBFX        R12,R3,8,8
        ADD         R12,R12,R2
        BFI         R3,R12,8,8
        UBFX        R12,R3,16,8
        ADD         R12,R12,R2
        BFI         R3,R12,16,8
        UBFX        R12,R3,24,8
        ADD         R12,R12,R2
        BFI         R3,R12,24,8
        STR         R3,[R0],4
        SUB         R1,R1,4
        B           loop
done:   BX          LR
```

```
4.Add: VADD.F32     S0,S0,S2
       VADD.F32     S1,S1,S3
       BX           LR
Sub:   VSUB.F32     S0,S0,S2
       VSUB.F32     S1,S1,S3
       BX           LR
Mult:  VMUL.F32     S4,S0,S2
       VMUL.F32     S5,S1,S3
       VMUL.F32     S6,S0,S3
       VMUL.F32     S7,S2,S1
       VSUB.F32     S0,S4,S5
       VADD.F32     S1,S6,S7
       BX           LR
Divi:  VMUL.F32     S4,S0,S2
       VMUL.F32     S5,S1,S3
       VMUL.F32     S6,S0,S3
       VMUL.F32     S7,S2,S1
       VMUL.F32     S8,S2,S2
       VMUL.F32     S9,S3,S3
       VADD.F32     S10,S4,S5
       VSUB.F32     S11,S7,S6
       VADD.F32     S12,S8,S9
       VDIV.F32     S0,S10,S12
       VDIV.F32     S1,S11,S12
```