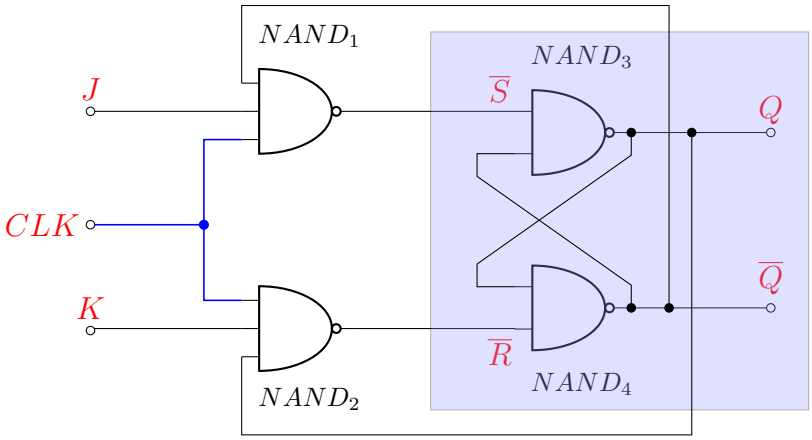
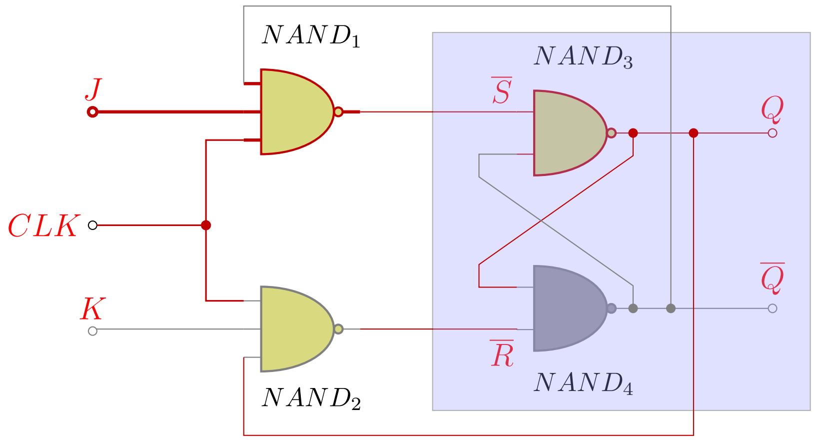
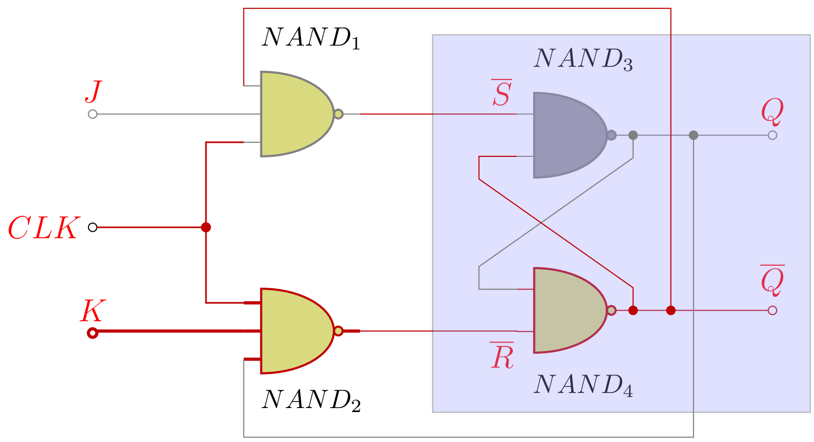
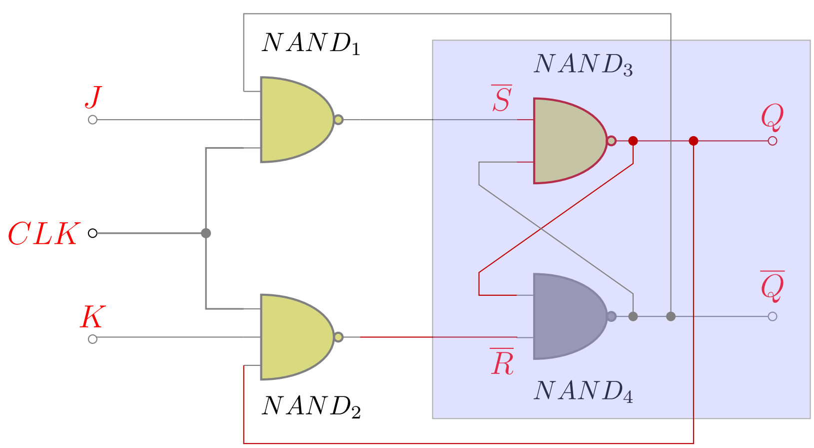
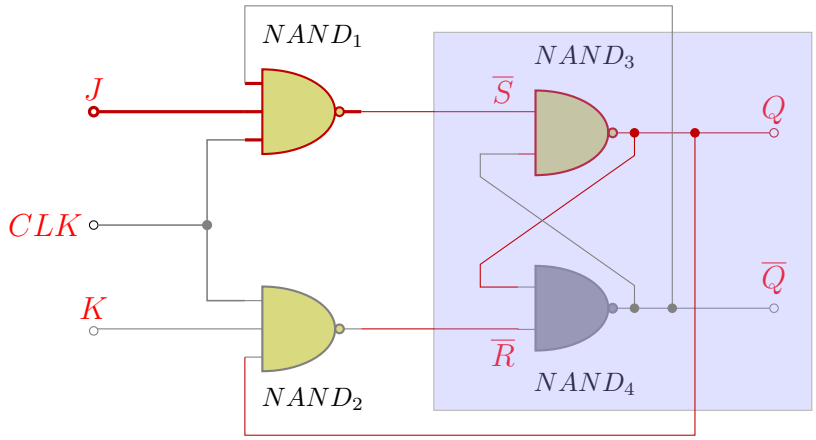


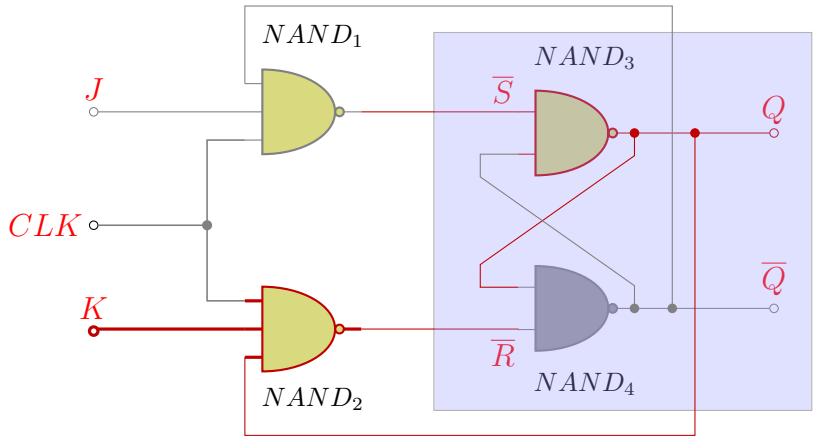
Figure 1: A gate-level schematic of one bit of memory, using a JK flip-flop circuit.


$NAND_1$
$NAND_3$
J
$\overline{S}$
Q
CLK
$\overline{Q}$
K
$\overline{R}$
$NAND_4$
$NAND_2$


$NAND_1$
$NAND_3$
J
$\overline{S}$
Q
CLK
$\overline{Q}$
K
$\overline{R}$
$NAND_4$
$NAND_2$


$NAND_1$
$NAND_3$
J
$\overline{S}$
Q
CLK
$\overline{Q}$
K
$\overline{R}$
$NAND_4$
$NAND_2$





					Previous		Result		
J	K	Clock	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Comment
x	x	0	NC	NC	NC	NC	NC	NC	Locked
0	0	1	0	0	1	0	1	0	No change
0	0	1	0	0	0	1	0	1	No change
1	0	1	0	0	1	0	1	0	No change
0	1	1	0	0	0	1	0	1	No change
0	1	1	0	0	1	0	0	1	Q goes to 0
1	0	1	0	0	0	1	1	0	Q goes to 1
1	1	1	0	0	–	–	–	–	Toggles

Table 1: A truth table for the JK flip-flop.