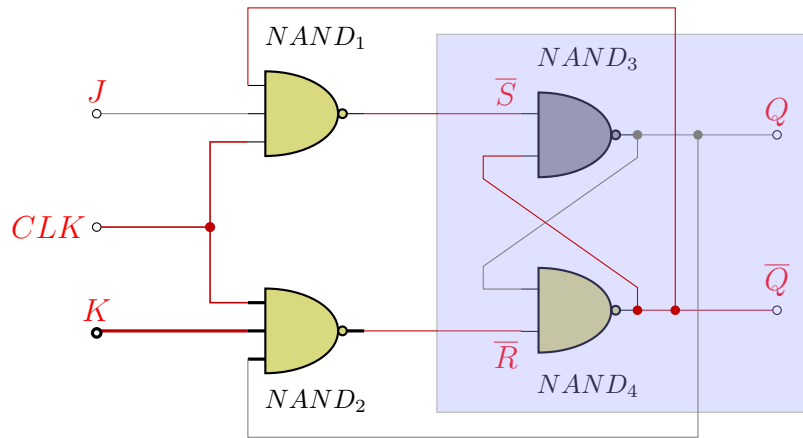Figure 1: A gate-level schematic of one bit of memory, using a JK flip-flop circuit.

2
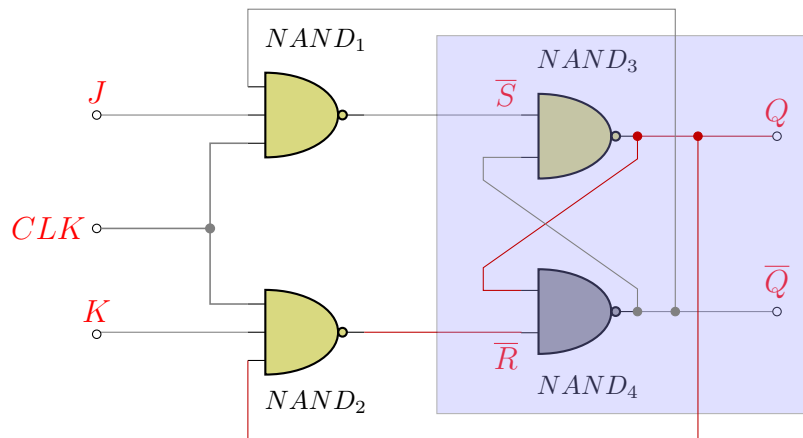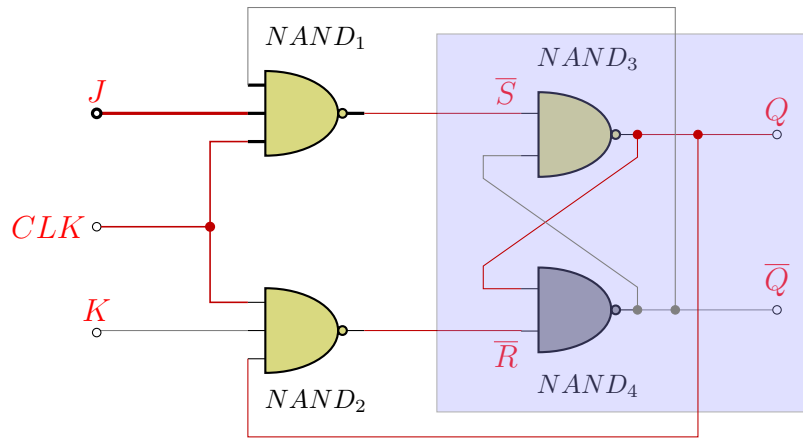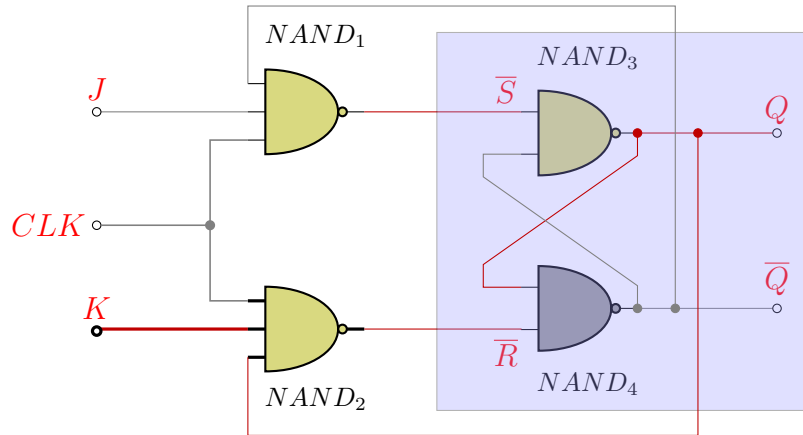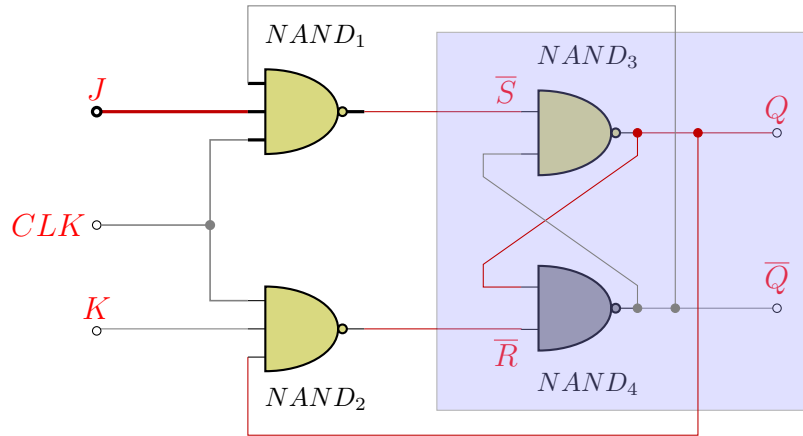
J	K	Clock	$\overline{S}$	$\overline{R}$	Previous		Result		Comment
					Q	$\overline{Q}$	Q	$\overline{Q}$	
x	x	0	NC	NC	NC	NC	NC	NC	Locked
0	0	1	0	0	1	0	1	0	No change
0	0	1	0	0	0	1	0	1	No change
1	0	1	0	0	1	0	1	0	No change
0	1	1	0	0	0	1	0	1	No change
0	1	1	0	0	1	0	0	1	Q goes to 0
1	0	1	0	0	0	1	1	0	Q goes to 1
1	1	1	0	0	–	–	–	–	Toggles

Table 1: A truth table for the JK flip-flop.