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# A Minimal RISC-V Microcontroller in VHDL

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<https://github.com/jesseopdenbrouw/riscv-minimal>

For design `riscv-pipe3-csr-md-lic`

## Abstract

The RISC-V Instruction Set Architecture (ISA) is an open source instruction set for a processor. This means that anybody can create a processor that uses this instruction set. There are already processors available such as E2-core from SiFive. More freeware cores are available on several platforms (e.g. on GitHub). This document describes a basic 32-bit RISC-V processor in VHDL. The processor can execute the RV32IM unprivileged instruction set, and most of the instructions from the privileged instruction set. The processor incorporates a ROM, RAM, some simple I/O, a CSR and LIC (local interrupt controller). It is targeted for implementation on an FPGA. It is tested on an Intel Cyclone V with a DE0-CV development board from Terasic with the use of Quartus Prime Lite 21.1 and QuestaSim Intel Starter Edition 2021.2. The GNU C-compiler for RISC-V is used for software development. Many C programs were successfully tested using the GNU C compiler. C++ is supported but most standard concepts create a binary that is too big to fit in the ROM.

This processor is not intended as a replacement for commercial available processors. It is intended as a study object for Computer Science students.

The processor has a three-stage pipeline and executes each instruction in three clock cycles, but the next instructions are fetched and decoded while the current instruction is executed. Jump/branches taken require three clock cycles. ROM, RAM and I/O reads need two clock cycles. This processor also has a basic Control and Status Registers (CSR) set, suitable to handle traps, and a hardware integer multiplier/divider.

This is work in progress. Things will certainly change in the future.

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## 1 Introduction

This document describes the buildup of a simple, one core, RISC-V processor, completely written in VHDL. The core contains one HART (Hardware Thread). The processor is able to run a compiled C-program. C++ is supported but some concepts (cout with iostream, STL) create binaries that is too big to fit in the ROM. The processor can handle the RV32IM Base Integer Instruction Set as set forward in “The RISC-V Instruction Set Manual Volume I: Unprivileged ISA”. The processor can handle traps (interrupts/exceptions). The aim is to synthesize for a minimum clock frequency of 80 MHz. The processor utilizes ROM, RAM and some simple I/O (including TIME and TIMECMP) effectively making it a microcontroller.

The processor requires three clock cycles to complete an instruction, but the next instructions are fetched and decoded while the current instruction is executed. Jumps, calls and branches taken require three clock cycles because a new instruction has to be fetched. Also, two clock cycles are needed when reading ROM (data), RAM and I/O. ROM and RAM are implemented using onboard RAM block (which are buffered with an output register). The I/O output has a buffer register to speed up the processor. The processor has a basic Control and Status Registers set, offering CYCLE and CYCLEH (completed clock cycles), TIME and TIMEH (time since last reset, in microseconds, shadowed from memory mapped registers), INSTRET and INSTRETH (number of retired instructions), and a basic set of CSRs to handle traps. A hardware multiplication requires three clock cycles to complete. A hardware division requires 32+3 or 16+3 clock cycles to complete, depending on the settings. CSR operations require one clock cycle.

The processor executes at top 1 CPI (clocks per instruction) with a sequential flow of instructions.

## 2 The processor

The RISC-V processors consist of one *core* and of the following building blocks:

- The registers contain intermediate data for calculations.
- The ALU is responsible for almost all computations in the processor.
- The PC is used to point to the currently fetched instruction (not the instruction that is currently being executed).
- The Address Decoder and Data Router is an interface between the memory (ROM, RAM, I/O) and the ALU and registers.
- The Instruction Decoder decodes the fetched instruction and provides control signals to other building blocks.
- The multiply/divide unit adheres the M-standard.
- The ROM contains the program instructions and constant (read-only) data.
- The RAM contains read-write data (mutable data).

- The I/O is an interface with the outside world.
- The Control and Status Registers contains a basic set of register.
- The Local Interrupt Controller determines which trap is to be served.

A block diagram of the core is shown in Figure 1.

## 2.1 Registers

The register file consists of thirty-two 32-bit registers denoted by `x0` to `x31`. Internally, the registers use Big Endian format. Register `x0` (alias `zero`) is hardwired to all zeros. Writing this register has no effect. Reading this register returns all zero bits. Normally, the `x`-names are not used but may be handy when simulating the designs. Table 1 shows the names of the registers as they should be used.

A register can be written to, and two register can be selected for data and/or base address.

**Table 1:** *RISC-V registers and their purpose.*

Register	Name	Purpose	Saver
<code>x0</code>	<code>zero</code>	Hard-wired zero	—
<code>x1</code>	<code>ra</code>	Return address	Caller
<code>x2</code>	<code>sp</code>	Stack pointer	Callee
<code>x3</code>	<code>gp</code>	Global pointer	—
<code>x4</code>	<code>tp</code>	Thread pointer	—
<code>x5</code>	<code>t0</code>	Temporary/alternate link register	Caller
<code>x6–x7</code>	<code>t1–t2</code>	Temporaries	Caller
<code>x8</code>	<code>s0/fp</code>	Saved register/frame pointer	Callee
<code>x9</code>	<code>s1</code>	Saved register	Callee
<code>x10–x11</code>	<code>a0–a1</code>	Function arguments/return values	Caller
<code>x12–x17</code>	<code>a2–a7</code>	Function arguments	Caller
<code>x18–x27</code>	<code>s2–s11</code>	Saved registers	Callee
<code>x28–x31</code>	<code>t3–t6</code>	Temporaries	Caller

## 2.2 ROM

The ROM consists of bytes and is only word addressable for instructions. The ROM is byte, half word and word addressable when reading constant data. Half word and word entries are in Little Endian format. When reading data from the ROM, half word accesses must be on 2-byte boundaries and word accesses must be on 4-byte boundaries. This simplifies the decoding circuitry. The ROM returns undefined data if an access is not aligned. The processor instantiates the ROM in onboard RAM. Rearranging half word and word data accesses in Big Endian format is handled by the ROM decoding unit. Reading ROM (both instructions and data) requires two clock cycles. This is automatically handled by the processor. The pipeline is stalled for one clock cycle when reading from ROM (data).

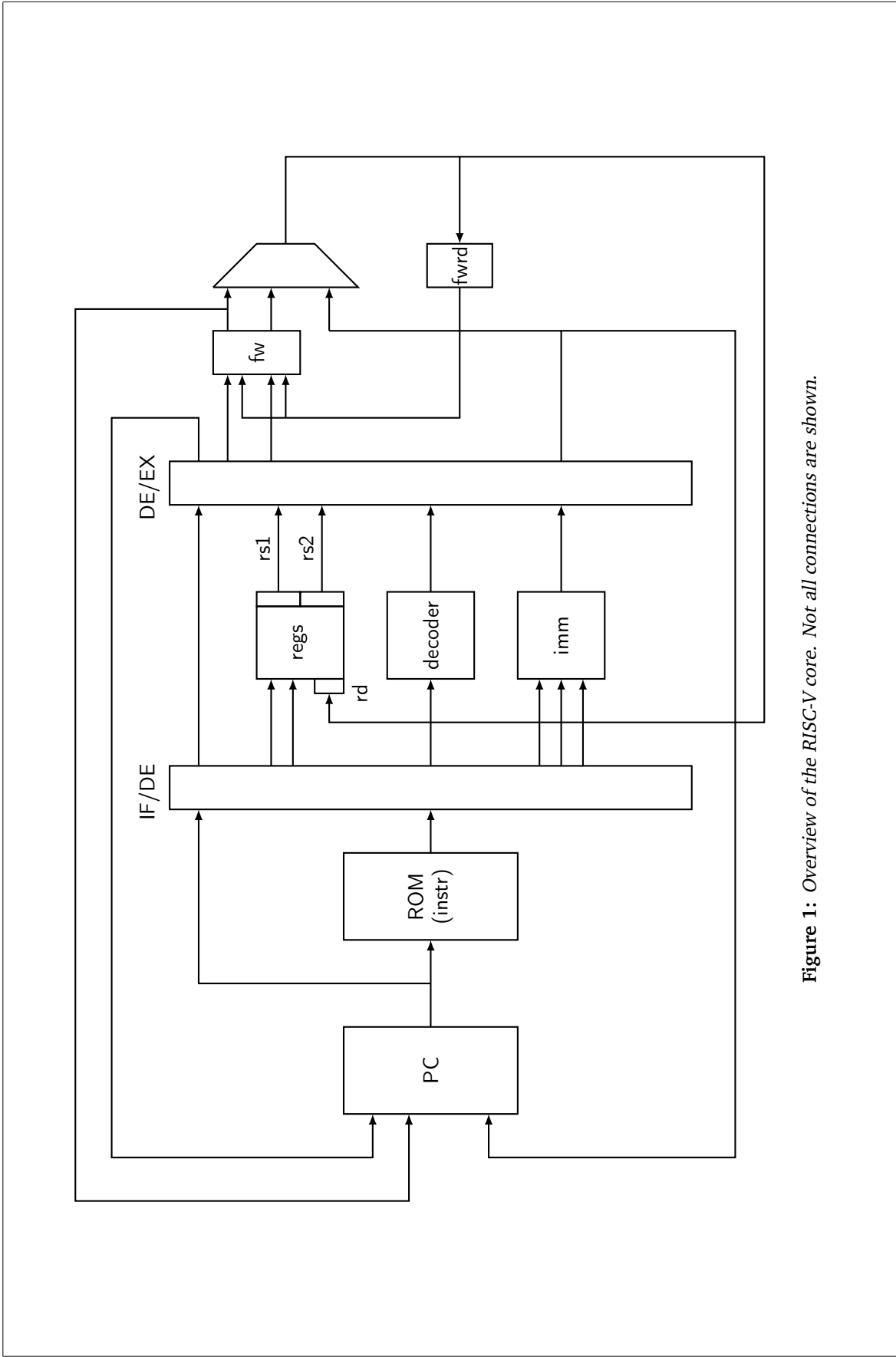


Figure 1: Overview of the RISC-V core. Not all connections are shown.

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Note: the Cyclone V has 3,153,920 bits of onboard RAM available. Because of the 32-bit entries a maximum of 2,097,152 (65536 x 32) bits can be instantiated. This is equivalent to 262,144 bytes.

Note: instructions can only be fetched from the ROM.

## 2.3 RAM

The RAM consists of bytes and is byte, half word and word addressable. Half word and word entries are in Little Endian format. The RAM itself is made up of word (i.e. 32-bit) entries and is instantiated with onboard RAM blocks. Due to this fact, half word accesses are only permitted on 2-byte boundaries and word accesses are only permitted on 4-byte boundaries. The RAM returns undefined data if an access is not aligned. Writes will not take place if an access is unaligned. This simplifies the decoding circuitry. For the Cyclone V a maximum of 65536 words of RAM can be instantiated. Rearranging half word and word data accesses in Big Endian format is handled by the RAM decoding unit. The RAM cannot be used for program data.

Note: the Cyclone V has 3,153,920 bits of onboard RAM available. Because of the 32-bit entries a maximum of 2,097,152 (65536 x 32) bits can be instantiated. This is equivalent to 262,144 bytes.

Reading the RAM (byte, half word, word) requires two clock cycles because the RAM output is buffered by a register. This is automatically handled by the processor. The pipeline is stalled for one clock cycle.

## 2.4 I/O

Currently, the I/O consists of one 32-bit data input and one 32-bit data output, a simple USART (well, really an UART), a simple timer and the TIME and TIMEH memory mapped time registers. Note that the I/O can only be accessed as words and the addresses must be on 4-byte boundaries. If not on a 4-byte boundaries or not word size reads/writes, reads return undefined data whereas writes will not write data. A read requires two clock cycles (the pipeline is stalled for one clock cycle), a write requires one clock cycle. Note that not all I/O addresses are used.

The USART can transmit and receive data at 7, 8 or 9 bits, no/even/odd parity and 1 or 2 stop bits. Tested speeds are 9600 bps, 115200 bps and 230400 bps. Several status flags are implemented to guide transmission. Note: more identical USARTs will be added. Receive and transmitted character (local) interrupts are provided. These interrupt request must be negated by software. The USART does not provide hardware flow control.

The timer has a 32-bit time register and increments on every clock cycle. It does not have a prescaler. It counts up to a compare match register, after which it will be loaded with 0 again. A compare match (local) interrupt is provided. Whenever the timer count register is greater than or equal to the compare register, an interrupt request is asserted. The interrupt request has to be negated by software.

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The I/O incorporates memory mapped TIMEH:TIME and TIMECMPH:TIMECMP registers. Whenever TIMEH:TIME (as viewed as a 64-bit register) is greater than or equal to TIMECMPH:TIMECMP (as viewed as a 64-bit register) an interrupt request is asserted. The interrupt request is negated if TIMEH:TIME is less than TIMECMPH:TIMECMP. This has to be handled by software.

## 2.5 ALU

The Arithmetic and Logic Unit (ALU) handles all computations on data. It can add, subtract, do logic operations such as AND, OR en XOR, can shift data left or right, and sign extend byte and half word data. Some operations require two registers, some only use one register. Some instructions use one register and immediate data. Furthermore the ALU is also used to determine if a conditional branch should be taken. Note that the RISC-V programmer's model does not incorporate status flags as some other architectures do. This requires some extra instructions when adding or subtracting double word (64-bit) data. This is handled by the C compiler. The ALU is also used to compute the return address from unconditional function calls (JAL and JALR instructions). The data is in Big Endian format. The ALU is the only building block that can write registers. The ALU does not compute multiplications and divisions, by merely passes on data from the MD unit.

Note that the computation of jump target addresses is handled by the Program Counter (PC) hardware.

## 2.6 PC

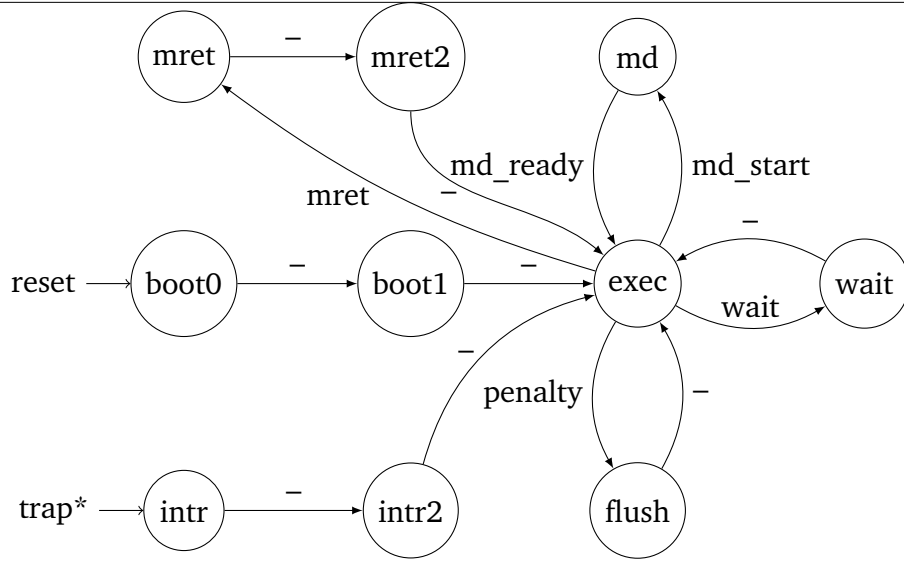
The Program Counter contains the address of the currently fetched instruction. The address is always on a 4-byte boundary although function calls and conditional jump (JAL, JALR en Bxx instructions) can be on non 4-byte boundaries (the C compiler will always create 4-bytes boundaries). The PC (or rather the VHDL description of the PC) handles the address calculations of jumps and branches taken.

## 2.7 Instruction Decoder

The instruction decoder decodes the instruction supplied by the ROM as pointed by the PC. An instruction is 4 bytes wide and in Little Endian order. The instruction decoder provides all control signals for the ALU, RAM, ROM, I/O, the PC, the Address Decoder, the CSR, the register file and the MD unit. Some signals are directly wired to the ROM, RAM and I/O.

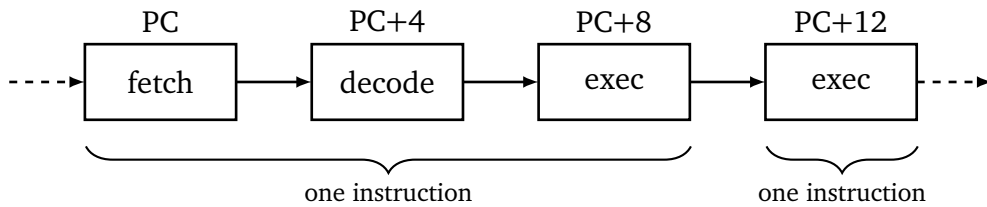
The processor uses a ten-state FSM, see figure 2. The PC points to +8 of the currently executing instruction, in a sequential instruction stream. If a jump or branch taken occurs, the FSM inserts a penalty because the PC has to be loaded with the correct value and a new instruction must be fetched (Figure 3). Reading RAM, ROM and I/O requires an extra state (Figure 4). When a multiply, divide or remainder instruction is encountered, the FSM enters the md state and waits for the md-unit to complete (32+3 or 16+3 clock cycles). Note that penalty, wait and md\_start cannot occur at the same time.



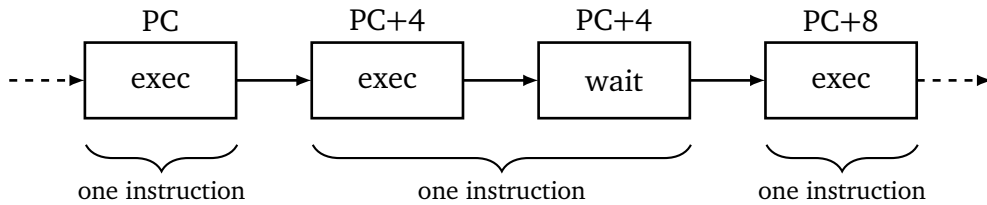


\* trap initiated by hardware or software.

**Figure 2:** FSM of the instruction flow of the processor.



**Figure 3:** State sequence for start up/penalty with instruction execution (no wait state).



**Figure 4:** State sequence for instruction execution (wait state).

### 2.7.1 Trap handling

When an interrupt occurs, the FSM enters the `intr` state for fetching the trap vector. An interrupt can occur any time and is called asynchronous. When an interrupt occurs, the current instruction is discarded and must be restarted after return. After fetching the trap handler, new instructions are fetched and the instruction pipeline is flushed.

Exceptions are synchronous to the executing of instructions. When a exceptions occurs, the current instruction is discarded and must be restarted after return. Exceptions to this are the `ECALL` and `EBREAK` instructions. These instructions do cause a trap, but are not restarted, so the next instruction is fetched after return.

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When a trap request is asserted, the trap vector is loaded in the next clock cycle. Then, in the second clock cycle, the instruction is fetched and in the third clock cycle the instruction is decoded and in the fourth cycle the instruction is executed. On return from a trap handler, the original contents of the PC is fetched from the CSR and then instructions are fetched. A return flushes the pipeline.

## 2.8 Address Decoder and Data Router

The Address Decoder and Data Router routes reads and writes to the ROM (only reads), RAM and the I/O. The processor uses a 32-bit linear address space for ROM, RAM and I/O. In the default setting, ROM starts at address 0x00000000 and the length is 64 kB. Unused ROM addresses return 0x00000000. The RAM starts at address 0x20000000 and length is 32 kB. The I/O starts at address 0xF0000000 and the length is 16 kB by default.

When data is read, the data is collected from the accessed memory and put on an internal bus to the ALU. The ALU can perform sign extension (byte and half word accesses) if needed. Please note that reading data from the RAM, ROM and I/O requires two clock cycles.

Note that instructions can only be fetched from ROM.

## 2.9 Control and Status registers

The RISC-V specification describes a set of 4096 control and status register in a separate address space. CSR operations require one clock cycle. Basic event counters are implemented:

- `cycle` and `cycleh` – these 32-bit registers form a 64-bit value that contains the counted clock cycles since the last reset.
- `time` and `timeh` – these registers shadow the contents of the `TIME` and `TIMEH` registers from the I/O.
- `instret` and `instreh` – these 32-bit registers form a 64-bit value that contains the counted retired instructions since the last reset.

Note that these registers are read-only. Writes are ignored.

Generic registers:

- `mvendorid` – this register is hardwired to all zero bits.
- `marchid` – this register is hardwired to all zero bits.
- `mimpid` – this register is hardwired to all zero bits.
- `mhartid` – this register is hardwired to all zero bits.
- `mconfigptr` – this register is hardwired to all zero bits.
- `misa` – hardwired to value 0x40001100, indicating 32-bit processing, RV32I base ISA and Integer Multiply/Divide extension.

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For trap handling, the following registers are implemented:

- `mstatus` – the only implemented bits are MIE, MPIE and MPP, all other bits are hardwired zero.
- `mie` – for the lower 16 bits, only MTIE is implemented, all other bits are hardwired zero.
- `mtvec` – contains the trap handler (vector) address, can be used in direct and vectored mode.
- `mstatush` – this register is hardwired to all zero bits.
- `mscratch` – currently not used, but can be used by software trap handlers.
- `mepc` – contains the PC at point of trap of the *currently* executing instruction.
- `mcause` – contains the cause of the trap as set forward in “The RISC-V Instruction Set Manual, Volume II: Privileged Architecture”. For local interrupts, additional codes are used.
- `mtval` – contains the address on the address bus when a trap occurs, not always relevant.
- `mip` – contains the pending interrupts. For the lower 16 bits, only MTIP is implemented. The upper 16 bits are used for local interrupts. This register is read-only.
- `mconfigptr` – this register is hardwired to all zero bits.

The `mcounteren` and `mcountinhibit` registers are not implemented, because U-mode is not implemented. The `menvcfg` and `menvcfgh` are not implemented, because only M-mode is implemented.

The trap handler (vector) address must be loaded by software at boot time. Both direct and vectored mode are supported. In direct mode all traps redirect to a single trap handler that has to handle both interrupts and exceptions. The most significant bit of `mcause` is 1 when a trap occurred from an interrupt. In vectored mode, the addresses of *interrupt handlers* are loaded from a jump table. Exceptions are redirected to a single handler. Note that the address of the jump table must be on a 4-byte boundary, and bit 0 of the jump table address has to be set to 1 for vectored mode.

Other CSRs are not implemented. Good synthesizers will remove not-used CSRs.

## 2.10 Local Interrupt Control unit

The Local Interrupt Controller is responsible for selecting which trap request must be serviced by the core. Interrupts have higher priority than exceptions. The state of the serviced trap is visible in the CSR.

The LIC can handle 16 local interrupts (numbered 16 to 31) and the Machine mode external timer interrupt (numbered 7). Other standard RISC-V interrupts (numbered 0

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to 6 and 8 to 15) are not available. The external timer interrupt has the highest priority, followed (currently) by the USART and TIMER1 interrupts.

Exceptions are handled as set forward in Table 3.7 of “The RISC-V Instruction Set Manual, Volume II: Privileged Architecture”: instruction access fault, instruction address misaligned, ECALL (M mode only), EBREAK, load/store address misaligned, load/store access fault. Note that ECALL and EBREAK are user instructions and can be interrupted by an interrupt (i.e. when the ECALL or EBREAK instruction is executing).

## **2.11 Multiply/Divide Unit**

The processor is equipped with a hardware multiply/divide unit. All multiply/divide instructions are supported (MUL, MULH, MULHSU, MULHU, DIV, DIVU, REM, REMU) and the result is fed to the ALU. A multiplication takes three clock cycles (one clock-in, one multiply, one clock-out). For division, two versions are available. By default, the divider needs 19 clocks (one clock-in, 16 divide, one clock-out, one clock-thru) for a division using a poor man’s radix-4 division unit. As an alternative, a simple radix-2 division unit can be selected taking 35 clock cycles (one clock-in, 32 divide, one clock-out, one clock-thru) to do the division. Thus, the radix-4 divider unit is faster, but needs more cells. The radix-2 divider unit is slower, but needs less cells. You have to enable the M-standard support in the compiler. The multiplier uses special DSP units in the Cyclone V. Most regular FPGAs have onboard multipliers. Note that when executing an operation, the pipeline is stalled. Also note that a trap can interrupt the computation, and then the instruction has to be restarted. Selecting the radix-4 division has a minimum impact on the clock speed.

## **2.12 Stack pointer**

The stack pointer is fully implemented although the ISA does not provide pushes and pops. The stack pointer is used to allocate local variables and is updated with each allocation and deallocation. As usual, the stack grows downwards (to lower addresses) on allocations and upwards (to higher addresses) on deallocations. Therefore the stack pointer is set to the highest RAM address + 1 on boot (which is 0x20008000 by default). The ISA postulates that the stack is aligned on 16-byte boundaries for the I standard.

## **2.13 Implemented instructions**

For the processor, all RV32IM Unprivileged instructions are implemented with the exception of the FENCE instruction. This instruction acts as a no-operation. From the privileged instruction, ECALL and EBREAK are supported and execute an exception. MRET is used to return from an exception or an interrupt. WFI is not supported and act as a no-operation (NOP).

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### 3 The FPGA

For this project, we use the Cyclone V FPGA from Intel (formerly Altera). See <https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/v.html>. The used Cyclone V is the 5CEFA4F23C7 which has 18480 ALMs available. It has 3080 kb of onboard RAM bits available which are used for RAM and ROM. Depending on the program and used resources, the compiled RISC-V processor uses about 2900 ALMs (about 15 %) and 786,432 bits of internal memory (25 %). The clock frequency is 80 MHz which is sufficient for all program examples. Note that the DE0-CV board has a onboard clock generator with a frequency of 50 MHz, so a PLL is needed to get a frequency of 80 MHz. This FPGA is mounted on a Terasic DE0-CV board. The board has 10 switches, 4 push buttons, 1 reset push button, 10 leds, and 6 seven-segment displays. It also has two 2x20-pin headers to connect off-board devices. See <http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=921>. For downloading the program file, the onboard USB-Blaster is used.

It is possible to add the Quartus' Signal Tap (embedded) Logic Analyzer. Follow the instructions on [https://people.ece.cornell.edu/land/courses/ece5760/Quartus/Signal\\_tap.html](https://people.ece.cornell.edu/land/courses/ece5760/Quartus/Signal_tap.html). Note that the Signal Tap uses onboard memory.

### 4 Processor hardware

The processor hardware is composed of the following VHDL files:

- `processor_common.vhd` – Common types and constants.
- `processor_common_rom.vhd` – Description of the ROM contents.
- `address_decode.vhd` – The address decoder and data router to the memory
- `core.vhd` – The core contains the PC, the registers, the ALU, the MD unit, the control state machine and the memory interface.
- `rom.vhd` – Description of the ROM. Will be placed in onboard, initialized RAM blocks.
- `ram.vhd` – Description of the RAM. Will be placed in onboard, uninitialized RAM blocks.
- `io.vhd` – Description of the I/O. It contains a 32-bit input register, a 32-bit output register, an USART, a simple timer and the TIME and TIMECMP memory mapped registers.
- `csr.vhd` – Description of the Control and Status registers.
- `lic.vhd` – Description of the Local Interrupt Controller.
- `riscv.vhd` – Top-level description of the processor. Connects all the building blocks to a viable processor.
- `riscv.sdc` – Constraints file. Sets the target clock frequency.

- `tb_riscv.vhd` – VHDL testbench to simulate the design.
- `tb_riscv.do` – QuestaSim/Modelsim command script.

In the file `processor_common.vhd`, a number of constant parameters are available:

- `SYSTEM_FREQUENCY` – Set to 50 MHz. Change this if you use a PLL with a different frequency.
- `CLOCK_FREQUENCY` – Set to 1 MHz. Used to calibrate the internal clock. The compiler assumes 1 MHz and some library functions depend on it.
- `NUMBER_OF_REGISTERS` – Set to 32 for I standard. Set to 16 for E standard.
- `HAVE_MULDIV` – Set to TRUE, MD unit is included. Set to FALSE to exclude MD unit. Note that you must not specify the M options while compiling software.
- `FAST_DIVIDE` – Set to TRUE to use the radix-4 divider. Set to FALSE to use the radix-2 divider.
- `VECTORED_MTVEC` – Set to TRUE to provide vectored interrupts. You still have to set bit 0 to 1 in `mtvec` CSR. You can still use direct mode. Set to FALSE to only use direct interrupts.
- `MSTATUS_MIE_DISABLES_INTERRUPTS` – Set to TRUE to only disable interrupts when `mstatus.MIE` is 0. Set to FALSE to disable all traps (so including exceptions and when `mstatus.MIE` is 0).

## 4.1 Pin assignments

The pin assignments for the DE0-CV board are as follows (Table 2). Note that not all signals are assigned to a pin, in which case the fitter will assign a suitable pin.

**Table 2:** *Pin assignments for the DE0-CV board.*

Signal	Pin Name	Comments
<code>clk</code>	M9	System clock
<code>areset</code>	P22	Asynchronous, active low, reset
<code>RxD</code>	N19	USART receive, on GPIO0
<code>TxD</code>	P19	USART transmit, on GPIO0
<code>pina[31]</code>	—	Fitter assigned
<code>pina[30]</code>	—	Fitter assigned
<code>pina[29]</code>	—	Fitter assigned
<code>pina[28]</code>	—	Fitter assigned
<code>pina[27]</code>	—	Fitter assigned
<code>pina[26]</code>	—	Fitter assigned
<code>pina[25]</code>	—	Fitter assigned
<code>pina[24]</code>	—	Fitter assigned
<code>pina[23]</code>	—	Fitter assigned

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<b>Signal</b>	<b>Pin Name</b>	<b>Comments</b>
pina[22]	—	Fitter assigned
pina[21]	—	Fitter assigned
pina[20]	—	Fitter assigned
pina[19]	—	Fitter assigned
pina[18]	—	Fitter assigned
pina[17]	—	Fitter assigned
pina[16]	—	Fitter assigned
pina[15]	M6	KEY3
pina[14]	M7	KEY2
pina[13]	W9	KEY1
pina[12]	U7	KEY0
pina[11]	—	Fitter assigned
pina[10]	—	Fitter assigned
pina[9]	AB12	SW9
pina[8]	AB13	SW8
pina[7]	AA13	SW7
pina[6]	AA14	SW6
pina[5]	AB15	SW5
pina[4]	AA15	SW4
pina[3]	T12	SW3
pina[2]	T13	SW2
pina[1]	V13	SW1
pina[0]	U13	SW0
pouta[31]	—	Fitter assigned
pouta[30]	U22	HEX16
pouta[29]	AA17	HEX15
pouta[28]	AB18	HEX14
pouta[27]	AA18	HEX13
pouta[26]	AA19	HEX12
pouta[25]	AB20	HEX11
pouta[24]	AA29	HEX10
pouta[23]	—	Fitter assigned
pouta[22]	AA22	HEX06
pouta[21]	Y21	HEX05
pouta[20]	Y22	HEX04
pouta[19]	W21	HEX03
pouta[18]	W22	HEX02
pouta[17]	V21	HEX01
pouta[16]	U21	HEX00
pouta[15]	—	Fitter assigned
pouta[14]	—	Fitter assigned
pouta[13]	—	Fitter assigned

*Continued on next page*

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Signal	Pin Name	Comments
pouta[12]	—	Fitter assigned
pouta[11]	—	Fitter assigned
pouta[10]	—	Fitter assigned
pouta[9]	L1	LEDR9
pouta[8]	L2	LEDR8
pouta[7]	U1	LEDR7
pouta[6]	U2	LEDR6
pouta[5]	N1	LEDR5
pouta[4]	N2	LEDR4
pouta[3]	Y3	LEDR3
pouta[2]	W2	LEDR2
pouta[1]	AA1	LEDR1
pouta[0]	AA2	LEDR0

## 4.2 Simulation

The designs can be simulated fully, using QuestaSim Intel Starter or ModelSim Intel Starter. You need a (free) license for QuestaSim. During simulation, all essential signals can be viewed, as is the RAM. The RAM is viewed as 32-bit entries, so we need to do some manual calculations to correctly find byte, half word and word accesses. Simulation can be started from Quartus.

## 5 Cloning the RISC-V project

Now we have to clone the RISC-V project. It incorporates the full Quartus Prime Lite project with the processor written in VHDL. It also incorporates some simple C program examples and a taylor-made program to convert a RISC-V executable to a VHDL table suitable for the ROM. Create a working directory (and change to that directory) and issue the command:

```
1 git clone https://github.com/jesseopdenbrouw/riscv-minimal
```

In the created directory, you will see the following directories:

CODE – Sample software programs, linker script and startup files

DOCS – Documentation

HARDWARE – the VHDL descriptions

OLD – yes, really old files for backup

RETIRED – Descriptions that are not used anymore

Change directory to CODE. Make sure the RISC-V C compiler is available (see Section 6) and is in your path environment variable. Now enter the command `make`. It will compile all programs and the taylor-made conversion program. To clean up the programs, issue the command `make clean`.



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If you want, you can compile the processor with the standard program incorporated, which is by default, flashing onboard leds and writing the current time since last reset via the USART at 9600 bps. Start your Quartus Prime Lite software and open the project in the `HARDWARE` directory. Now start a build by clicking on the play-symbol. It should compile a standard setting (this takes a long time). When finished, you can download the FPGA contents to the DE0-CV board.

To test one of the programs, change directory to one of the directories in `CODE` and copy the file with `.vhd` extension to the directory containing the VHDL description under the name `processor_common_rom.vhd`. Now start Quartus and start the compilation. After a successful compilation, you can program the Cyclone V on a DE0-CV board.

The design is targeted for a clock speed of 80 MHz. This is a minimum requirement. Depending on how “good” the device is fabricated, higher clock speeds may be obtained. With one device, we could speed up the clock to 152 MHz.

Compilation of the hardware design is independent of the size of the software program. Several design goals may be selected, such as highest clock speed, minimum power or minimum area. Depending on the compilation settings, compilation time may decrease or increase.

## 6 Setting up the GNU C compiler for *this* RISC-V

The processor can run C and C++ programs that are compiled using the GNU C/C++ compiler for RISC-V. Besides that, a separate linker script and startup file are needed to setup the compiled code. It is possible to set up the C library for multiple RISC-V architecture versions and select a version during compilation. Building the C/C++ compiler (from Linux) is straightforward:

1. You need a current GNU C/C++ compiler installed on your Linux box. You also need all essential building tools:

```
1 apt install autoconf automake autotools-dev curl python3 ↵  
    ↵ libmpc-dev libmpfr-dev libgmp-dev gawk build-essential ↵  
    ↵ bison flex texinfo gperf libtool patchutils bc zlib1g ↵  
    ↵ -dev libexpat-dev
```

2. You need the texinfo package. On Ubuntu et al. issue

```
1 apt install texinfo
```

3. In your home directory, enter the command

```
1 git clone --recursive https://github.com/riscv/riscv-gnu- ↵  
    ↵ toolchain
```

4. Wait for the cloning to end (takes a long time, about 30 minutes on a Zbook G5 2020 with a 10 MB/s internet connection)

5. Change to the directory with

```
1 cd riscv-gnu-toolchain
```

6. Make the build directory with:

```
1 mkdir build; cd build
```

7. Check the current configuration with

```
1 ../configure --help | grep abi
```

It should say:

```
1 --with-abi=lp64d      Sets the base RISC-V ABI, defaults to ↵  
    ↵lp64d
```

The toolchain is currently configured for 64-bit RISC-V. That is not what we want.

8. Enter:

```
1 ../configure --prefix=/opt/riscv32 --with-arch=rv32im --↵  
    ↵with-abi=ilp32 --with-multilib-generator="rv32i-ilp32↵  
    ↵--;rv32e-ilp32e--"
```

This will set the default architecture to RV32IM, with options for RV32I and RV32E (reduced registers), and the ABI to ilp32 and ilp32e (reduced registers). This means that integers, long integers and pointers use 32-bit entities. The destination directory is /opt/riscv32.

9. Now enter the make command as root: make

MAKE SURE TO ENTER THIS COMMAND AS root, because the toolchain is put in /opt/riscv32. This takes a long time (about 45 minutes on a Zbook G5). At some points the compilation seems to hang, but it is just compiling complicated C-files. By the way, you will see a lot of warnings.

10. Now that the toolchain is setup, we have to put the path into the \$PATH environment variable so enter

```
1 export PATH=/opt/riscv32/bin:$PATH
```

11. Check if the compiler is available:

```
1 riscv32-unknown-elf-gcc -v
```

It should say something like:

```
1 Using built-in specs.  
2 COLLECT_GCC=riscv32-unknown-elf-gcc  
3 COLLECT_LTO_WRAPPER=/opt/riscv32/libexec/gcc/riscv32-↵  
    ↵unknown-elf/11.1.0/lto-wrapper  
4 Target: riscv32-unknown-elf
```

```

5 Configured with: /mnt/d/PROJECTS/riscv-gnu-toolchain/build
  ↪../riscv-gcc/configure --target=riscv32-unknown-elf ↪
  ↪--prefix=/opt/riscv32 --disable-shared --disable-
  ↪threads --enable-languages=c,c++ --with-system-zlib --
  ↪enable-tls --with-newlib --with-sysroot=/opt/riscv32/
  ↪riscv32-unknown-elf --with-native-system-header-dir=/
  ↪include --disable-libmudflap --disable-libssp --
  ↪disable-libquadmath --disable-libgomp --disable-nls --
  ↪disable-tm-clone-registry --src=../riscv-gcc --
  ↪enable-multilib --with-multilib-generator='rv32i-ilp32
  ↪--;rv32e-ilp32e--' --with-abi=ilp32 --with-arch=rv32i
  ↪--with-tune=rocket 'CFLAGS_FOR_TARGET=-Os -mcmmodel=
  ↪medlow' 'CXXFLAGS_FOR_TARGET=-Os -mcmmodel=medlow'
6 Thread model: single
7 Supported LTO compression algorithms: zlib
8 gcc version 11.1.0 (GCC)

```

## 6.1 Register subset

It is possible to compile the toolchain to only use register x0 to x15. This is called the RISC-V E extension. As a positive side effect, the register file can be cut down from 32 registers to 16 registers, saving 512 memory element. This will lower the ALM (cell) count and possible speed up the device. A negative side effect is that the pressure on register allocation is higher, possibly increasing instruction count when saving registers on the stack.

Using the above recipe, the toolchain is set up for both RV32I and RV32E. You need the specify the architecture and ABI during compile time of the RISC-V programs.

Now compile a C program with:

```

1 riscv32-unknown-elf-gcc -O2 -g -o flash flash.c -Wall -T ↪
  ↪ldfiles/riscv.ld -march=rv32e -mabi=ilp32e -nostartfiles --↪
  ↪specs=nano.specs ../crt/startup.c

```

Make sure to use `-march=rv32e` and `-mabi=ilp32e`.

## 7 Compiling a C program by hand

We tested a large amount of programs with and without trap handling. We tested all I/O. We did test the use of the C library (`malloc` et al, floats and double calculation, some trigonometry functions from the mathematical library), but more tests are needed.

Compiling a program requires the following steps:

- In the program directory CODE, create a new directory and change to that directory.
- Create a C program file, we assume `flash.c`.

- Now issue the command:

```
1 riscv32-unknown-elf-gcc -O2 -g -o flash flash.c -Wall -T ↵
    ↵ ../ldfiles/riscv.ld -march=rv32i -nostartfiles --specs ↵
    ↵ =nano.specs ../crt/startup.c
```

We supply our own linker file (-T ../ldfiles/riscv.ld) and we supply our own startup file (../crt/startup.c). Make sure to use -nostartupfiles ↵ ↵ otherwise the default startup file will be linked and errors will report. There are three startup files:

- empty.S – Empty startup file only providing the entry symbol. Can be used with assembler programs.
- minmal.S – Provides the entry symbol, loads the global pointer and stack pointer. Can be used with assembler programs.
- startup.S – Provides the entry symbol, loads the global pointer and stack pointer and calls main. On return of main, it waits in an endless loop. Can be used with minimalistic C programs.
- startup.c – Full support for C programs. Can be used with malloc et al.

- Next issue the command:

```
1 riscv32-unknown-elf-objcopy -O srec flash flash.srec
```

This will create an S-record file in Motorola hex-format.

- Next issue the command:

```
1 ../bin/srec2vhd1 -wf flash.srec flash.vhd
```

This will create a VHDL file with the ROM encoded as 32-bit Little Endian quantities. Note: the taylor-made srec2vhd1 has to be compiled before. See Section 5.

- Next issue the command:

```
1 cp flash.vhd ../../HARDWARE/riscv-pipe-csr-md-lic/ ↵
    ↵ processor_common_rom.vhd
```

This will copy the VHDL file to the RISC-V processor ROM file.

- Now start the compilation of the VHDL code in Quartus Prime Lite and program the compiled file. This file has the extension .sof. See Figures 5 to 7.

## 8 Implemented system calls

The sbrk/brk system call, used for allocating RAM memory, is implemented. Note that there is a limited amount of RAM. Note that sbrk is not called by the user. Use malloc et al.

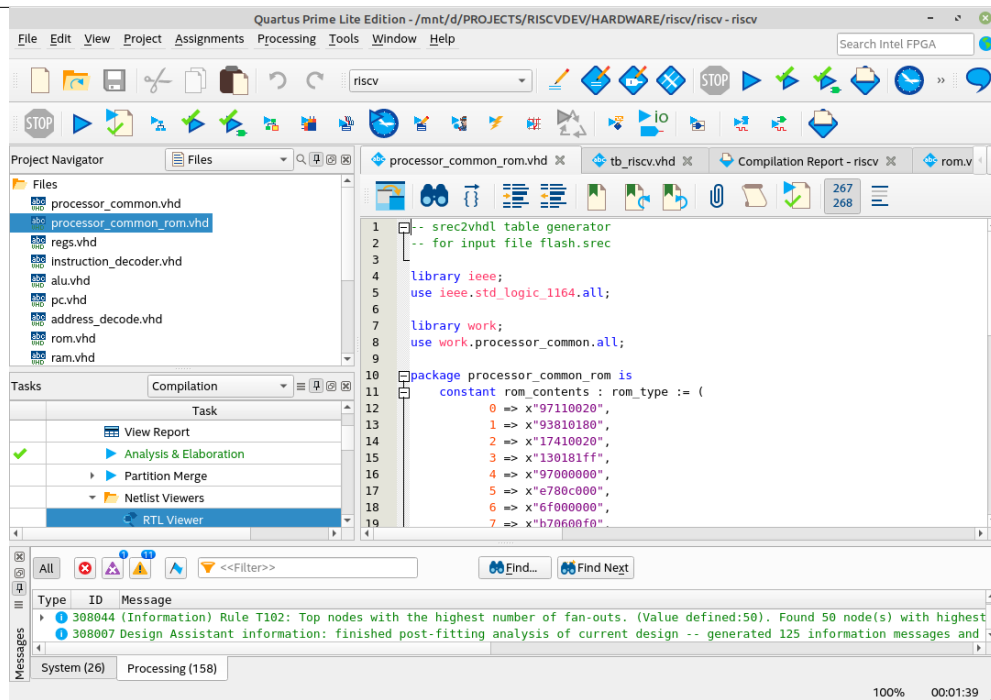


Figure 5: Image of the Quartus project (1).

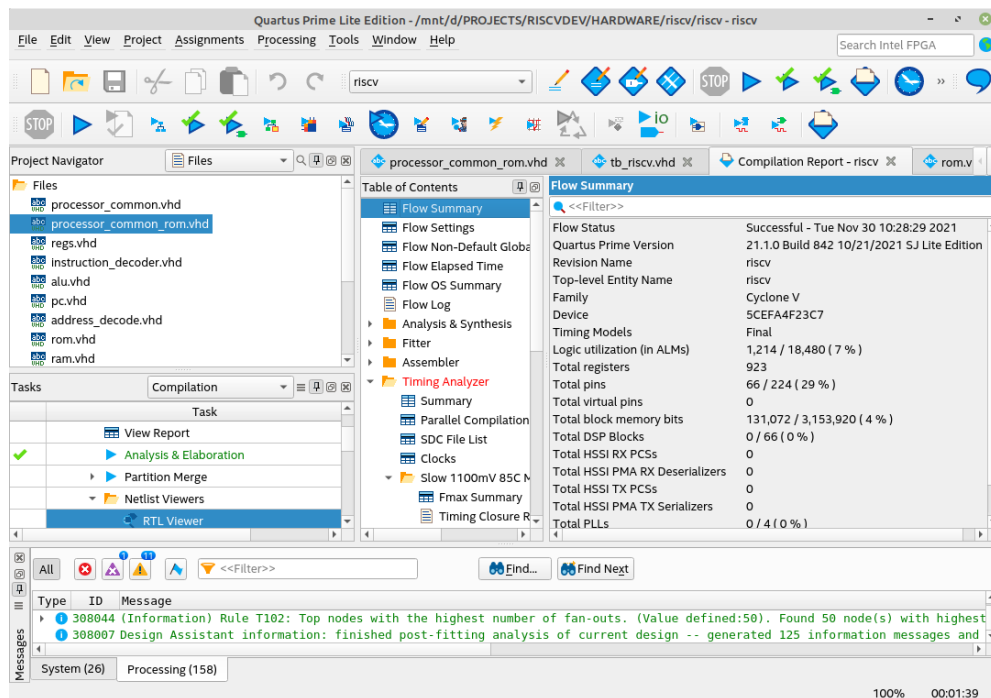
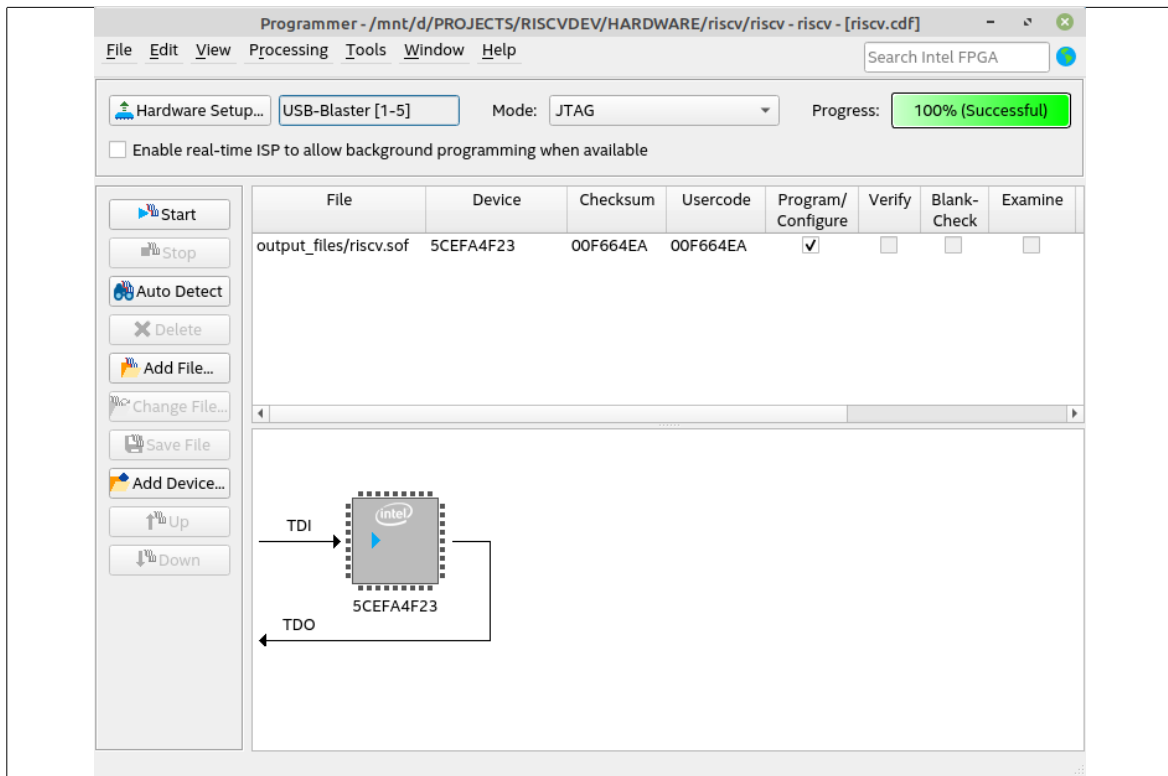


Figure 6: Image of the Quartus project (2).

The `gettimeofday` system call is implemented. It returns the seconds and microseconds since the last reset of the processor. You need to call the `gettimeofday` C function for proper handling.

The `times` system call is implemented, but only for non-trap system calls. When using



**Figure 7:** Image of the programmer.

trapped systems calls (using ECALL), `gettimeofday` is used.

The read and write system calls are implemented but in turn they call the userland functions `__io_getchar` and `__io_putchar` functions to read or write a character. Normal use is for the latter two to transmit or receive via the USART. When implemented, `printf` and `scanf` can be used.

Other system calls return an error because they cannot fulfill the requested operation, such as `open`. Note that some system calls are in fact not implemented and return undetermined behavior.

Note: when using traps, the system calls are handled by a trap handler (by using ECALL). This is the default behavior of the tool chain. When not using traps, the system calls are rerouted to functions in a library. You need to set up your software properly. See the software examples.

## 9 Using trap handlers in software

We provide (see software examples `interrupt_direct` and `interrupt_vectored`) a basic implementation of trap handlers. The `universal_handler` handles all traps (interrupts and exceptions) in direct mode. The entry point (the address loaded in the `mtvec` CSR) must be set in the main function, as is enabling traps. In vectored mode, interrupts are redirected to their own handlers via a jump table. The start address of

---

---

the jump table must be set in the main function, and traps must be enabled. The external timer has its own handler called `external_timer_handler`. TIMER1 has its own handler called `timer1_cmpt_handler`. The USART has its own handler called `usart_handler`. This handler is used for both receive and transmit interrupts. Note that negating the interrupt request must be done by software in the respective handlers. The interrupt requests are *not* negated by hardware. Note: the external timer interrupt has to be enabled by writing a 1 to `mie.MTIE`.

## 10 Software programs

In the `CODE` directory, there are a number of software programs available. First, the common files:

- `ldfiles` – contains the linker script. There is one script:
  - `riscv.ld` – default linker script: ROM = 64 kB, RAM = 32 kB, I/O = 16 kB.
- `crt` – contains the startup files.
- `bin` – contains the binary of `srec2vhd1`.

Some examples are to be used in the simulator only, mainly to test functionality on clock cycle accuracy. Some examples work on the DE0-CV board, but without testing traps. Two examples work on the board and use traps.

- `add64` – simple 64-bit addition. For use in the simulator.
- `assembler` – a simple assembler program. For use in the simulator.
- `base1_problem` – a program that calculates the sum of the inverses of the squares of natural numbers, up to 1000. For use in the simulator. Used to test the divider.
- `clock` – a simple clock using the CSR TIME and TIMEH registers to fetch the time since last reset. Works on the board.
- `double` – some floating point double computations. For simulation.
- `exp` – calculates Euler's number  $e$ . For simulation.
- `flash` – flash the DE0-CV board leds, works on the board.
- `float` – some floating point float computations. For simulation.
- `global` – test for globals and local statics with initialization. For simulation
- `hex_display` – program that reads 8 switches from the board and display them as a 2-digit hexadecimal value on the 7-segment display. Works on the board. Note that on the DE0-CV board, the decimal points cannot be used, because they are not connected to FPGA pins.
- `interrupt_direct` – program to test the interrupt handling using direct mode. Works on the board.

- `interrupt_vector` – program to test the interrupt handling using vectored mode. Works on the board.
- `interval` – program that uses the `clock` C library function to time 5 seconds since last read. Uses the USART. Works on the board.
- `ioadd` – adds the lower 5 switches to the upper 5 switches and displays the result on the leds. Tests addition, shifting and I/O. Works on the board.
- `malloc` – example to test `malloc` and friends. Works. Used in simulations.
- `monitor` – simple monitor program. Works on the board. Uses strings, USART, RAM, ROM, I/O and `sprintf` (and therefore `malloc` et al.).
- `mult` – integer multiplication with the hardware `md` unit or by C library. Depends on the compiler settings. For simulations.
- `qsort_int` – sorts an integer array using the `qsort` C library function. Works in simulation.
- `riemann_left` – calculates the Riemann Left Sum of  $\sin^2 x$  from 0 to  $2\pi$ . For use in the simulator. The result must be  $\pi$ .
- `shift` – shifts. For use in simulations.
- `sprintf` – prints integers, floats/doubles to a string. This is a big binary. For simulations.
- `string` – some string functions. For simulations.
- `syscalls` – implementing common system calls without traps.
- `testio` – simple program that copies the input (switches) to the output (leds) (works on the board).
- `trig` – some float trigonometry functions. For simulations.
- `uart` – simple USART program. Works on the board.
- `uart_cpp` – simple C++ USART program. Makes use of a singleton design pattern. Uses a lot of ROM. Works on the board. This is a big binary.
- `uart_printf` – simple program that prints an integer, a pointer, a float and a double to the terminal using `printf`, this is a big binary. Works on the board.
- `uart_sprintf` – simple program that prints an integer, a pointer, a float and a double to the terminal, this is a big binary. Works on the board.

Note: we use a lot of the `volatile` keyword to emit the variables to RAM for easy inspection. You will see compiler warnings from C library functions.

Note that the floating point programs loads (huge) functions from the C library and possibly creates a binary that is too large to fit in the ROM. In that case, the linker will issue an error and does not build the binary. You have to update the data sizes in the VHDL description and update the linker script with suitable data sizes.



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When using floats and doubles in `sprintf/printf`, you need to supply the linker with the `-u _printf_float` option. When using floats and doubles in `sscanf/scanf`, you need to supply the linker with the `-u _scanf_float` option. Also, using `printf` and `scanf` create big binaries.

## 10.1 srec2vhd1

This is a homebrew utility to convert a Motorola S-record file into a VHDL file suitable for inclusion of the processor. The program is called with:

```
1 srec2vhd1 [-fbwhqv0] [-i <arg>] inputfile [outputfile]
```

`inputfile` is the S-record file, created by the `objdump` program. `outputfile` is the VHDL output file. When omitted, `stdout` is used. There are a number of options:

- `-f` makes a full output that directly can be used. If not used, only the ROM table contents itself is produced.
- `-w` ROM contents is in words (32 bits).
- `-h` ROM contents is in half words (16 bits).
- `-b` ROM contents is in bytes (8 bits).
- `-v` Verbose output.
- `-0` Output unused ROM data as 0 instead of don't care.
- `-q` Quiet output, only error messages are displayed.
- `-i <arg>` indents each line with `<arg>` spaces.

Note: uninitialized ROM contents is emitted as don't care, except when the `-0` option is used. Don't cares are set to 0 by Quartus on default.

## 10.2 Monitor program

A simple monitor program is available, see the `monitor` directory in software examples. It makes use of the USART. You need a terminal program like Putty and a USART to USB device for your computer. Currently the following commands are available:

- `l` – set Little Endian (default),
- `b` – set Big endian.
- `rw <address>` – read word at address (4-byte boundary),
- `rh <address>` – read half word at address (2-byte boundary),
- `rb <address>` – read byte at address,
- `ww <address> <data>` – write word at address (4-byte boundary),
- `wh <address> <data>` – write half word at address (2-byte boundary),

- `wb <address> <data>` – write byte at address,

`<address>` and `<data>` in hexadecimal and Big Endian format. For ROM and RAM read accesses, best set to Little Endian. For I/O accesses, set Big Endian. Make sure to read and write I/O as words. Note that ROM cannot be written.

## 11 Address ranges and memory sizes

By default, the ROM starts at address 0x00000000 and has a size of 64 kB (16 k words). The Program Counter starts at address 0x00000000. The RAM starts at address 0x20000000 and has a size of 32 kB (8 k words). The stack pointer is set to one address above the last RAM byte, by default at 0x20008000. The I/O starts at address 0xF0000000 and has a size of 16 kB (4 k words).

The ROM, RAM and I/O may be moved to another start location. The Program Counter is started at the correct address. The placement of the ROM is in 256 MB intervals, which are the 4 most significant bits of a 32-bit address. The same holds for the RAM and the I/O. To move the ROM, open the VHDL file `processor_common.vhd` and go down to the end of the file. There you will see the following lines:

```
1  -- The highest nibble (4 bits) of the ROM, RAM and I/O
2  -- This will set the memories at 256 MB intervals
3  constant rom_high_nibble : std_logic_vector(3 downto 0) := x"0";
4  constant ram_high_nibble : std_logic_vector(3 downto 0) := x"2";
5  constant io_high_nibble  : std_logic_vector(3 downto 0) := x"F";
```

Change the start locations of the memories by changing the constants. Make sure the memories do not overlap. To change the sizes of the memory, look for the lines as shown below:

```
1  -- The ROM
2  -- NOTE: the ROM is word (32 bits) size.
3  -- NOTE: data is in Little Endian format (as by the toolchain)
4  --         for half word and word entities
5  --         Set rom_size_bits as if it were bytes
6  -- NOTE: rom_size_bits must be <= 16
7  constant rom_size_bits : integer := 16;
8  constant rom_size      : integer := 2**(rom_size_bits-2);
9  type rom_type is array(0 to rom_size-1) of data_type;
10 -- The contents of the ROM is loaded by processor_common_rom.vhd
11
12 -- The RAM
13 -- NOTE: the RAM is 4x byte (8 bits) size, supporting
14 --         32-bit Big Endian storage,
15 --         so we have to recode to support Little Endian.
16 --         Set ram_size_bits as if it were bytes
17 -- NOTE: ram_size_bits must be <= 16
```

```

18 constant ram_size_bits : integer := 15;
19 constant ram_size : integer := 2**(ram_size_bits-2);
20 -- The type of the RAM block, there are 4 blocks instantiated
21 type ram_type is array (0 to ram_size-1) of std_logic_vector(7 ↵
    ↵ downto 0);
22
23 -- The I/O
24 -- NOTE: the I/O is word (32 bits) size, Big Endian
25 --       there is no need to recode the data
26 --       The I/O can only handle word size access
27 --       Set io_size_bits as if it were bytes
28 constant io_size_bits : integer := 8;
29 constant io_size : integer := 2**(io_size_bits-2);
30 type io_type is array (0 to io_size-1) of data_type;

```

Note that you also have to make changes to the linker script. In the file `riscv.ld`, at the top you will find the following lines. Change the origins in accordance with the VHDL description.

```

1 ENTRY( _start )
2
3 MEMORY
4 {
5     ROM (rx)      : ORIGIN = 0x00000000, LENGTH = 64K
6     RAM (rw)      : ORIGIN = 0x20000000, LENGTH = 32K
7     IO (rw)       : ORIGIN = 0xf0000000, LENGTH = 16K
8 }

```

In this setting, the ROM is 64 kB long and the RAM is 32 kB long. Please note that both ROM and RAM bits may not exceed 3,153,920 bits of onboard RAM. For increased ROM and RAM size, typical values may be 128 kB ROM and 64 kB RAM.

Note that we do not use full address decoding for ROM, RAM and I/O. This means that, for example, the ROM is visible multiple times in the address space. This is called *memory foldback*. For the ROM this is at 64 kB intervals. So the contents of address 0x00000000 is also available at address 0x00010000.

## 12 Future plans (or not) and issues

Some future plans:

- We are *not* planning the C standard.
- Plans to create a hardcoded bootloader to load programs when the processor is loaded in an FPGA. We need to modify the instruction fetch hardware and the ROM ports, because we have to write the ROM. Instructions can currently only be fetched from ROM.

- We strive to implement SPI and I2C, and PWM. I2C is a bit of a problem, because it uses one data line to transfer data (i.e. bidirectional).
- Implement an I/O input/output multiplexer for `pina` and `pouta`. This will enable I/O functions to be multiplexed with normal port I/O.
- Implement Supervisor Mode (this will take some time ;-)).
- Smaller (in cells) divide unit.
- Test more functions of the standard and mathematical libraries. Now only a few functions are tested.
- It is not possible to print `long long` (i.e. 64-bit) using `printf` et al. When using the format specifier `%lld`, `printf` just prints `ld`. This due to lack of support in the `nano` library.
- Further optimize the ALU for size and speed. The ALU is single-cycle and determines the maximum clock speed (in some constraints, the CSR is slower).
- The `time` (`TIMEH:TIME`) registers are currently read only, but should be writable.
- We were considering a five-stage pipeline, but because loads take two clock cycles, we abandoned that thought. Furthermore, adding extra stages would complicate the forward logic thereby increasing the latency of the execute stage. At this point, the ALU has the greatest latency.

## A Port I/O

The processor is equipped with a single 32-bit input and 32-bit output port. There is no data direction register. The reason for this is that the tri-state buffers for bi-direction must be in the top-level entity of the hardware design, making it impossible to use the processor in a greater design. Note that all accesses on the I/O are in Big Endian. This means that bit 31 of the input will be placed in bit 31 of the used variable.

The I/O registers are directly addressable or by a struct. See the listing below.

```

1 #ifndef _IO_H
2 #define _IO_H
3
4 #include <stdint.h>
5
6
7 /* Base address of the I/O */
8 #define IO_BASE (0xf0000000UL)
9
10 /* General purpose I/O */
11 #define GPIOA_PIN  (*(volatile uint32_t*) (IO_BASE+0x00000000UL))
12 #define GPIOA_POUT (*(volatile uint32_t*) (IO_BASE+0x00000004UL))
13
```

```

14 typedef struct {
15     volatile uint32_t PIN;
16     volatile uint32_t POUT;
17 } GPIO_struct_t;
18
19 #define GPIOA_BASE (IO_BASE+0x00000000UL)
20
21 #define GPIOA ((GPIO_struct_t *) GPIOA_BASE)
22
23
24 /* USART (USART1) */
25 #define USART_DATA (*(volatile uint32_t*) (IO_BASE+0x00000020UL))
26 #define USART_BAUD (*(volatile uint32_t*) (IO_BASE+0x00000024UL))
27 #define USART_CTRL (*(volatile uint32_t*) (IO_BASE+0x00000028UL))
28 #define USART_STAT (*(volatile uint32_t*) (IO_BASE+0x0000002CUL))
29
30 typedef struct {
31     volatile uint32_t DATA;
32     volatile uint32_t BAUD;
33     volatile uint32_t CTRL;
34     volatile uint32_t STAT;
35 } USART_struct_t;
36
37 #define USART_BASE (IO_BASE+0x00000020UL)
38
39 #define USART ((USART_struct_t *) USART_BASE)
40
41
42 /* TIMER (TIMER1) */
43 typedef struct {
44     volatile uint32_t CTRL;
45     volatile uint32_t STAT;
46     volatile uint32_t CNTR;
47     volatile uint32_t CMPT;
48 } TIMER_struct_t;
49
50 #define TIMER1_BASE (IO_BASE+0x00000080UL)
51 #define TIMER1 ((TIMER_struct_t *) TIMER1_BASE)
52
53
54 /* RISC-V system timer (in I/O) */
55 #define TIME (*(volatile uint32_t*) (IO_BASE+0x000000f0UL))
56 #define TIMEH (*(volatile uint32_t*) (IO_BASE+0x000000f4UL))
57 #define TIMECMP (*(volatile uint32_t*) (IO_BASE+0x000000f8UL))
58 #define TIMECMPPH (*(volatile uint32_t*) (IO_BASE+0x000000fcUL))

```

```

59
60 typedef struct {
61     volatile uint32_t time;
62     volatile uint32_t timeh;
63 } TIME_struct_t;
64
65 typedef struct {
66     volatile uint32_t timecmp;
67     volatile uint32_t timecmph;
68 } TIMECMP_struct_t;
69
70 #endif

```

To read the inputs, use:

```

1 uint32_t input;
2
3 input = GPIOA->PIN;

```

To set the outputs, use:

```

1 uint32_t output = 0xff00ff00;
2
3 GPIOA->POUT = output;

```

Modifying bits of a I/O register must be done by a read-modify-write cycle. This is *not* atomically handled and can interfere with interrupts! For example, to set bit 2 of POUT, use:

```

1 GPIOA->POUT |= 0x04;

```

## B USART Code

The USART can send and receive data with one start bit, 7/8/9 data bits, N/E/O parity and 1 or 2 stop bits. Transmission is tested with a baud rate of 9600 bps, 115200 bps and 230400 bps. Send and receive speeds are equal as is the number of data bits, parity and the number of stop bits. There are no auxiliary control signals (e.g. RTS and CTS). There is no embedded FIFO to buffer incoming data. The USART is programmable using I/O registers, see Appendix E. Note that using a system frequency of 50 MHz, the baud rate cannot be lower than 763 bps, because the baud rate generator uses a 16-bit number.

To initialize the USART, use the code in the listing below:

```

1 /* Frequency of the DE0-CV board */
2 #define F_CPU (50000000UL)
3 /* Transmission speed */
4 #define BAUD_RATE (9600UL)
5

```

---

---

```

6  /* Initialize the Baud Rate Generator */
7  void usart_init(void)
8  {
9      /* Set baud rate generator */
10     USART->BAUD = F_CPU/BAUD_RATE-1;
11 }

```

To send a single character with waiting, use the code in the listing below:

```

1  /* Send one character over the USART */
2  void usart_putc(int ch)
3  {
4      /* Transmit data */
5      USART->DATA = (uint8_t) ch;
6
7      /* Wait for transmission end */
8      while ((USART->STAT & 0x10) == 0);
9  }

```

To send a null-terminated string, use the code in the listing below:

```

1  /* Send a null-terminated string over the USART */
2  void usart_puts(char *s)
3  {
4      if (s == NULL)
5      {
6          return;
7      }
8
9      while (*s != '\0')
10     {
11         usart_putc(*s++);
12     }
13 }

```

To wait for a character reception, use the code in the listing below:

```

1  /* Get one character from the USART in
2   * blocking mode */
3  int usart_getc(void)
4  {
5      /* Wait for received character */
6      while ((USART->STAT & 0x04) == 0);
7
8      /* Return 8-bit data */
9      return USART->DATA & 0x000000ff;
10 }

```

---

---

To receive a string from the USART, including some simple line editing, use the code in the listing below:

```
1  /* Gets a string terminated by a newline character from usart
2  * The newline character is not part of the returned string.
3  * The string is null-terminated.
4  * A maximum of size-1 characters are read.
5  * Some simple line handling is implemented */
6  int usart_gets(char buffer[], int size) {
7      int index = 0;
8      char chr;
9
10     while (1) {
11         chr = usart_getc();
12         switch (chr) {
13             case '\n':
14                 case '\r': buffer[index] = '\0';
15                             usart_puts("\r\n");
16                             return index;
17                             break;
18                 /* Backspace key */
19                 case 0x7f:
20                 case '\b': if (index>0) {
21                             usart_putc(0x7f);
22                             index--;
23                         } else {
24                             usart_putc('\a');
25                         }
26                         break;
27                 /* control-U */
28                 case 21: while (index>0) {
29                             usart_putc(0x7f);
30                             index--;
31                         }
32                         break;
33                 /* control-C */
34                 case 0x03: usart_puts("<break>\r\n");
35                             index=0;
36                             break;
37                 default: if (index<size-1) {
38                             if (chr>0x1f && chr<0x7f) {
39                                 buffer[index] = chr;
40                                 index++;
41                                 usart_putc(chr);
42                             }
43                             } else {
```



```

44         usart_putc('\a');
45     }
46     break;
47 }
48 }
49 return index;
50 }

```

When printing a C newline, you have to use:

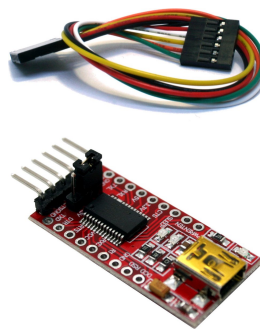
```

1 usart_puts("\r\n");

```

This will set the cursor to the beginning of a new line. Here, `\r` returns the cursor to the beginning of the current line and `\n` advances the cursor to the next line. Some terminal emulation programs can be instructed to move to the beginning of a new line with only `\n`.

For working with the USART on board of the processor, you need an USB-to-USART device with TTL (3.3 V) converter. An example is shown in Figure 8.



**Figure 8:** An USB-to-USART converter. Make sure that the voltages do not exceed 3.3 V.

## C TIMER1 code

Based on a frequency of 50 MHz, the following code will set TIMER1 interrupt on 0,5 s intervals:

```

1 /* Activate TIMER1 with a cycle of 2 Hz */
2 /* for a 50 MHz clock. Use interrupt. */
3 TIMER1->CMPT = 24999999;
4 /* Bit 0 = enable, bit 4 is interrupt enable */
5 TIMER1->CTRL = (1<<4) | (1<<0);

```

## D The external time registers

The time registers (TIME, TIMEH, TIMECMP and TIMECMPH) can be accessed via the I/O and are therefore memory mapped. These registers are shadowed by the CSR. The

---

---

following code reads in the current time and increments the compare registers with a certain *delta*. Whenever TIMEH:TIME is greater than or equal to TIMEH:TIME, an interrupt request is asserted. Negating the interrupt request is accomplished by writing a value greater than the time registers to the compare registers.

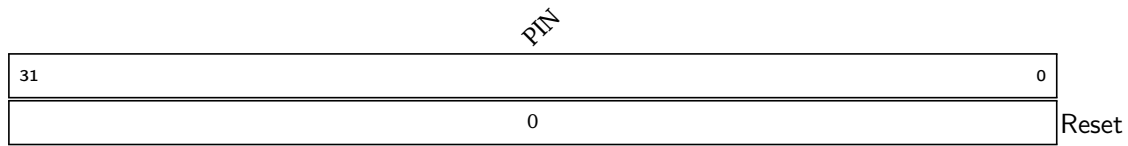
```
1 include "io.h"
2
3 register uint32_t time;
4 register uint32_t timeh;
5
6 /* Fetch current time */
7 do {
8     timeh = TIMEH;
9     time = TIME;
10 } while (timeh != TIMEH);
11
12 /* Fetch current time */
13 register uint64_t cur_time;
14 cur_time = ((uint64_t)timeh << 32) | (uint64_t)time;
15
16 /* Add delta */
17 cur_time += external_timer_delta;
18
19 /* Set TIMECMP to maximum */
20 TIMECMPH = -1;
21 TIMECMP = -1;
22
23 /* Store new TIMECMP */
24 TIMECMP = (uint32_t)(cur_time & 0xffffffff);
25 TIMECMPH = (uint32_t)(cur_time>>32);
```

Normally, this code is placed in the interrupt handler. These registers are read-only shadowed to the CSR time registers.

## E I/O registers

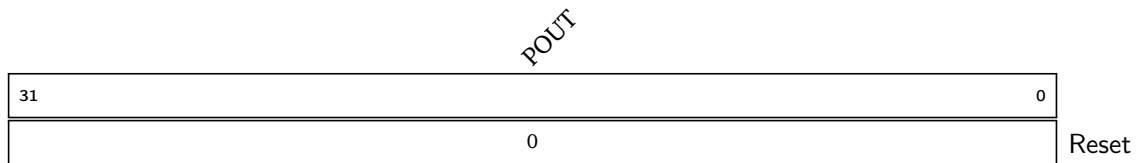
This is a list of currently supported I/O addresses. The default start address is 0xF0000000. The offset is given in bytes. Note that the I/O can only be accesses on 4-byte boundaries and on word size accesses.

## E.1 General purpose I/O



**Register E.1:** PORT A INPUT REGISTER PIN (0x00)

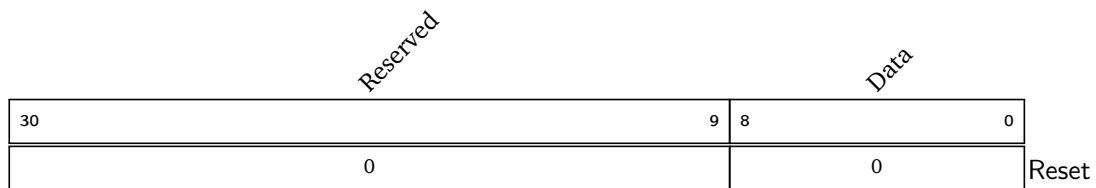
**Note:** This I/O register can only be read.



**Register E.2:** PORT A OUTPUT REGISTER POUT (0x04)

**Write** The data is written to the output pins.  
**Read** The last entered data is read back.

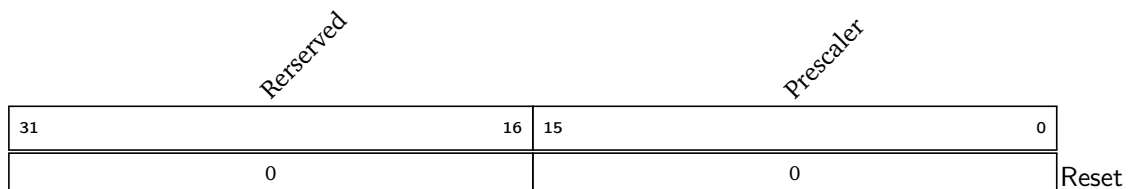
## E.2 USART



**Register E.3:** USART DATA REGISTER USART\_DATA (0x20)

**Write** The data is written to an internal buffer and transmitted.  
**Read** The last received data is read.

Size depends on the Size field in the USART Control Register.



**Register E.4:** USART BAUD RATE REGISTER USART\_BAUD (0x24)

$$\text{Baud rate} = \frac{f_{\text{system}}}{\text{prescaler} + 1}$$

Reserved								TCIE		RCIE		Parity		Size		Reserved		SP							
31								8		7		6		5		4		3		2		1		0	
0										1		1		0		0		0		0		0		Reset	

Reset

**Register E.5:** USART CONTROL REGISTER USART\_CTRL (0x28)

- TCIE** Transmit character interrupt enable.  
**RCIE** Receive character interrupt enable.  
**Parity** 00: none, 10: even, 11: odd.  
**Size** 00: 8 bits, 10: 9 bits, 11: 7 bits, excluding the parity.  
**SP** 0: one stop bit, 1: two stop bits.

Reserved					TC	PE	RC	RF	FE
31				5	4	3	2	1	0
0					0	0	0	0	0

Reset

**Register E.6:** USART STATUS REGISTER USART\_STAT (0x2c)

- TC** Transmit completed. Set directly to 1 when a character was transmitted. Automatically cleared when writing new character to the data register or when writing 0 in the TC bit in USART\_STAT.
- PE** Parity error. Set to 1 if parity is enabled and there is a parity error while receiving. Automatically cleared when data register is read or when writing 0 in the PE bit in USART\_STAT.
- RC** Receive completed. Set to 1 when a character was received. Automatically cleared when data register is read or when writing 0 in the RC bit in USART\_STAT.
- RF** Receive failed. Set to 1 when failed receiving (invalid start bit). Automatically cleared when data register is read or when writing 0 in the RF bit in USART\_STAT.
- FE** Frame error. Set to 1 when a low is detected at the position of the (first) stop bit. Automatically cleared when data register is read or writing a 0 in the FE bit in USART\_STAT.

### E.3 TIMER1

Reserved					TIE	Reserved	EN	
31				5	4	3	1	0
0					0	000	0	Reset

**Register E.7:** TIMER1 CONTROL REGISTER TIMER1\_CTRL (0x80)

**EN** Enable the timer  
**TIE** Timer compare match interrupt enable

Reserved					TCI	Reserved		
31				5	4	3	0	
0					0	0000		Reset

**Register E.8:** TIMER1 STATUS REGISTER TIMER1\_STAT (0x84)

**TCI** Timer compare match interrupt. Set to 1 on compare match between the timer Count register and the Compare Match register. Must be cleared by software by writing a 0.

CNTR	
31	0
0	
Reset	

**Register E.9:** TIMER1 COUNT REGISTER TIMER1\_CNTR (0x88)

**CNTR** This register holds the counted clock pulses on the timer. This register may be written by software. Rolls over at maximum every  $2^{32}/f_{clk}$  seconds.

CMPT	
31	0
0	
Reset	

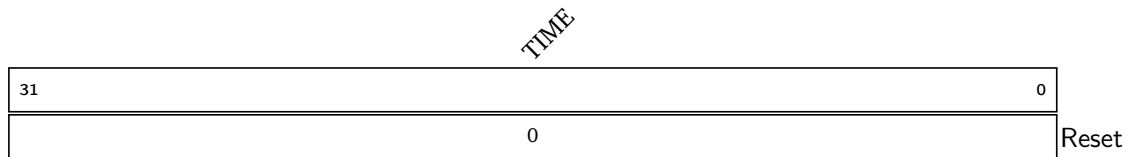
**Register E.10:** TIMER1 COMPARE TIMER REGISTER TIMER1\_CMPT (0x8c)

**CMPT** This register holds the value at which the counter register is compared. On CNTR compares to greater than or equal to

CMPT, the counter register will be cleared and the TCI flag will be set (both in the next clock cycle).

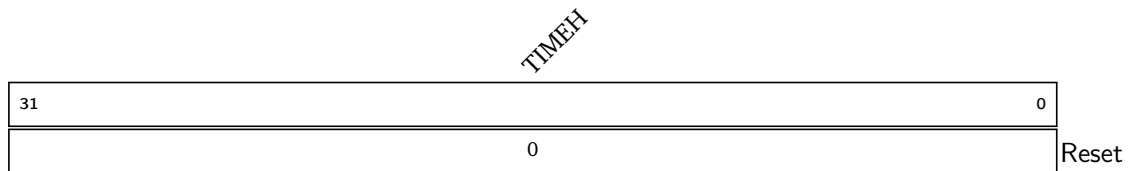
## E.4 TIME

Note: the external timer interrupt has to be enabled by writing a 1 to mie.MTIE.



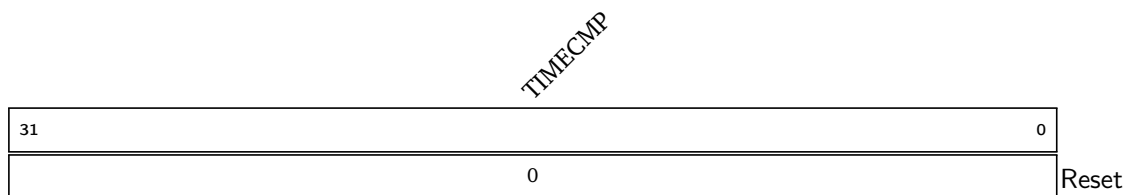
**Register E.11:** TIME EXTERNAL TIMER REGISTER TIME (0xf0)

This register holds the low 32 bits of the external timer. Currently read-only.



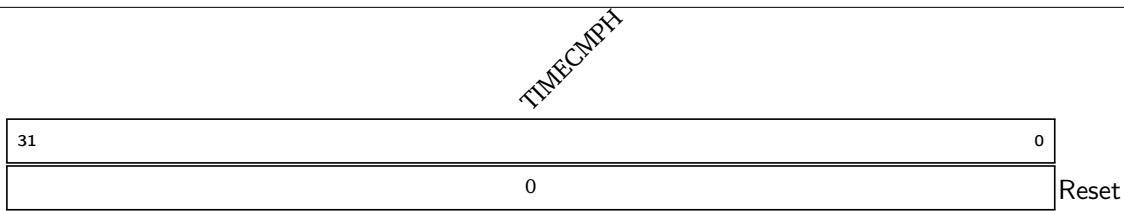
**Register E.12:** TIMEH EXTERNAL TIMER REGISTER TIME (0xf4)

This register holds the upper 32 bits of the external timer. Currently read-only.



**Register E.13:** TIMECMP EXTERNAL TIMER COMPARE REGISTER TIMECMP (0xf8)

This register holds the low 32 bits of the external timer compare register.



**Register E.14:** TIMECMPH EXTERNAL TIMER COMPARE REGISTER TIMECMP (*0xfc*)

This register holds the upper 32 bits of the external timer compare register.