A RISC-V Microcontroller in VHDL

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https://github.com/jesseopdenbrouw/riscv-rv32

For design `riscv-pipe3-csr-md-lic`

Abstract

The RISC-V Instruction Set Architecture (ISA) is an open source instruction set for a processor. This means that anybody can create a processor that uses this instruction set. There are already processors available such as E2-core from SiFive. More freeware cores are available on several platforms (e.g. on GitHub). This documents describes a basic 32-bit RISC-V processor in VHDL. The processor can execute the RV32IM unprivileged instruction set, and most of the instructions from the privileged instruction set. The processor incorporates a ROM, RAM, some simple I/O, a CSR and LIC (local interrupt controller). It is targeted for implementation on an FPGA. It is tested on an Intel Cyclone V with a DE0-CV development board from Terasic with the use of Quartus Prime Lite 21.1 and QuestaSim Intel Starter Edition 2021.2. The GNU C-compiler for RISC-V is used for software development. Many C programs were successfully tested using the GNU C compiler. C++ is supported but most standard concepts create a binary that is too big to fit in the ROM.

This processor is not intended as a replacement for commercial available processors. It is intended as a study object for Computer Science students.

The processor has a three-stage pipeline and executes each instruction in three clock cycles, but the next instructions are fetched and decoded while the current instruction is executed. Jump/branches taken require three clock cycles. ROM, RAM and I/O reads need two clock cycles. This processor also has a basic Control and Status Registers (CSR) set, suitable to handle traps, and a hardware integer multiplier/divider. This version incorporates a bootloader.

This is work in progress. Things will certainly change in the future.

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Contents

1 Introduction

This document describes the buildup of a simple, one core, RISC-V processor, completely written in VHDL. The core contains one HART (Hardware Thread). The processor is able to run a compiled C-program. C++ is supported but some concepts (`cout` with `iostream`, STL) create binaries that is too big to fit in the ROM. The processor can handle the RV32IM Base Integer Instruction Set as set forward in "The RISC-V Instruction Set Manual Volume I: Unprivileged ISA". The processor can handle traps (interrupts/exceptions). The aim is to synthesize for a clock frequency of 80 MHz. The processor utilizes ROM, RAM and some simple I/O (including MTIME and MTIMECMP) effectively making it a microcontroller.

The processor requires three clock cycles to complete an instruction, but the next instructions are fetched and decoded while the current instruction is executed. Jumps, calls and branches taken require three clock cycles because an new instruction has to be fetched. Also, two clock cycles are needed when reading ROM (data), RAM and I/O. ROM and RAM are implemented using onboard RAM block (which are buffered with an output register). The I/O output has a buffer register to speed up the processor. The processor has a basic Control and Status Registers set, offering [M]CYCLE and [M]CYCLEH (completed clock cycles), MTIME and MTIMEH (time since last reset, in microseconds, shadowed from memory mapped registers), [M]INSTRET and [M]INSTRETH (number of retired instructions), and a basic set of CSRs to handle traps. A hardware multiplication requires three clock cycles to complete. A hardware division requires 32+2 or 16+2 clock cycles to complete, depending on the settings. CSR operations require one clock cycle.

The processor executes at top 1 CPI (clocks per instruction) with a sequential flow of instructions. A preliminary test with CoreMark showed a CPI of 1.52.

2 The processor

The RISC-V processors consist of one *core* and some building blocks:

The core:

- The registers contain intermediate data for calculations. The registers may be placed in onboard RAM of ALM flip-flops.
- The ALU is responsible for almost all computations in the processor.
- The PC is used to point to the currently fetched instruction (not the instruction that is currently being executed).
- The Instruction Decoder decodes the fetched instruction and provides control signals to other building blocks.
- The multiply/divide unit calculates integer multiplications, divisions and remainder.

- The control unit regulates the data flow and control flow in the core.

The remaining building blocks:

- The ROM contains the program instructions and constant data. When the bootloader is implemented, the ROM may be written.
- The bootloader ROM contains the program instructions and constant (read-only) data. The boorloader ROM may be excluded from the design
- The RAM contains read-write data (mutable data).
- The I/O is an interface with the outside world.
- The Address Decoder and Data Router is an interface between the memory (ROM, BOOT, RAM, I/O) and the ALU and registers.
- The instruction router routes instructions from the ROM and the boot ROM (if enabled).
- The Control and Status Registers contains a basic set of register.
- The Local Interrupt Controller determines which trap is to be served.

A block diagram of the core is shown in Figure 1.

2.1 Registers

The register file consists of thirty-two 32-bit registers denoted by `x0` to `x31`. Internally, the registers use Big Endian format. Register `x0` (alias `zero`) is hardwired to all zeros. Writing this register has no effect. Reading this register returns all zero bits. Normally, the `x`-names are not used but may be handy when simulating the designs. Table 1 shows the names of the registers as they should be used.

A register can be written to, and two register can be selected for data and/or base address.

The register can optionally be put in onboard RAM blocks. This saves a lot of ALM flip-flops but possibly lowers the system frequency.

2.2 ALU

The Arithmetic and Logic Unit (ALU) handles all computations on data. It can add, subtract, do logic operations such as AND, OR en XOR, can shift data left or right, and sign extend byte and half word data. Some operations require two registers, some only use one register. Some instructions use one register and immediate data. Furthermore the ALU is also used to determine if a conditional branch should be taken. Note that the RISC-V programmer's model does not incorporate status flags as some other architectures do. This requires some extra instructions when adding or subtracting double word (64-bit) data. This is handled by the C compiler. The ALU is also used to compute the return address from unconditional function calls (JAL and JALR instructions). The data is in

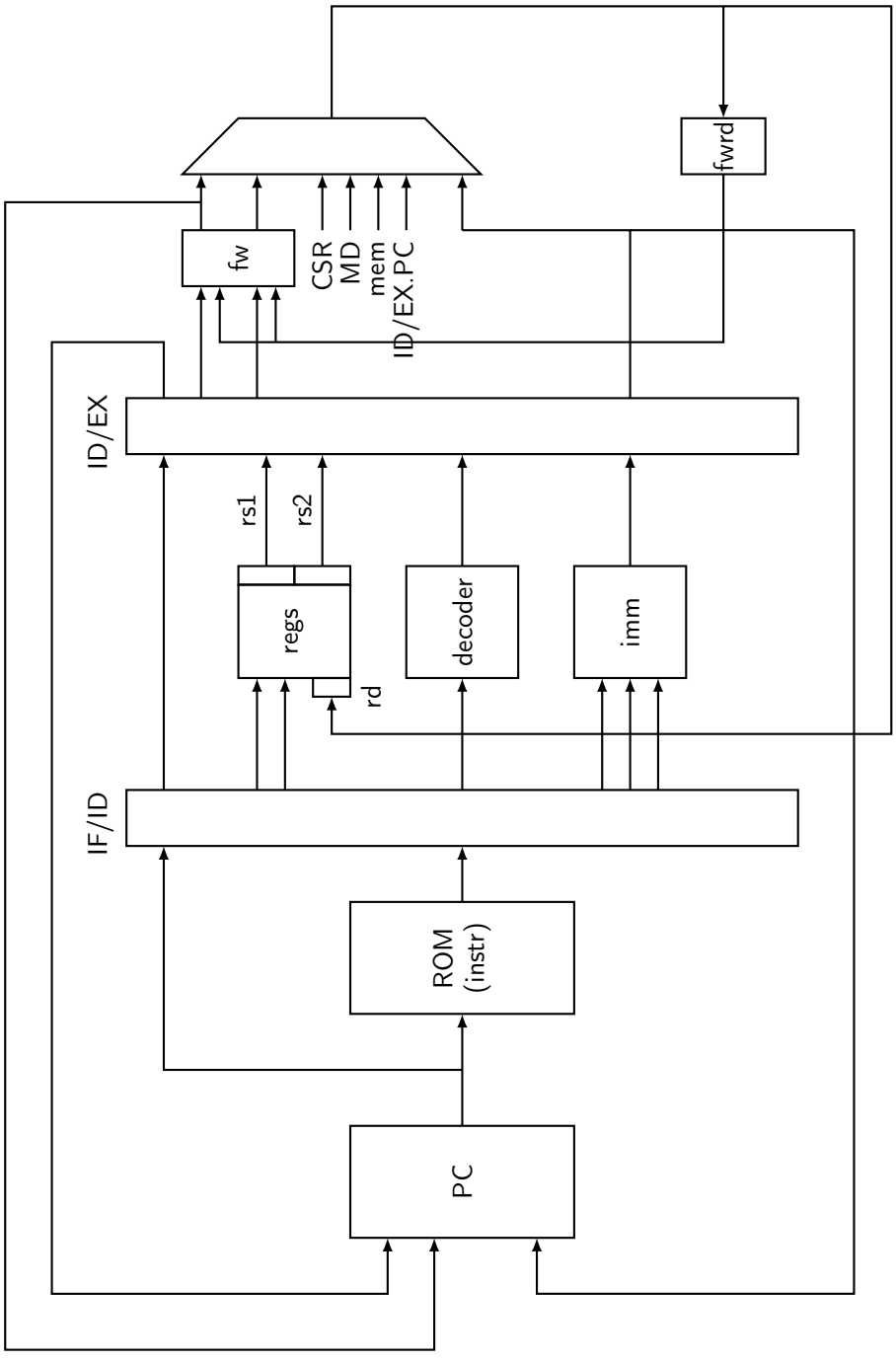


Figure 1: *Overview of the RISC-V core. Not all connections are shown.*

Table 1: *RISC-V registers and their purpose.*

Register	Name	Purpose	Saver
x0	zero	Hard-wired zero	—
x1	ra	Return address	Caller
x2	sp	Stack pointer	Callee
x3	gp	Global pointer	—
x4	tp	Thread pointer	—
x5	t0	Temporary/alternate link register	Caller
x6–x7	t1–t2	Temporaries	Caller
x8	s0/fp	Saved register/frame pointer	Callee
x9	s1	Saved register	Callee
x10–x11	a0–a1	Function arguments/return values	Caller
x12–x17	a2–a7	Function arguments	Caller
x18–x27	s2–s11	Saved registers	Callee
x28–x31	t3–t6	Temporaries	Caller

Big Endian format. The ALU is the only building block that can write registers. The ALU does not compute multiplications and divisions, but merely passes on data from the MD unit.

Note that the computation of jump target addresses is handled by the Program Counter (PC) hardware.

2.3 PC

The Program Counter contains the address of the currently fetched instruction. The address is always on a 4-byte boundary although function calls and conditional jump (JAL, JALR en Bxx instructions) can be on non 4-byte boundaries (the C compiler will always create 4-bytes boundaries). The PC (or rather the VHDL description of the PC) handles the address calculations of jumps and branches taken.

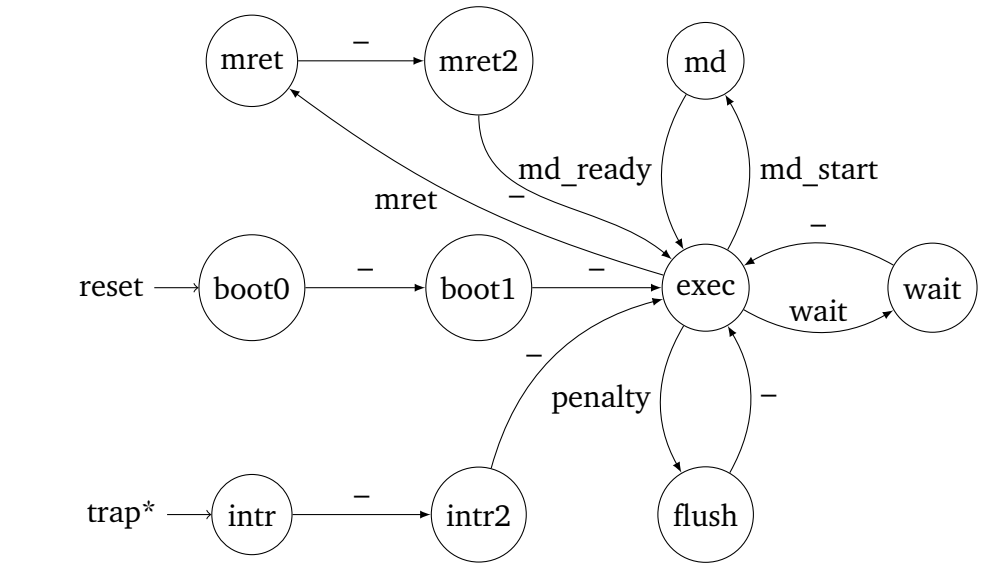
2.4 Instruction Decoder

The instruction decoder decodes the instruction supplied by the ROM as pointed by the PC. An instruction is 4 bytes wide and in Little Endian order. The instruction decoder provides all control signals for the ALU, RAM, ROM, I/O, the PC, the Address Decoder, the CSR, the register file and the MD unit. Some signals are directly wired to the ROM, RAM and I/O.

2.5 Control Unit

The processor uses a ten-state FSM, see figure 2. The PC points to +8 of the currently executing instruction, in a sequential instruction stream. If a jump or branch taken occurs, the FSM inserts a penalty because the PC has to be loaded with the correct value and a new instruction must be fetched (Figure 3). Reading RAM, ROM and I/O requires an

extra state (Figure 4). When a multiply, divide or remainder instruction is encountered, the FSM enters the `md` state and waits for the md-unit to complete (32+2 or 16+2 clock cycles). Note that penalty, wait and md_start cannot occur at the same time.



* trap initiated by hardware or software.

Figure 2: *FSM of the instruction flow of the processor.*

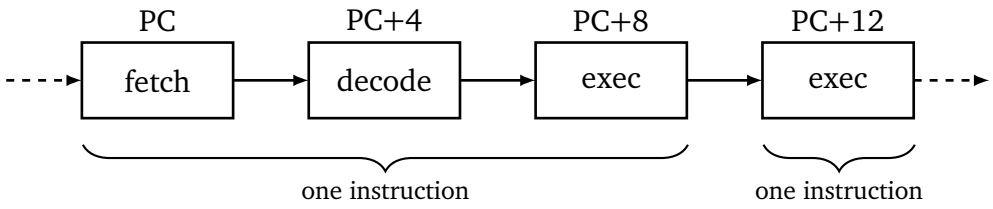


Figure 3: *State sequence for start up/penalty with instruction execution (no wait state).*

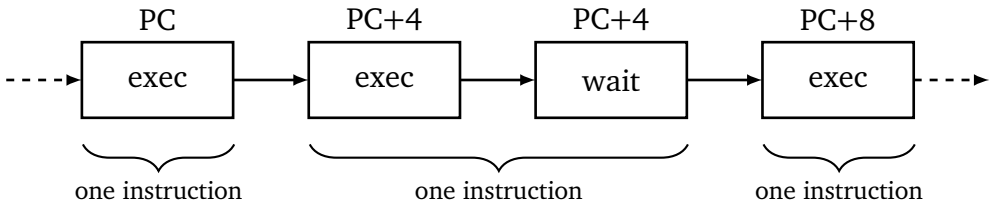


Figure 4: *State sequence for instruction execution (wait state).*

2.5.1 Trap handling

When an interrupt occurs, the FSM enters the `intr` state for fetching the trap vector. An interrupt can occur any time and is called asynchronous. When an interrupt occurs, the current instruction is discarded and must be restarted after return. After fetching the trap handler, new instructions are fetched and the instruction pipeline is flushed.

Exceptions are synchronous to the executing of instructions. When a exceptions occurs, the current instruction is discarded and must be restarted after return. Exceptions to this are the ECALL and EBREAK instructions. These instructions do cause a trap, but are not restarted, so the next instruction is fetched after return. This is handled by the CSR hardware, no software intervention is needed.

When a trap request is asserted, the trap vector is loaded in the next clock cycle. Then, in the second clock cycle, the instruction is fetched and in the third clock cycle the instruction is decoded and in the fourth cycle the instruction is executed. On return from a trap handler, the original contents of the PC is fetched from the CSR and then instructions are fetched. A return flushes the pipeline.

2.6 Address Decoder and Data Router

The Address Decoder and Data Router routes reads and writes to the ROM, bootloader ROM (only reads), RAM and the I/O. The processor uses a 32-bit linear address space for ROM, RAM and I/O. In the default setting, ROM starts at address 0x00000000 and the length is 64 kB. The bootloader ROM starts at address 0x10000000 and the length is 4 kB. Unused ROM addresses return 0x0000000. The RAM starts at address 0x20000000 and length is 32 kB. The I/O starts at address 0xF0000000 and the length is 16 kB by default.

When data is read, the data is collected from the accessed memory and put on an internal bus to the ALU. The ALU can perform sign extension (byte and half word accesses) if needed. Please note that reading data from the RAM, (bootloader) ROM and I/O requires two clock cycles.

Note that instructions can only be fetched from ROM and boot ROM.

2.7 Instruction Router

The Instruction Router routes instructions from the ROM and the boot ROM. If the boot ROM is disabled, the synthesizer will remove this block.

2.8 Control and Status registers

The RISC-V specification describes a set of 4096 control and status register in a separate address space. CSR operations require one clock cycle. Basic event counters are implemented:

- `cycle` and `cycleh` – these 32-bit registers form a 64-bit value that contains the counted clock cycles since the last reset.
- `time` and `timeh` – these registers shadow the contents of the `MTIME` and `MTIMEH` registers from the I/O.
- `instret` and `instreth` – these 32-bit registers form a 64-bit value that contains the counted retired instructions since the last reset.

Note that these registers are read-only. Writes are ignored.

Generic registers:

- `mvendorid` – this register is hardwired to all zero bits.
- `marchid` – this register is hardwired to all zero bits.
- `mimpid` – this register is hardwired to all zero bits.
- `mhartid` – this register is hardwired to all zero bits.
- `mconfigptr` – this register is hardwired to all zero bits.
- `misa` – hardwired to value 0x40001100, indicating 32-bit processing, RV32I base ISA and Integer Multiply/Divide extension.

For trap handling, the following registers are implemented:

- `mstatus` – the only implemented bits are `MIE`, `MPIE` and `MPP`, all other bits are hardwired zero.
- `mie` – for the lower 16 bits, only `MTIE` is implemented, all other bits are hardwired zero.
- `mtvec` – contains the trap handler (vector) address, can be used in direct and vectored mode.
- `mstatush` – this register is hardwired to all zero bits.
- `mscratch` – currently not used, but can be used by software trap handlers.
- `mepc` – contains the PC at point of trap of the *currently* executing instruction.
- `mcause` – contains the cause of the trap as set forward in "The RISC-V Instruction Set Manual, Volume II: Privileged Architecture". For local interrupts, additional codes are used.
- `mtval` – contains the address on the address bus when a trap occurs, not always relevant.
- `mip` – contains the pending interrupts. For the lower 16 bits, only `MTIP` is implemented. The upper 16 bits are used for local interrupts. This register is read-only.
- `mconfigptr` – this register is hardwired to all zero bits.
- `mcountinhibit` – this register has bit 2 (`[m]instret`and 0 (`[m]cycle`)implemented.

The `mcounteren` register are not implemented, because U-mode is not implemented. The `menvcfg` and `menvcfgh` are not implemented, because only M-mode is implemented.

The trap handler (vector) address must be loaded by software at boot time. Both direct and vectored mode are supported. In direct mode all traps redirect to a single trap handler that has to handle both interrupts and exceptions. The most significant bit of `mcause` is 1 when a trap occurred from an interrupt. In vectored mode, the addresses

of *interrupt handlers* are loaded from a jump table. Exceptions are redirected to a single handler. Note that the address of the jump table must be on a 4-byte boundary, and bit 0 of the jump table address has to be set to 1 for vectored mode.

Other CSRs are not implemented. Good synthesizers will remove unused CSRs.

2.9 Local Interrupt Control unit

The Local Interrupt Controller is responsible for selecting which trap request must be serviced by the core. Interrupts have higher priority than exceptions. The state of the serviced trap is visible in the CSR.

The LIC can handle 16 local interrupts (numbered 16 to 31) and the Machine mode external timer interrupt (numbered 7). Other standard RISC-V interrupts (numbered 0 to 6 and 8 to 15) are not available. The external timer interrupt has the highest priority, followed (currently) by the SPI1, TIMER2, USART and TIMER1 interrupts.

Exceptions are handled as set forward in Table 3.7 of "The RISC-V Instruction Set Manual, Volume II: Privileged Architecture": instruction access fault, instruction address misaligned, ECALL (M mode only), EBREAK, load/store address misaligned, load/store access fault. Note that ECALL and EBREAK are user instructions and can be interrupted by an interrupt (i.e. when the ECALL or EBREAK instruction is executing).

2.10 Multiply/Divide Unit

The processor is equipped with a hardware integer multiply/divide unit. All multiply/-divide instructions are supported (`MUL`, `MULH`, `MULHSU`, `MULHU`, `DIV`, `DIVU`, `REM`, `REMU`) and the result is fed to the ALU. A multiplication takes three clock cycles (one clock-in, one multiply, one clock-out). For division, two versions are available. By default, the divider needs 18 clocks (one clock-in, 16 divide, one clock-out) for a division using a poor man's radix-4 division unit. As an alternative, a simple radix-2 division unit can be selected taking 34 clock cycles (one clock-in, 32 divide, one clock-out) to do the division. Thus, the radix-4 divider unit is faster, but needs more cells. The radix-2 divider unit is slower, but needs less cells. You have to enable the M-standard support in the compiler. The multiplier uses special DSP units in the Cyclone V. Most regular FPGAs have onboard multipliers. Note that when executing an operation, the pipeline is stalled. Also note that a trap can interrupt the computation, and then the instruction has to be restarted. Selecting the radix-4 division has a minimum impact on the clock speed.

2.11 Stack pointer

The stack pointer is fully implemented although the ISA does not provide pushes and pops. The stack pointer is used to allocate local variables and is updated with each allocation and deallocation. As usual, the stack grows downwards (to lower addresses) on allocations and upwards (to higher addresses) on deallocations. Therefore the stack pointer is set to the highest RAM address + 1 on boot (which is 0x20008000 by default). The ISA postulates that the stack is aligned on 16-byte boundaries for the I standard.

2.12 ROM

The ROM consists of bytes and is only word addressable for instructions. The ROM is byte, half word and word addressable when reading constant data. Half word and word entries are in Litte Endian format. When reading data from the ROM, half word accesses must be on 2-byte boundaries and word accesses must be on 4-byte boundaries. This simplifies the decoding circuitry. The ROM returns undefined data if an access is not aligned. The processor instantiates the ROM in onboard RAM. Rearranging half word and word data accesses in Big Endian format is handled by the ROM decoding unit. Reading ROM (both instructions and data) requires two clock cycles. This is automatically handled by the processor. The pipeline is stalled for one clock cycle when reading from ROM (data).

Note: the Cyclone V has 3,153,920 bits of onboard RAM available. Because of the 32-bit entries a maximum of 2,097,152 (65536 x 32) bits can be instantiated. This is equivalent to 262,144 bytes.

Note: instructions can only be fetched from the ROM and bootloader ROM. Note: when the bootloader is synthesized in the FPGA, the ROM may also be written with 32-bit data on 4-byte boundaries.

2.13 Booloader ROM

The bootloader ROM contains a small program to upload S-record files in the ROM. The bootloader ROM cannot be written by an upload. Besides that, the bootloader contains a simple monitor program. The bootloader ROM is places in onboard immutable RAM blocks. See Section 12. The bootloader may be excluded from synthesis.

2.14 RAM

The RAM consists of bytes and is byte, half word and word addressable. Half word and word entries are in Little Endian format. The RAM itself is made up of word (i.e. 32-bit) entries and is instantiated with onboard RAM blocks. Due to this fact, half word accesses are only permitted on 2-byte boundaries and word accesses are only permitted on 4-byte boundaries. The RAM returns undefined data if an access is not aligned. Writes will not take place if an access is unaligned. This simplifies the decoding circuitry. For the Cyclone V a maximum of 65536 words of RAM can be instantiated. Rearranging half word and word data accesses in Big Endian format is handled by the RAM decoding unit. The RAM cannot be used for program data.

Note: the Cyclone V has 3,153,920 bits of onboard RAM available. Because of the 32-bit entries a maximum of 2,097,152 (65536 x 32) bits can be instantiated. This is equivalent to 262,144 bytes.

Reading the RAM (byte, half word, word) requires two clock cycles because the RAM output is buffered by a register. This is automatically handled by the processor. The pipeline is stalled for one clock cycle.

2.15 I/O

Currently, the I/O consists of one 32-bit data input and one 32-bit data output, a simple UART, a simple timer, a more elaborate timer, an minimal I^2C peripheral, a general purpose SPI peripheral with interrupt, a dedicated SPI peripheral for SD card access and the TIME and TIMEH memory mapped time registers. Note that the I/O can only be accessed as words and the addresses must be on 4-byte boundaries. If not on a 4-byte boundaries or not word size reads/writes, reads return undefined data whereas writes will not write data. A read requires two clock cycles (the pipeline is stalled for one clock cycle), a write requires one clock cycle. Note that not all I/O addresses are used.

The GPIO has separate inputs and output, both 32 bits. This is because some FPGAs/synthesizers don't allow buried tri-state signals, i.e. the tri-state action must be done in the top level entity. Because of that, there is no data direction register. Currently the inputs come from the slide switches and the push buttons. Note that KEY4 a.k.a. FPGA_RESET is connected to the reset of the processor. The outputs are connected to the 10 red leds and to the two least significant 7-segment displays. Also two output pins are connected to facilitate software generated NSS signals.

The UART can transmit and receive data at 7, 8 or 9 bits, no/even/odd parity and 1 or 2 stop bits. Tested speeds are 9600 bps, 115200 bps and 230400 bps. Several status flags are implemented to guide transmission. Note: more identical UARTs will be added. Receive and transmitted character (local) interrupts are provided (one vector). These interrupt requests must be negated by software. The UART does not provide hardware flow control.

TIMER1 has a 32-bit time register and increments on every clock cycle. It does not have a prescaler. It counts up to compare match T register, after which is will be loaded with 0 again. A compare match (local) interrupt is provided (one vector). Whenever the timer count register is greater than or equal to the compare match T register, an interrupt request is asserted. The interrupt request has to be negated by software. A value of 0 in the compare match T register is valid: the counter does not count, but the compare match (local) interrupt is asserted.

TIMER2 has a 16-bit time register and a 16-bit prescaler, and increments on every clock cycle. It counts up to compare match T register, after which is will be loaded with 0 again. Compare match (local) interrupts are provided (one vector). Whenever the timer count register is greater than or equal to the compare match T register, an interrupt request is asserted. The interrupt request has to be negated by software. The timer provides three more compare registers (A, B, C). Whenever the timer count register is greater than or equal to a compare register (A, B, C) the respective interrupt request is asserted. The interrupt requests have to be negated by software. A value of 0 in the compare match T register is valid: the counter does not count, but the compare match T (local) interrupt is asserted and the compare match interrupts (A, B, C) are asserted whenever the respective compare match register is 0. The prescaler is always preloaded: if the timer is off, the shadow prescaler register is directly written, if the timer is running, the preload register is written and the shadow register is updated at the the next CMPT match. The CMPT/A/B/C registers may optionally use a preload register. If preload is

off, the shadow registers are directly written, if preload is on, the preload registers are written and the shadow registers are updated at the next CMPT match.

Preliminary! I2C1 is a minimized I^2C controller peripheral (master-only). It cannot react to clock stretching and lost arbitration, so only modern targets (slaves) can be connected in a one-master-only system. Both Standard mode (Sm) with a transmission speed of up to 100 kbps and Fast mode (Fm) with a transmission speed of 400 kbps are implemented. Before sending the address byte, the send-start bit must be set and a START is send to the target when the address is written to the I2C1 data register. Before sending or receiving the last data byte, the send-stop bit must be set and a STOP is send to the target after the byte is send to the target or received by the controller. When the read-write bit is set to write, the controller may send another byte when the previous byte is send. When the read-write bit is set to read, the controller switches to read mode and will continuously send clock pulses to read data until the send-stop bit is activated (of course in the last byte to receive). After that, the controller may start transmission again. When reading data, the data from the target is always acknowledged. When an address byte is send and no target responds, a STOP is automatically send, unless the disable-stopbit-generation bit is active. In that case, no STOP is send and the controller may issue a repeated-START. The baud rate prescaler must be loaded with the number of system clock cycles of **one-half** bit time minus 1 for Standard mode and **one-third** bit time for Fast mode. Note that the prescaler is part of the control register CTRL and its value must be preserved when setting or clearing other bits.

SPI1 is a full-fledged SPI master. It can transfer 8-bit, 16-bit, 24-bit and 32-bit data in one SPI cycle. It incorporates a programmable prescaler (from /2 to /256 in powers of 2) and all four phases of clock polarity (CPOL) and phase polarity (CPHA), hardware NSS (Slave Select, active low) and programmable Slave Select setup and hold time. It is possible to use a GPIO pin to use software-controlled NSS.

SPI2 is a simple SPI master dedicated for the micro SC card reader. It can transfer 8-bit, 16-bit, 24-bit and 32-bit data in one SPI cycle. It does not have an hardware NSS signal and no interrupt capability. A single I/O pin is needed for NSS.

The I/O incorporates memory mapped TIMEH:TIME and TIMECMPH:TIMECMP registers. Whenever TIMEH:TIME (as viewed as a 64-bit register) is greater than or equal to TIMECMPH:TIMECMP (as viewed as a 64-bit register) an interrupt request is asserted (one vector). The interrupt request is negated if TIMEH:TIME is less than TIMECMPH:TIMECMP. This has to be handled by software.

2.16 Implemented instructions

For the processor, all RV32IM Unprivileged instructions are implemented but the FENCE instruction act as a no-operation (NOP). From the privileged instruction, ECALL and EBREAK are supported and execute an exception. MRET is used to return from an exception or an interrupt. WFI is not implemented and act as a no-operation (NOP).

3 The FPGA

For this project, we use the Cyclone V FPGA from Intel (formerly Altera). See https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/v.html. The used Cyclone V is the 5CEFA4F23C7 which has 18480 ALMs available. It has 3080 kb of onboard RAM bits available which are used for RAM, ROM, (possibly) bootloader ROM and (possibly) the registers. Depending on the program and used resources, the compiled RISC-V processor uses about 3000 ALMs (about 17 %) and 1,343,488 bits of internal memory (43 %). The clock frequency is approximately 80 MHz, which is sufficient for all program examples. Note that the DE0-CV board has a onboard clock generator with a frequency of 50 MHz, so a PLL is needed to get a frequency of 80 MHz. This FPGA is mounted on a Terasic DE0-CV board. The board has 10 switches, 4 push buttons, 1 reset push button, 10 leds, and 6 seven-segment displays. It also has two 2x20-pin headers to connect off-board devices. See http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=921. For downloading the bitstream file, the onboard USB-Blaster is used.

Disabling the bootloader saves one copy of the ROM and the bootloader ROM. Then the used RAM is 786,432 bits (25 %). Disabling registers in RAM saves 2048 bits, but increases the ALM count.

It is possible to add the Quartus' Signal Tap (embedded) Logic Analyzer. Follow the instructions on https://people.ece.cornell.edu/land/courses/ece5760/Quartus/Signal_tap.html. Note that the Signal Tap uses onboard memory.

To find the best compilation result for speed and/or area, we have to tweak the compiler setting for the synthesizer and the fitter. Best is to do a design space exploration, and randomize the seed. Tweaking the seed may show a difference of 5 MHz on the clock speed.

Table 2 gives some estimates on the design. In all cases, the seed is set to 1 and the optimization is set to balanced. The total amount of ALMs is 18480. The total amount of RAM bits is 3153920.

Table 2: *FPGA resource utilization.*

	no boot no reg in ram	no boot reg in ram	boot no reg in ram	boot reg in ram
Freq	83.33	80.50	77.31	79.05
ALM	3213	2664	3210	2733
RAM	786,432	788,480	1,343,488	1,345,536

4 Processor hardware

The processor hardware is composed of the following VHDL files:

- `processor_common.vhd` – Common types and constants.

- `processor_common_rom.vhd` – Description of the ROM contents.
- `address_decode.vhd` – The address decoder and data router to the memory
- `core.vhd` – The core contains the PC, the registers, the ALU, the MD unit, the control state machine and the memory interface.
- `instr_router.vhd` – Description of the instruction router.
- `rom.vhd` – Description of the ROM. Will be placed in onboard, initialized RAM blocks.
- `bootloader.vhd` – Description of the bootloader ROM. Will be placed in onboard, initialized RAM blocks.
- `ram.vhd` – Description of the RAM. Will be placed in onboard, uninitialized RAM blocks.
- `io.vhd` – Description of the I/O. It contains a 32-bit input register, a 32-bit output register, an UART, a simple timer and the TIME and TIMECMP memory mapped registers.
- `csr.vhd` – Description of the Control and Status registers.
- `lic.vhd` – Description of the Local Interrupt Controller.
- `riscv.vhd` – Top-level description of the processor. Connects all the building blocks to a viable processor.
- `riscv.sdc` – Constraints file. Sets the target clock frequency.
- `tb_riscv.vhd` – VHDL testbench to simulate the design.
- `tb_riscv.do` – QuestaSim/Modelsim command script.

In the file `processor_common.vhd`, a number of constant parameters are available:

- `SYSTEM_FREQUENCY` – Set to 50 MHz. Change this if you use a PLL with a different frequency.
- `CLOCK_FREQUENCY` – Set to 1 MHz. Used to calibrate the internal clock. The compiler assumes 1 MHz and some library functions depend on it.
- `NUMBER_OF_REGISTERS` – Set to 32 for I standard. Set to 16 for E standard.
- `HAVE_MULDIV` – Set to TRUE, the MD unit is included. Set to FALSE to exclude MD unit. If set to false, you must not specify the hardware multiply/divide options while compiling software, i.e. multiply and division occur in software.
- `FAST_DIVIDE` – Set to TRUE to use the radix-4 divider. Set to FALSE to use the radix-2 divider.
- `VECTORED_MTVEC` – Set to TRUE to provide vectored interrupts. You still have to set bit 0 to 1 in `mtvec` CSR. You can still use direct mode. Set to FALSE to only use direct interrupts.

- `MSTATUS_MIE_DISABLES_INTERRUPTS` – Set to TRUE to only disable interrupts when `mstatus.MIE` is 0. Set to FALSE to disable all traps (so including exceptions and when `mstatus.MIE` is 0).
- `HAVE_BOOTLOADER_ROM` – Set to TRUE to provide the bootloader ROM. The PC is set to the start of the bootloader. Set to FALSE to disable the bootloader ROM. The PC is set to the start of the ROM. Disabling the bootloader reduces the RAM block count considerably.
- `HAVE_REGISTERS_IN_RAM` – Set to TRUE to place the registers in onboard RAM blocks. This lowers the ALM count drastically, but may have an impact on the system frequency. Set to FALSE to place the registers in ALM flipflops.

4.1 Pin assignments

The pin assignments for the DE0-CV board are as follows (Table 3). Note that not all signals are assigned to a pin, in which case the fitter will assign a suitable pin.

Table 3: *Pin assignments for the DE0-CV board.*

Signal	Pin Name	Board name, comments
clk	M9	System clock
areset	P22	FPGA_RESET, active low reset
uart1rxd	N19	GPIO_0_D15, UART1 receive
uart1txd	P19	GPIO_0_D17, UART1 transmit
pina[31]	—	Fitter assigned
pina[30]	—	Fitter assigned
pina[29]	—	Fitter assigned
pina[28]	—	Fitter assigned
pina[27]	—	Fitter assigned
pina[26]	—	Fitter assigned
pina[25]	—	Fitter assigned
pina[24]	—	Fitter assigned
pina[23]	—	Fitter assigned
pina[22]	—	Fitter assigned
pina[21]	—	Fitter assigned
pina[20]	—	Fitter assigned
pina[19]	—	Fitter assigned
pina[18]	—	Fitter assigned
pina[17]	—	Fitter assigned
pina[16]	—	Fitter assigned
pina[15]	M6	KEY3
pina[14]	M7	KEY2
pina[13]	W9	KEY1
pina[12]	U7	KEY0

Continued on next page

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Signal	Pin Name	Board name, comments
pina[11]	—	Fitter assigned
pina[10]	—	Fitter assigned
pina[9]	AB12	SW9
pina[8]	AB13	SW8
pina[7]	AA13	SW7
pina[6]	AA14	SW6
pina[5]	AB15	SW5
pina[4]	AA15	SW4
pina[3]	T12	SW3
pina[2]	T13	SW2
pina[1]	V13	SW1
pina[0]	U13	SW0
pouta[31]	—	Fitter assigned
pouta[30]	U22	HEX16
pouta[29]	AA17	HEX15
pouta[28]	AB18	HEX14
pouta[27]	AA18	HEX13
pouta[26]	AA19	HEX12
pouta[25]	AB20	HEX11
pouta[24]	AA29	HEX10
pouta[23]	—	Fitter assigned
pouta[22]	AA22	HEX06
pouta[21]	Y21	HEX05
pouta[20]	Y22	HEX04
pouta[19]	W21	HEX03
pouta[18]	W22	HEX02
pouta[17]	V21	HEX01
pouta[16]	U21	HEX00
pouta[15]	T17	GPIO_0_D34, software NSS
pouta[14]	C11	SDDAT3, SPI2 software NSS
pouta[13]	—	Fitter assigned
pouta[12]	—	Fitter assigned
pouta[11]	—	Fitter assigned
pouta[10]	—	Fitter assigned
pouta[9]	L1	LEDR9
pouta[8]	L2	LEDR8
pouta[7]	U1	LEDR7
pouta[6]	U2	LEDR6
pouta[5]	N1	LEDR5
pouta[4]	N2	LEDR4
pouta[3]	Y3	LEDR3
pouta[2]	W2	LEDR2

Continued on next page

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Signal	Pin Name	Board name, comments
pouta[1]	AA1	LEDR1
pouta[0]	AA2	LEDR0
timer2oct	N21	GPIO_0_D10, output compare T
timer2oca	R21	GPIO_0_D12, output compare/PWM A
timer2ocb	N20	GPIO_0_D14, output compare/PWM B
timer2occ	M22	GPIO_0_D16, output compare/PWM C
spi1sck	K19	GPIO_0_D26, SPI1 clock
spi1mosi	R16	GPIO_0_D28, SPI1 MOSI
spi1miso	R16	GPIO_0_D30, SPI1 MISO
spi1nss	T19	GPIO_0_D32, SPI1 hardware NSS
spi2sck	H11	SDCLOCK, SPI2 clock
spi2mosi	B11	SDCMD, SPI2 MOSI
spi2miso	K9	SDDAT0, SPI2 MISO
i2c1scl	T18	GPIO_0_D33, I2C1 SCL
i2c1sda	T15	GPIO_0_D35, I2C1 SDA

4.2 Simulation

The designs can be simulated fully, using QuestaSim Intel Starter or ModelSim Intel Starter. You need a (free) license for QuestaSim. During simulation, all essential signals can be viewed, as is the RAM. The RAM is viewed as 32-bit entries, so we need to do some manual calculations to correctly find byte, half word and word accesses. Simulation can be started from Quartus. Please note that the bootloader must be disabled for normal program start up.

5 Cloning the RISC-V project

Now we have to clone the RISC-V project. It incorporates the full Quartus Prime Lite project with the processor written in VHDL. It also incorporates some simple C program examples and a taylor-made program to convert a RISC-V executable to a VHDL table suitable for the ROM. Create a working directory (and change to that directory) and issue the command:

```
1 git clone https:/github.com/jesseopdenbrouw/riscv-minimal
```

In the created directory, you will see the following directories:

`sw` – Sample software programs, linker script, library and startup files
`docs` – Documentation
`rtl` – the VHDL description(s)

Change directory to `sw`. Make sure the RISC-V C compiler is available (see Section 6) and is in your path environment variable. Now enter the command `make`. It will compile all

programs and the support programs `srec2vhdl` and `upload`. To clean up the programs, issue the command `make clean`.

If you want, you can compile the processor with the standard program incorporated, which is by default, flashing onboard leds and writing the current time since last reset via UART1 at 115200 bps. Start your Quartus Prime Lite software and open the project in the `rtl` directory. Now start a build by clicking on the play-symbol. It should compile a standard setting (this takes a long time). When finished, you can download the FPGA contents to the DE0-CV board.

To test one of the programs, change directory to one of the directories in `sw` and copy the file with `.vhd` extension to the directory containing the VHDL description under the name `processor_common_rom.vhd`. Now start Quartus and start the compilation. After a successful compilation, you can program the Cyclone V on a DE0-CV board.

The design is targeted for a clock speed of 80 MHz. Depending on how "good" the device is fabricated, higher clock speeds may be obtained. With one device, we could speed up the clock to 152 MHz.

Compilation of the hardware design is independent of the size of the software program. Several design goals may be selected, such as highest clock speed, minimum power or minimum area. Depending on the compilation settings, compilation time may decrease or increase.

6 Setting up the GNU C compiler for *this* RISC-V

The processor can run C and C++ programs that are compiled using the GNU C/C++ compiler for RISC-V. Besides that, a separate linker script and startup file are needed to setup the compiled code. It is possible to set up the C library for multiple RISC-V architecture versions and select a version during compilation. Building the C/C++ compiler (from Linux) is straightforward:

1. You need a current GNU C/C++ compiler installed or your Linux box. You also need all essential building tools:

```
apt install autoconf automake autotools-dev curl python3 libmpc-dev libmpfr-dev libgmp-dev gawk build-essential bison flex texinfo gperf libtool patchutils bc zlib1g-dev libexpat-dev
```

2. You need the texinfo package. On Ubuntu et al. issue

```
apt install texinfo
```

3. In your home directory, enter the command

```
git clone --recursive https://github.com/riscv/riscv-gnu-toolchain
```

4. Wait for the cloning to end (takes a long time, about 30 minutes on a Zbook G5 2020 with a 10 MB/s internet connection)
5. Change to the directory with

```
cd riscv-gnu-toolchain
```

6. Make the `build` directory with:

```
mkdir build; cd build
```

7. Check the current configuration with

```
../configure --help | grep abi
```

   It should say:

```
--with-abi=lp64d    Sets the base RISC-V ABI, defaults to lp64d
```

   The toolchain is currently configured for 64-bit RISC-V. That is not what we want.

8. Enter:

```
../configure --prefix=/opt/riscv32 --with-arch=rv32im --with-abi=ilp32 --with-multilib-generator="rv32i-ilp32--;rv32e-ilp32e--"
```

   This will set the default architecture to RV32IM, with options for RV32I and RV32E (reduced registers, without hardware integer multiply/divide), and the ABI to ilp32 and ilp32e (reduced registers). This means that integers, long integers and pointers use 32-bit entities. The destination directory is `/opt/riscv32`.

9. Now enter the `make` command: `sudo make`
   Here `make` has to run with supervisor privilege, because the toolchain is put in `/opt/riscv32`. This takes a long time (about 45 minutes on a Zbook G5). At some points the compilation seems to hang, but it is just compiling complicated C-files. By the way, you will see a lot of warnings.
10. Now that the toolchain is setup, we have to put the path into the `$PATH` environment variable so enter

```
export PATH=/opt/riscv32/bin:$PATH
```

11. Check if the compiler is available:

```
riscv32-unknown-elf-gcc -v
```

    It should say something like:

```
Using built-in specs.
COLLECT_GCC=riscv32-unknown-elf-gcc
COLLECT_LTO_WRAPPER=/opt/riscv32/libexec/gcc/riscv32-unknown-elf/12.1.0/lto-wrapper
```

```
Target: riscv32-unknown-elf
Configured with: /home/jesse/riscv-gnu-toolchain/build/../gcc/configure --target=riscv32-unknown-elf --prefix=/opt/riscv32 --disable-shared --disable-threads --enable-languages=c,c++ --with-pkgversion=g1ea978e3066 --with-system-zlib --enable-tls --with-newlib --with-sysroot=/opt/riscv32/riscv32-unknown-elf --with-native-system-header-dir=/include --disable-libmudflap --disable-libssp --disable-libquadmath --disable-libgomp --disable-nls --disable-tm-clone-registry --src=/home/jesse/riscv-gnu-toolchain/gcc --enable-multilib --with-multilib-generator='rv32i-ilp32--;rv32e-ilp32e--' --with-abi=ilp32 --with-arch=rv32im --with-tune=rocket --with-isa-spec=2.2 'CFLAGS_FOR_TARGET=-Os   -mcmodel=medlow' 'CXXFLAGS_FOR_TARGET=-Os   -mcmodel=medlow'
Thread model: single
Supported LTO compression algorithms: zlib
gcc version 12.1.0 (g1ea978e3066)
```

6.1 Register subset

It is possible to compile the toolchain to only use register `x0` to `x15`. This is called the RISC-V E extension. As a positive side effect, the register file can be cut down from 32 registers to 16 registers, saving 512 memory element. This will lower the ALM (cell) count and possible speed up the device. A negative side effect is that the pressure on register allocation is higher, possibly increasing instruction count when saving registers on the stack.

Using the above recipe, the toolchain is set up for both RV32I and RV32E (without hardware integer multiply/divide). You need the specify the architecture and ABI during compile time of the RISC-V programs.

Now compile a C program with:

```
riscv32-unknown-elf-gcc -O2 -g -o flash flash.c -Wall -T ../ldfiles/riscv.ld -march=rv32e -mabi=ilp32e -nostartfiles --specs=nano.specs ../crt/startup.c
```

Make sure to use `-march=rv32e` and `-mabi=ilp32e`.

7 Compiling a C program by hand

We tested a large amount of programs with and without trap handling. We tested all I/O. We did test the use of the C library (`malloc` et al, floats and double calculation, some trigonometry functions from the mathematical library), but more tests are needed.

Compiling a program requires the following steps:

- In the program directory `CODE`, create a new directory and change to that directory.
- Create a C program file, we assume `flash.c`.
- Now issue the command:

```
riscv32-unknown-elf-gcc -O2 -g -o flash flash.c -Wall -T ../ldfiles/riscv.ld -march=rv32i -nostartfiles --specs=nano.specs ../crt/startup.c
```

  We supply our own linker file (`-T ../ldfiles/riscv.ld`) and we supply our own startup file (`../crt/startup.c`). Make sure to use `-nostartupfiles` otherwise the default startup file will be linked and errors will report. There a four startup files:

  - `empty.S` – Empty startup file only providing the entry symbol. Can be used with assembler programs. Written in assember.
  - `minmal.S` – Provides the entry symbol, loads the global pointer and stack pointer. Can be used with assembler programs. Written in assembler.
  - `startup.S` – Provides the entry symbol, loads the global pointer and stack pointer and calls `main`. On return of `main`, it waits in an endless loop. Can be used with minimalistic C programs that do not need global variable initialization and BSS. Written in assembler.
  - `startup.c` – Full support for C programs. Can be used with the standard C library and the mathematical library. Written in C and uses a few assembler instructions.

- Next issue the command:

```
riscv32-unknown-elf-objcopy -O srec flash flash.srec
```

  This will create an S-record file in Motorola hex-format.

- Next issue the command:

```
../bin/srec2vhdl -wf flash.srec flash.vhd
```

  This will create a VHDL file with the ROM encoded as 32-bit Little Endian quantities. Note: the taylor-made `srec2vhdl` has to be compiled before. See Section 5.

- If the bootloader is disabled: issue the command:

```
cp flash.vhd ../../HARDWARE/riscv-pipe3-csr-md-lic.bootloader/processor_common_rom.vhd
```

  This will copy the VHDL file to the RISC-V processor ROM file.

- Now start the compilation of the VHDL code in Quartus Prime Lite and program the compiled file. This file has the extension `.sof`. See Figures 5 to 7.

- If the bootloader is enabled: reset the board to start the bootloader. Then start uploading the S-record file with:

```
../bin/upload -v flash.srec
```

This will upload the file `flash.srec` to the board. See also Section 12.

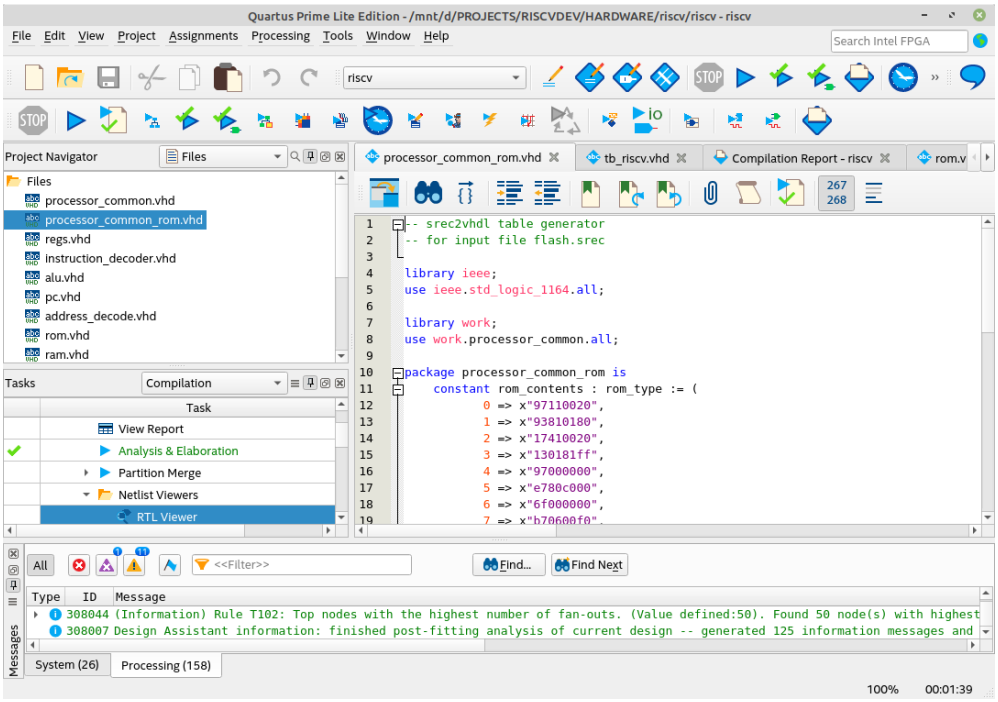


Figure 5: *Image of the Quartus project (1).*

8 Implemented system calls

The `sbrk` system call, used for allocating RAM memory, is implemented. Note that there is a limited amount of RAM. Note that `sbrk` is not called by the user. Use `malloc` et al.

The `gettimeofday` system call is implemented. It returns the seconds and microseconds since the last reset of the processor. You need to call the `gettimeofday` C function for proper handling.

The `times` system call is implemented, but only for non-trap system calls. When using trapped systems calls (using ECALL), `gettimeofday` is used.

The `read` and `write` system calls are implemented but in turn they call the userland functions `__io_getchar` and `__io_putchar` functions to read or write a character. Normal use is for the latter two to transmit or receive via UART1. When implemented, `printf` and `scanf` can be used.

Other system calls return an error because they cannot fulfill the requested operation, such as `open`. Note that some system calls are in fact not implemented and return undetermined behavior.

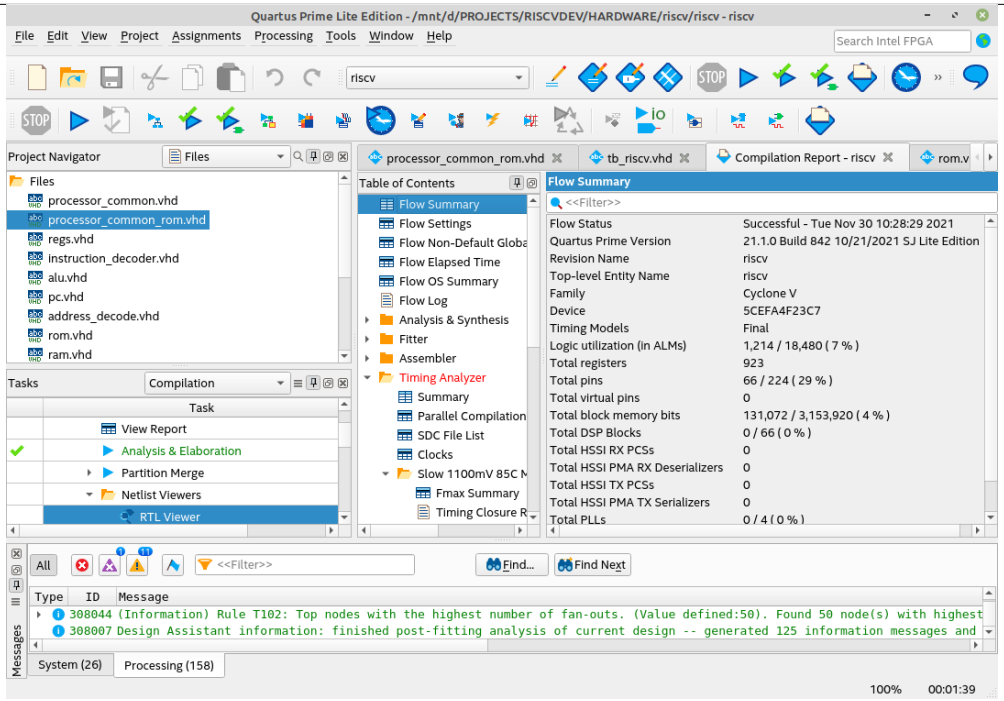


Figure 6: *Image of the Quartus project (2).*

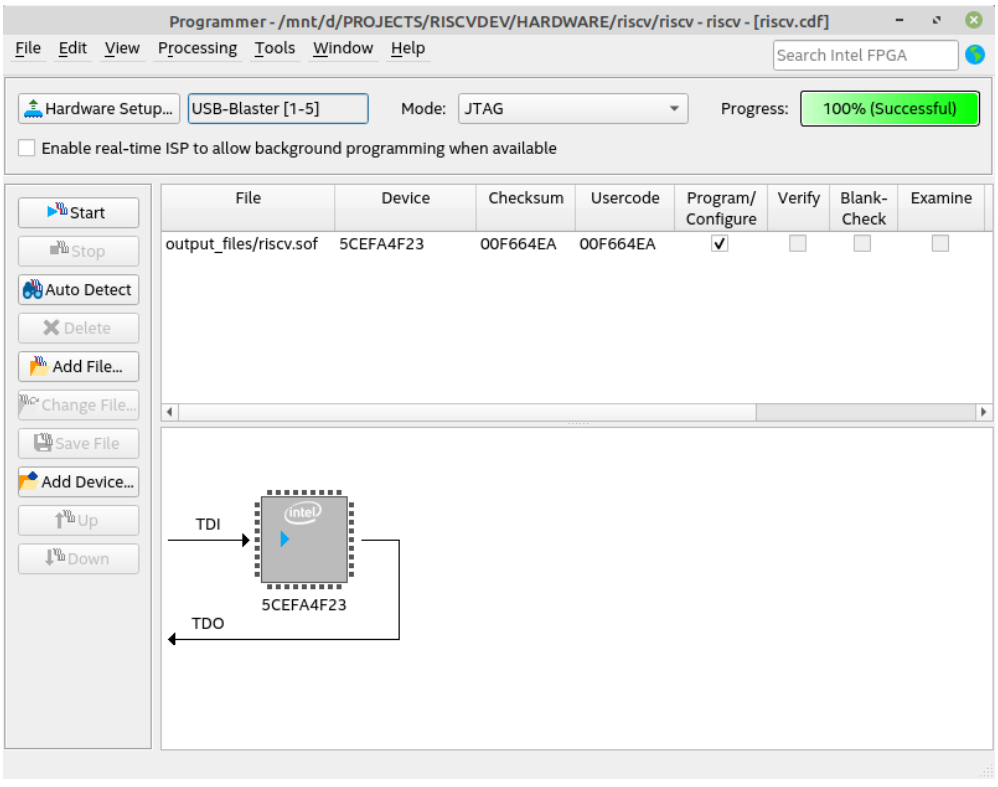


Figure 7: *Image of the programmer.*

Note: when using traps, the system calls are handled by a trap handler (by using ECALL). This is the default behavior of the tool chain. When not using traps, the system calls

are rerouted to functions in a library. You need to set up your software properly, in essence provide functions that override the standard C library functions. See the software examples.

9 Using trap handlers in software

We provide (see software examples `interrupt_direct` and `interrupt_vectored`) a basic implementation of trap handlers. In direct mode, the `universal_handler` handles all traps (interrupts and exceptions). The entry point (the address loaded in the `mtvec` CSR) must be set in the `main` function on a 4-byte boundary, as is enabling traps. In vectored mode, interrupts are redirected to their own handlers via a jump table. The start address of the jump table must be set in the `main` function on a 4-byte boundary AND bit 0 must be set to 1, and traps must be enabled. The first entry of the jump table points the universal handler that only handles exceptions. The external timer has its own handler called `external_timer_handler`. I2C1 has its own handler for transmit and receive complete interrupts, which is only one handler. The handler is called `i2c1_handler`. TIMER1 has its own handler called `timer1_handler`. TIMER2 has its own handler called `timer2_handler`. Note that there is only one handler for all four interrupt requests. SPI1 has it own handler called `spi1_handler`. UART1 has its own handler called `uart1_handler`. This handler is used for both receive and transmit interrupts. Note that negating the interrupt request must be done by software in the respective handlers. The interrupt requests are *not* negated by hardware. Note: the external timer interrupt has to be enabled by writing a 1 to `mie.MTIE`. Both software examples implement all available interrupts: system timer, SPI1, I2C1, TIMER2, UART1 and TIMER1. SPI2 doesn't have interrupts.

10 Software programs

In de `sw` directory, there are a number of software programs available. First, the common files:

- `ldfiles` – contains the linker scripts. There are three scripts:
  - `riscv.ld` – default linker script: ROM = 64 kB, RAM = 32 kB, I/O = 16 kB.
  - `riscv-largerom.ld` – default linker script: ROM = 128 kB, RAM = 32 kB, I/O = 16 kB.
  - `riscv-big.ld` – default linker script: ROM = 128 kB, RAM = 64 kB, I/O = 16 kB.
- `crt` – contains the startup files.
- `bin` – contains the binaries of `srec2vhdl` and `upload`.
- `include` – contains the header files for the design. Use `#include <thuasrv32.h>` in programs.

- `lib` – contains the libraries for the design. Link against`libthuasrv32.a`.

Some examples are to be used in de simulator only, mainly to test functionality on clock cycle accuracy. Some examples work on the DE0-CV board, but without testing traps. Two examples work on the board and use traps.

- `add64` – simple 64-bit addition. For use in the simulator.
- `assembler` – a simple assembler program. For use in the simulator.
- `basel_problem` – a program that calculates the sum of the inverses of the squares of natural numbers, up to 1000. For use in the simulator. Used to test the divider.
- `bootloader` – the bootloader program, placed in the bootloader ROM. It has separate startup and linker files. Uses UART1. Works on the board.
- `clock` – a simple clock using the CSR MTIME and MTIMEH registers to fetch the time since last reset. Uses UART1. Works on the board.
- `double` – some floating point double computations. For simulation.
- `exp` – calculates Euler's number e. For simulation.
- `fatfs` – implementation of FATFS[1], supports read/write, long filename, codepage 437 (US). FAT16, FAT32 supported. exFAT not tested. Works on the board.
- `flash` – flash the DE0-CV board leds, works on the board.
- `float` – some floating point float computations. For simulation.
- `global` – test for globals and local statics with initialization. For simulation
- `hex_display` – program that reads 8 switches from the board and display them as a 2-digit hexadecimal value on the 7-segment display. Works on the board. Note that on the DE0-CV board, the decimal points cannot be used, because they are not connected to FPGA pins.
- `i2c1findslaves` – program that uses the I2C1 peripheral to find slaves on the I^2C bus. Prints out the found slaves addresses on the terminal. Works on the board.
- `i2c1tmp102` – program that uses the I2C1 peripheral to fetch the temperature data of an TMP102 temperature sensor and displays the raw data on the terminal. Works on the board.
- `interrupt_direct` – program to test the interrupt handling using direct mode and prints out the elapsed time. Uses UART1. Works on the board.
- `interrupt_vectored` – program to test the interrupt handling using vectored mode.and prints out the elapsed time. Uses UART1. Works on the board.
- `interval` – program that uses the `clock` C library function to time 5 seconds since last read. Uses UART1. Works on the board.

[1] http://elm-chan.org/fsw/ff/00index_e.html

- `ioadd` – adds the lower 5 switches to the upper 5 switches and displays the result on the leds. Tests addition, shifting and I/O. Works on the board.
- `linked\_list` – example on how to use linked lists. This program soups up all available dynamic RAM but does not penetrate the reserved stack space. Uses UART1. Works on the board.
- `malloc` – example to test `malloc` and friends. Works. Used in simulations.
- `monitor` – simple monitor program. Works on the board. Uses strings, UART1, RAM, ROM, I/O and `sprintf` (and therefore `malloc` et al.).
- `mult` – integer multiplication with the C library. Set to the E extension with no hardware multiply/divide support. For simulations.
- `qsort` – sorts an integer array using the `qsort` C library function. Works in simulation.
- `riemann_left` – calculates the Riemann Left Sum of $\sin^2 x$ from 0 to 2π. For use in the simulator. The result must be π.
- `shift` – shifts. For use in simulations.
- `spi1readeeprom` – using the SPI1 peripheral to read out 16 bytes of the 25AA010A EEPROM slave, one byte at the time, using hardware Slave Select. Uses UART1. Works on the board.
- `spi1softnss` – as `spi1readeeprom`, using software Slave Select.
- `spi1speed` – using the SPI1 peripheral to read out (full speed) 16 bytes of the 25AA010A EEPROM slave, using hardware Slave Select. Uses UART1. Works on the board.
- `spi1writeeeprom` – using the SPI1 peripheral to write and read out (full speed) the 25AA010A EEPROM slave, using software Slave Select. Uses UART1. Works on the board.
- `sprintf` – prints integers, floats/doubles to a string. This is a big binary. For simulations.
- `string` – some string functions. For simulations.
- `testio` – simple program that copies the input (switches) to the output (leds). Works on the board.
- `trig` – some float trigonometry functions for float and double. Prints results to UART1. This is a big binary.
- `upload` – a Linux/PC program to upload an S-record file using the bootloader.
- `uart_test` – simple UART1 program. Works on the board.
- `uart_cpp`– simple C++ UART program. Makes use of a singleton design pattern. Uses a lot of ROM. Works on the board.

- `uart_printf` – simple program that prints an integer, a pointer, a float and a double to the terminal using `printf`, this is a big binary. Works on the board.
- `uart_sprintf` – simple program that prints an integer, a pointer, a float and a double to the terminal, this is a big binary. Works on the board.

Note: we use a lot of the `volatile` keyword to emit the variables to RAM for easy inspection in the simulator. You will see compiler warnings from C library functions.

Note that the floating point programs loads (huge) functions from the C library and possibly creates a binary that is too large to fit in the ROM. In that case, the linker will issue an error and does not build the binary. You have to update the data sizes in the VHDL description and update the linker script with suitable data sizes.

When using floats and doubles in `sprintf/printf`, you need to supply the linker with the `-u _printf_float` option. When using floats and doubles in `sscanf/scanf`, you need to supply the linker with the `-u _scanf_float` option. Also, using `printf` and `scanf` create big binaries.

10.1 srec2vhdl

This is a homebrew utility to convert a Motorola S-record file into a VHDL file suitable for inclusion of the processor. The program is called with:

```
srec2vhdl [-fbwhqv0] [-i <arg>] inputfile [outputfile]
```

`inputfile` is the S-record file, created by the `objdump` program. `outputfile` is the VHDL output file. When omitted, `stdout` is used. There are a number of options:

- `-f` makes a full output that directly can be used. If not used, only the ROM table contents itself is produced.
- `-w` ROM contents is in words (32 bits).
- `-h` ROM contents is in half words (16 bits).
- `-b` ROM contents is in bytes (8 bits).
- `-v` Verbose output.
- `-0` Output unused ROM data as 0 instead of don't care.
- `-q` Quiet output, only error messages are displayed.
- `-i <arg>` indents each line with `<arg>` spaces.

Note: uninitialized ROM contents are emitted as don't care, except when the `-0` option is used. Don't cares are set to 0 by Quartus on default.

11 Address ranges and memory sizes

By default, the ROM starts at address 0x00000000 and and has a size of 64 kB (16 k words). The bootloader ROM starts at address 0x10000000 and has a size of 4 kB (1 k words). The Program Counter starts at address 0x10000000. The RAM starts at address 0x20000000 and has a size of 32 kB (8 k words). The stack pointer is set to one address above the last RAM byte, by default at 0x20008000. The I/O starts at address 0xF0000000 and has a size of 16 kB (4 k words).

The ROM, bootloader ROM, RAM and I/O may be moved to another start location. The Program Counter is started at the correct address. The placement of the ROM is in 256 MB intervals, which are the 4 most significant bits of a 32-bit address. The same holds for the RAM and the I/O. To move the ROM, open file `processor_common.vhd` and go down to the end of the file. There you will see the following lines:

```
1  -- The highest nibble (4 bits) of the ROM, bootloader, RAM and I/O
2  -- This will set the memories at 256 MB intervals
3  constant rom_high_nibble : std_logic_vector(3 downto 0) := x"0";
4  constant bootloader_high_nibble : std_logic_vector(3 downto 0) := x"1";
5  constant ram_high_nibble : std_logic_vector(3 downto 0) := x"2";
6  constant io_high_nibble : std_logic_vector(3 downto 0) := x"F";
```

Change the start locations of the memories by changing the constants. Make sure the memories do not overlap. To change the sizes of the memory, look for the lines as shown below:

```
1  -- The ROM
2  -- NOTE: the ROM is word (32 bits) size.
3  -- NOTE: data is in Little Endian format (as by the toolchain)
4  --       for half word and word entities
5  --       Set rom_size_bits as if it were bytes
6  --       default is 64 kB data
7  constant rom_size_bits : integer := 16;
8  constant rom_size : integer := 2**(rom_size_bits-2);
9  type rom_type is array(0 to rom_size-1) of data_type;
10 -- The contents of the ROM is loaded by processor_common_rom.vhd
11
12 -- The bootloader ROM
13 -- NOTE: the bootloader ROM is word (32 bits) size.
14 -- NOTE: data is in Little Endian format (as by the toolchain)
```

```
    --       for half word and word entities
    --       Set bootloader rom_size_bits as if it were bytes
    --       default is 4 kB data
    constant bootloader_size_bits : integer := 12;
    constant bootloader_size : integer := 2**(↩
       ↪bootloader_size_bits-2);
    type bootloader_type is array(0 to bootloader_size-1) of ↩
       ↪data_type;
    -- The contents of the bootloader ROM is loaded by ↩
       ↪bootloader.vhd

    -- The RAM
    -- NOTE: the RAM is 4x byte (8 bits) size, supporting
    --       32-bit Big Endian storage,
    --       so we have to recode to support Little Endian.
    --       Set ram_size_bits as if it were bytes
    -- Default is 32 kB data
    constant ram_size_bits : integer := 15;
    constant ram_size : integer := 2**(ram_size_bits-2);
    -- The type of the RAM block
    type ram_type is array (0 to ram_size-1) of std_logic_vector↩
       ↪(7 downto 0);

    -- The I/O
    -- NOTE: the I/O is word (32 bits) size, Big Endian
    --       there is no need to recode the data
    --       The I/O can only handle word size access
    --       Set io_size_bits as if it were bytes
    -- Default 256 bytes data
    constant io_size_bits : integer := 8;
    constant io_size : integer := 2**(io_size_bits-2);
    type io_type is array (0 to io_size-1) of data_type;
```

Note that you also have to make changes to the linker script. In the file `riscv.ld`, at the top you will find the following lines. Change the origins in accordance with the VHDL description.

```
ENTRY( _start )

MEMORY
{
   ROM (rx)    : ORIGIN = 0x00000000, LENGTH = 64K
   RAM (rw)    : ORIGIN = 0x20000000, LENGTH = 32K
   IO (rw)     : ORIGIN = 0xf0000000, LENGTH = 16K
}
```

In this setting, the ROM is 64 kB long and the RAM is 32 kB long. Please note that both

ROM and RAM bits may not exceed 3,153,920 bits of onboard RAM. For increased ROM and RAM size, typical values may be 128 kB ROM and 64 kB RAM.

Note that we do not use full address decoding for ROM, RAM and I/O. This means that, for example, the ROM is visible multiple times in the address space. This is called *memory foldback*. For the ROM this is at 64 kB intervals. So the contents of address 0x00000000 is also available at address 0x00010000.

12 Using the bootloader

The design incorporates a hard-coded bootloader with an upload and a simple monitor program. The bootloader is placed in a separate ROM starting at address 0x10000000 and has a maximum length of 4 KB (may be extended). The bootloader cannot be overwritten by an upload. The bootloader can be disabled.

12.1 S-record file

The S-record standard is invented by Motorola in the 1980's. It consists of formatted lines, called records. Each line can be seen as a record. A record starts with `S` followed by a single digit. `S0` is used as header record. This record is ignored by the bootloader (skipped). `S1`, `S2` and `S3` are data record using a 2-byte, 3-byte and 4-byte start address respectively. `S4` is reserved and skipped by the bootloader. `S5` and `S6` are count records and are ignored. `S7`, `S8` and `S9` are termination records with a start address incorporated, with 4-byte, 3-byte and 2-byte address respectively. This start address is used by the bootloader to start the application. Records have a checksum at the end, this checksum is ignored by the bootloader.

12.2 Startup sequence

After loading the design in the FPGA, or after resetting the FPGA, the bootloader starts. It presents itself with a welcome string printed via UART1 at default 115200 bps. Then the bootloader waits for about 5 seconds before starting the application at address 0x00000000. During these 5 seconds, at half second intervals, a `*` is printed via UART1. At the same time, the 10 red leds on the DE0-CV board are lit and dimmed on half second intervals from left (high led) to right (low led). If a character is received within the five seconds, either a S-record file can be uploaded or the bootloader falls to a simple monitor program.

12.3 Uploading an S-record file

A Motorola S-record file can be uploaded with the `upload` program found in the `CODE` directory. It is tested on Linux, Windows is currently not supported. S-record files for all RISC-V programs are generated as part of the `make` process by the RISC-V `objcopy` program. The `upload` program is invoked with:

```
1 upload -d <device> -b <baud> -t <timeout> -s <sleep> -v -j file
```

The default device is `/dev/ttyUSB0` which is the first plugged-in USB-to-U(S)ART converter. The baudrate may be 9600 bps or 115200 bps (default). Timeout is the time the `uplead` program waits for expected data from the bootloader. The time is set in deciseconds (0.1 seconds) intervals. The default value is 10 (1.0 seconds). Sleep is the time the `upload` program waits after transmitting a character tor the bootloader in microseconds intervals. The default value is 0. The option `-v` turns on verbose mode. The option `-j` instructs `upload` to send a "start application" command to the bootloader after the S-record file is uploaded. File must be a valid S-record file.

To upload an S-record file, reset the FPGA or program the FPGA design in the FPGA. Then, within the 5 seconds interval, start the `upload` program with options and file name supplied. If the `upload` programs manages the contact the bootloader, the S-record file will be uploaded. Depending on the size, uploading may take as short as a few seconds to minutes for a large file. As a rule of thumb, about 2400 file characters per seconds are send (at 115200 bps). Make sure that *no* terminal program (e.g. Putty) is active. If the `upload` program cannot contact the bootloader, it exits with an error message. If during sending the records, a response from the bootloader is not read, the `upload` exits with an error message. This is mostly due to an open terminal connection. To start the application after the upload, supply the `-j` option to the `upload` program, otherwise the monitor is started. Before starting the application, UART1 is turned off and the output port is set to 0x00000000 (i.e. all port bits are set to 0).

Using an USB-to-serial adapter can be troublesome, for example when stopping (Ctrl-C) the upload program. There will be characters in the USB buffer and the upload program and the bootloader will be out of sync. Best is to remove the USB-to-serial adapter from the PC and reinsert it again. Then the USB buffer will be empty. During the transmission, the low led of the DE0-CV board will flash rapidly. If not, there is no upload and the USB-to-serial adapter and the DE0-CV board are out of sync.

12.4 Using the monitor

If within the 5 seconds grace period a character is received by the bootloader, the bootloader falls to a simple monitor program. The monitor recognized some simple commands. Each command is terminated by an enter key.

`r`

Run the program at address 0x00000000.

`rw <address>`

Read and print word at address. Address must be on a 4-byte boundary. Data is presented in big endian.

`dw <address>`

Dump 16 words from memory to the terminal. Address must be on a 4-byte boundary. After each word, 4 ASCII characters are printed, if printable. If not printable, a dot is printed. Useful for finding strings in memory. Data is presented in big endian.

`n`

Dump next 16 words from memory to the terminal, and ASCII characters.

`rw <address> <data>`

Write 4-byte data at address. Address must be on a 4-byte boundary. Data must be in big endian.

`h`

A simple help menu is presented.

Note: the capabilities of the monitor may be extended.

12.5 Upload protocol

Uploading an S-record file uses a simple handshake protocol. The `upload` program sends a single exclamation mark (`!`). The bootloader responds with an question mark (`?`) and a newline (`\n`). Now each S-record line is transmitted character by character, including the end-of-line termination character (`\r` and/or `\n`). After a line is processed, the bootloader responds with a question mark and a newline. After all S-record lines are transmitted, the `upload` program either sends a `J` to start the application, or a `#` to start the monitor.

12.6 Implications on the hardware design

The design has a separate ROM that incorporates the bootloader. The original ROM, at address 0x00000000 is extended with a write port, together with the instruction read port and the data read port. In fact, the ROM has become a (program) RAM. Because the Cyclone FPGA ROMs (and RAMs) can only have two ports (out/out or in/out), the original ROM hardware is duplicated (by the synthesizer). This takes up onboard RAM blocks, but very few ALMs (cells).

Note that the ROM can only be (over)written with words on a 4-byte boundary.

13 Future plans (or not) and issues

Some future plans:

- We are *not* planning the C standard.
- The CSR is not conform the standard, but should be.
- Implement clock stretching and arbitration in the I^2C peripheral.
- Adding input synchronization for SPI1/SPI2 and I2C1 peripherals.
- Adding Input Capture for TIMER2.

- Implement an I/O input/output multiplexer for `pina` and `pouta`. This will enable I/O functions to be multiplexed with normal port I/O.
- Smaller (in cells) divide unit.
- Test more functions of the standard and mathematical libraries.
- It is not possible to print `long long` (i.e. 64-bit) using `printf` et al. When using the format specifier `%lld`, `printf` just prints `ld`. This due to lack of support in the `nano` library.
- The `mtime` (MTIMEH:MTIME) registers are currently read only, but should be writable.

A The I/O at a glance

The I/O registers are directly addressable or by a struct. See the listing below.

```
/*
 *     io.h - definitions for the I/O of the
 *            THUAS RISC-V processor
 */

#ifndef _IO_H
#define _IO_H

#ifdef __cplusplus
extern "C" {
#endif

#include <stdint.h>


/* Base address of the I/O */
#define IO_BASE (0xf0000000UL)


/*
 * General purpose I/O
 */
typedef struct {
        volatile uint32_t PIN;
        volatile uint32_t POUT;
} GPIO_struct_t;

#define GPIOA_BASE (IO_BASE+0x00000000UL)
#define GPIOA ((GPIO_struct_t *) GPIOA_BASE)

```

```
#define GPIOA_PIN  (*(volatile uint32_t*)(GPIOA_BASE+0x00000000UL))
#define GPIOA_POUT (*(volatile uint32_t*)(GPIOA_BASE+0x00000004UL))


/* UART1 */
typedef struct {
    volatile uint32_t DATA;
    volatile uint32_t BAUD;
    volatile uint32_t CTRL;
    volatile uint32_t STAT;
} UART_struct_t;

#define UART_BASE (IO_BASE+0x00000020UL)
#define UART1 ((UART_struct_t *) UART_BASE)

#define UART1_DATA (*(volatile uint32_t*)(UART_BASE+0x00000000UL))
#define UART1_BAUD (*(volatile uint32_t*)(UART_BASE+0x00000004UL))
#define UART1_CTRL (*(volatile uint32_t*)(UART_BASE+0x00000008UL))
#define UART1_STAT (*(volatile uint32_t*)(UART_BASE+0x0000000cUL))


/*
 * I2C1
*/
typedef struct {
    volatile uint32_t CTRL;
    volatile uint32_t STAT;
    volatile uint32_t DATA;
} I2C_struct_t;

#define I2C_BASE (IO_BASE+0x00000040UL)
#define I2C1 ((I2C_struct_t *) I2C_BASE)

#define I2C1_CTRL (*(volatile uint32_t*)(I2C_BASE+0x00000000UL))
#define I2C1_STAT (*(volatile uint32_t*)(I2C_BASE+0x00000004UL))
#define I2C1_DATA (*(volatile uint32_t*)(I2C_BASE+0x00000008UL))


/*
 * SPI1, SPI2
 */
typedef struct {
    volatile uint32_t CTRL;
    volatile uint32_t STAT;
    volatile uint32_t DATA;
```

```
76  } SPI_struct_t;
77
78  #define SPI_BASE (IO_BASE+0x00000060UL)
79  #define SPI1 ((SPI_struct_t *) SPI_BASE)
80  #define SPI2 ((SPI_struct_t *) (SPI_BASE + 0x10))
81
82  #define SPI1_CTRL (*(volatile uint32_t*)(SPI_BASE+0x00000000UL))
83  #define SPI1_STAT (*(volatile uint32_t*)(SPI_BASE+0x00000004UL))
84  #define SPI1_DATA (*(volatile uint32_t*)(SPI_BASE+0x00000008UL))
85  #define SPI2_CTRL (*(volatile uint32_t*)(SPI_BASE+0x00000010UL))
86  #define SPI2_STAT (*(volatile uint32_t*)(SPI_BASE+0x00000014UL))
87  #define SPI2_DATA (*(volatile uint32_t*)(SPI_BASE+0x00000018UL))
88
89
90  /*
91   * TIMER1
92   */
93  typedef struct {
94      volatile uint32_t CTRL;
95      volatile uint32_t STAT;
96      volatile uint32_t CNTR;
97      volatile uint32_t CMPT;
98  } TIMER1_struct_t;
99
100 #define TIMER1_BASE (IO_BASE+0x00000080UL)
101 #define TIMER1 ((TIMER1_struct_t *) TIMER1_BASE)
102
103 #define TIMER1_CTRL (*(volatile uint32_t*)(TIMER1_BASE+0x00000000UL))
104 #define TIMER1_STAT (*(volatile uint32_t*)(TIMER1_BASE+0x00000004UL))
105 #define TIMER1_CNTR (*(volatile uint32_t*)(TIMER1_BASE+0x00000008UL))
106 #define TIMER1_CMPT (*(volatile uint32_t*)(TIMER1_BASE+0x0000000cUL))
107
108
109 /*
110  * TIMER2
111  */
112 typedef struct {
113     volatile uint32_t CTRL;
114     volatile uint32_t STAT;
115     volatile uint32_t CNTR;
116     volatile uint32_t CMPT;
117     volatile uint32_t PRSC;
118     volatile uint32_t CMPA;
119     volatile uint32_t CMPB;
120     volatile uint32_t CMPC;
```

```
} TIMER2_struct_t;

#define TIMER2_BASE (IO_BASE+0x000000a0UL)
#define TIMER2 ((TIMER2_struct_t *) TIMER2_BASE)

#define TIMER2_CTRL (*(volatile uint32_t*)(TIMER2_BASE+0x00000000UL))
#define TIMER2_STAT (*(volatile uint32_t*)(TIMER2_BASE+0x00000004UL))
#define TIMER2_CNTR (*(volatile uint32_t*)(TIMER2_BASE+0x00000008UL))
#define TIMER2_CMPT (*(volatile uint32_t*)(TIMER2_BASE+0x0000000cUL))
#define TIMER2_PRSC (*(volatile uint32_t*)(TIMER2_BASE+0x00000010UL))
#define TIMER2_CMPA (*(volatile uint32_t*)(TIMER2_BASE+0x00000014UL))
#define TIMER2_CMPB (*(volatile uint32_t*)(TIMER2_BASE+0x00000018UL))
#define TIMER2_CMPC (*(volatile uint32_t*)(TIMER2_BASE+0x0000001cUL))


/*
 * RISC-V system timer (in I/O)i
 */
#define TIME (*(volatile uint32_t*)(IO_BASE+0x000000f0UL))
#define TIMEH (*(volatile uint32_t*)(IO_BASE+0x000000f4UL))
#define TIMECMP (*(volatile uint32_t*)(IO_BASE+0x000000f8UL))
#define TIMECMPH (*(volatile uint32_t*)(IO_BASE+0x000000fcUL))

typedef struct {
    volatile uint32_t time;
    volatile uint32_t timeh;
} TIME_struct_t;

typedef struct {
    volatile uint32_t timecmp;
    volatile uint32_t timecmph;
} TIMECMP_struct_t;

#ifdef __cplusplus
}
#endif

#endif
```

B Port I/O

The processor is equipped with a single 32-bit input and 32-bit output port. There is no data direction register. This may be changed to using bi-direction port pins. Note that all accesses on the I/O are in Big Endian. This means that bit 31 of the input will be placed in bit 31 of the used variable.

To set the outputs, use:

```
uint32_t output = 0xff00ff00;

GPIOA->POUT = output;
```

Modifying bits of a I/O register must be done by a read-modify-write cycle. This is *not* atomically handled and can interfere with interrupts! For example, to set bit 2 of POUT, use:

```
GPIOA->POUT |= 0x04;
```

C UART1 Code

UART1 can send and receive data with one start bit, 7/8/9 data bits, N/E/O parity and 1 or 2 stop bits. Transmission is tested with a baud rate of 9600 bps, 115200 bps and 230400 bps. Send and receive speeds are equal as is the number of data bits, parity and the number of stop bits. There are no auxiliary control signals (e.g. RTS and CTS). There is no embedded FIFO to buffer incoming data. UART1 is programmable using I/O registers, see Appendix G. Note that using a system frequency of 50 MHz, the baud rate cannot be lower than 763 bps, because the baud rate generator uses a 16-bit register.

To initialize UART1, use the code in the listing below:

```
/* Frequency of the DE0-CV board */
#define F_CPU (50000000UL)
/* Transmission speed */
#define BAUD_RATE (9600UL)

/* Initialize the Baud Rate Generator */
void UART1_init(void)
{
    /* Set baud rate generator */
    UART1->BAUD = F_CPU/BAUD_RATE-1;
}
```

To send a single character with waiting, use the code in the listing below:

```
/* Send one character over UART1 */
void uart1_putc(int ch)
{
    /* Transmit data */
    UART1->DATA = (uint8_t) ch;

    /* Wait for transmission end */
    while ((UART1->STAT & 0x10) == 0);
}
```

To send a null-terminated string, use the code in the listing below:

```
/* Send a null-terminated string over UART1 */
void uart1_puts(char *s)
{
    if (s == NULL)
    {
        return;
    }

    while (*s != '\0')
    {
        uart1_putc(*s++);
    }
}
```

To wait for a character reception, use the code in the listing below:

```
/* Get one character from UART1 in
 * blocking mode */
int uart1_getc(void)
{
    /* Wait for received character */
    while ((UART1->STAT & 0x04) == 0);

    /* Return 8-bit data */
    return UART1->DATA & 0x000000ff;
}
```

To receive a string from UART1, including some simple line editing, use the code in the listing below:

```
/* Gets a string terminated by a newline character from UART1
 * The newline character is not part of the returned string.
 * The string is null-terminated.
 * A maximum of size-1 characters are read.
 * Some simple line handling is implemented */
int uart1_gets(char buffer[], int size)
{
    int index = 0;
    char chr;

    while (1) {
        chr = uart1_getc();
        switch (chr) {
            case '\n':
            case '\r':  buffer[index] = '\0';
                    uart1_puts("\r\n");
```

```
                    return index;
                    break;
            /* Backspace key */
            case 0x7f:
            case '\b':  if (index>0) {
                            uart1_putc(0x7f);
                            index--;
                        } else {
                            uart1_putc('\a');
                        }
                        break;
            /* control-U */
            case 21:    while (index>0) {
                            uart1_putc(0x7f);
                            index--;
                        }
                        break;
            /* control-C */
            case 0x03:      uart1_puts("<break>\r\n");
                        index=0;
                        break;
            default:    if (index<size-1) {
                            if (chr>0x1f && chr<0x7f) {
                                buffer[index] = chr;
                                index++;
                                uart1_putc(chr);
                            }
                        } else {
                            uart1_putc('\a');
                        }
                        break;
        }
    }
    return index;
}
```

When printing a C newline, you have to use:

```
uart1_puts("\r\n");
```

This will set the cursor to the beginning of a new line. Here, `\r` returns the cursor to the beginning of the current line and `\n` advances the cursor to the next line. Some terminal emulation programs can be instructed to move to the beginning of a new line with only `\n`.

For working with the UART on board of the processor, you need an USB-to-U(S)ART device with TTL (3.3 V) converter. An example is shown in Figure 8.

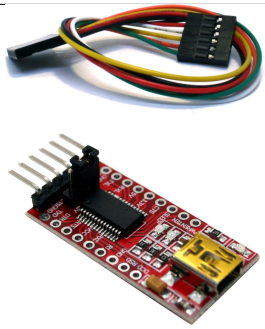


Figure 8: *An USB-to-U(S)ART converter. Make sure that the voltages do not exceed 3.3 V.*

D I²C code

The baud rate prescaler must be loaded with the number of system clock cycles for **one-half** bit time for Standard mode, and **one-third** bit time for Fast mode. Note that the prescaler is in the CTRL register and must be preserved:

```
/* Standard mode, exact number */
#define TRAN_SPEED ((F_CPU/2UL/100000UL)-1)
I2C1->CTRL = TRAN_SPEED << 16;
/* Fast mode, round up to integer */
#define TRAN_SPEED (((F_CPU/3UL/400000UL)-1)+1)
I2C1->CTRL = (TRAN_SPEED << 16) | (1 << 2);
```

Note that for a 50 MHz system clock frequency, an exact count is achieved for Standard Mode (250), but not for Fast mode (41.6667), so the rounding must be up.

To send a startbit, before an address byte is send, use:

```
I2C1->CTRL |= (1 << 9);
```

To send an address byte, with read-write bit, left-shift the address by 1 and add the read/write bit:

```
I2C1->DATA = (ADDR << 1) | RWBIT;
while ((I2C1->STAT & 0x08) == 0x00);
```

To check for acknowledge, use:

```
if (I2C1->STAT & (1 << 5)) {
    uart1_puts("ACK failed!\r\n");
} else {
    uart1_puts("ACK ok\r\n");
}
```

To send a byte and wait for transmission complete, use:

```
I2C1->DATA = some_data;
while ((I2C1->STAT & 0x08) == 0x00);
```

After the address is transmitted, and the read-write bit is set to write, the controller changes to receive mode. It will then constantly send clock pulses. To stop transmission, the send-stopbit must be activated on the last byte to receive.

```
/* Controller is receiving */
while ((I2C1->STAT & 0x10) == 0x00);
some_variable = I2C1->DATA;

/* Set STOP generation */
I2C1->CTRL |= (1 << 8);
/* Wait for data transmission completed */
while ((I2C1->STAT & 0x10) == 0x00);
some_variable = I2C1->DATA;
```

To check if a target is listening on a address, send address (with read or write) and send a startbit and stopbit:

```
/* Set START and STOP generation */
I2C1->CTRL |= (1 << 9) | (1 << 8);

/* Write address + write bit */
I2C1->DATA = (some_address << 1) | 0;
```

E TIMER1 code

Based on a frequency of 50 MHz, the following code will set TIMER1 interrupt on 0,5 s intervals:

```
/* Activate TIMER1 with a cycle of 2 Hz */
/* for a 50 MHz clock. Use interrupt. */
TIMER1->CMPT = 24999999;
/* Bit 0 = enable, bit 4 is interrupt enable */
TIMER1->CTRL = (1<<4)|(1<<0);
```

F The external `time` registers

The `time` registers (MTIME, MTIMEH, MTIMEMCP and MTIMECMPH) can be accessed via the I/O and are therefore memory mapped. These registers are shadowed by the CSR. The following code reads in the current time and increments the compare registers with a certain *delta*. Whenever TIMEH:TIME is greater than or equal to TIMEH:TIME, an interrupt request is asserted. Negating the interrupt request is accomplished by writing a value greater than the time registers to the compare registers.

```
void external_timer_handler(void)
{
    register uint32_t time;
```

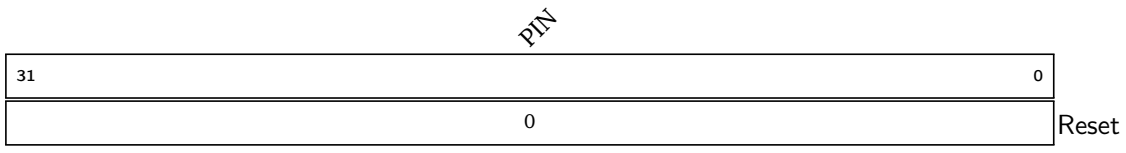
```
    register uint32_t timeh;

    /* Fetch current time */
    do {
        timeh = MTIMEH;
        time  = MTIME;
    } while (timeh != MTIMEH);

    /* Fetch current time */
    register uint64_t cur_time = ((uint64_t)timeh << 32) | (
       ↪uint64_t)time;

    /* Add delta */
    cur_time += external_timer_delta;
    /* Set TIMECMP to maximum */
    MTIMECMPH = -1;
    MTIMECMP = -1;
    /* Store new TIMECMP */
    MTIMECMP = (uint32_t)(cur_time & 0xffffffff);
    MTIMECMPH = (uint32_t)(cur_time>>32);
    /* Flip output bit 1 (led) */
    GPIOA->POUT ^= 0x2;
}
```

Normally, this code is placed in the interrupt handler. These registers are read-only shadowed to the CSR time registers.

G I/O registers

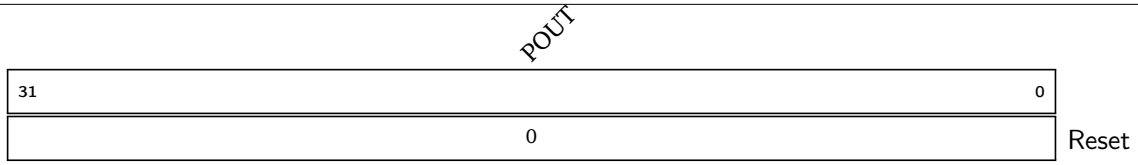
This is a list of currently supported I/O addresses. The default start address is 0xF0000000. The offset is given in bytes. Note that the I/O can only be accesses on 4-byte boundaries and on word size accesses.

G.1 GPIOA – General Purpose I/O



Register G.1: PORT A INPUT REGISTER GPIOA_PIN *(0x00)*

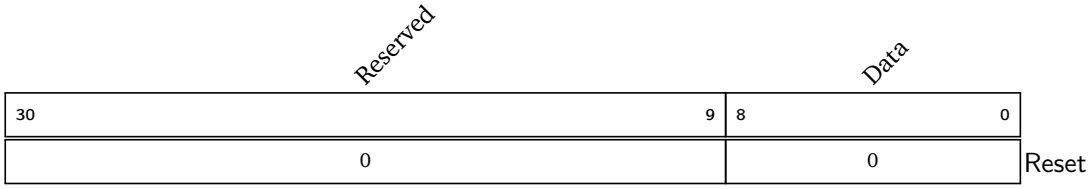
Note: This I/O register can only be read.



Register G.2: PORT A OUTPUT REGISTER GPIOA_POUT *(0x04)*

Write	The data is written to the output pins.
Read	The last entered data is read back.

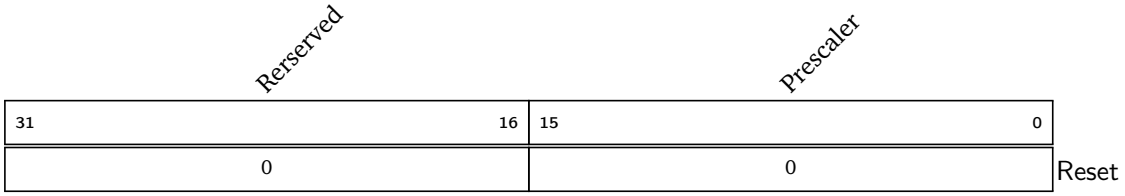
G.2 UART1 – Universal Asynchronous Receiver/Transmitter



Register G.3: UART1 DATA REGISTER UART1_DATA *(0x20)*

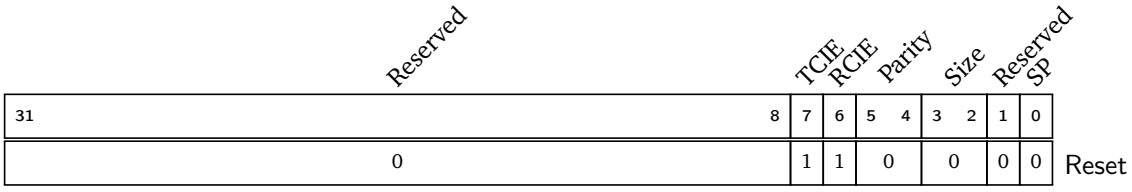
Write	The data is written to an internal buffer and transmitted.
Read	The last received data is read.

Size depends on the Size field in the UART1 Control Register.



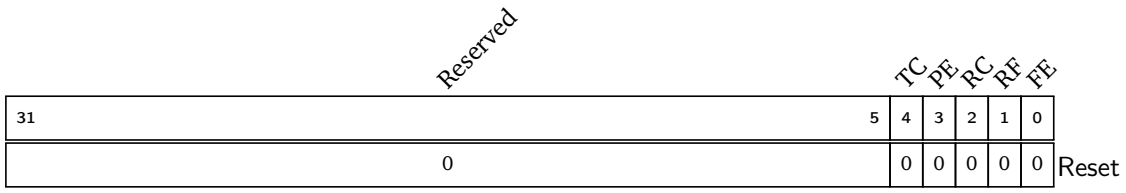
Register G.4: UART1 BAUD RATE REGISTER UART1_BAUD *(0x24)*

Prescaler $\text{Baud rate} = \dfrac{f_{system}}{\text{prescaler} + 1}$



Register G.5: UART1 CONTROL REGISTER UART1_CTRL *(0x28)*

TCIE	Transmit character interrupt enable.
RCIE	Receive character interrupt enable.
Parity	00: none, 10: even, 11: odd.
Size	00: 8 bits, 10: 9 bits, 11: 7 bits, excluding the parity.
SP	0: one stop bit, 1: two stop bits.

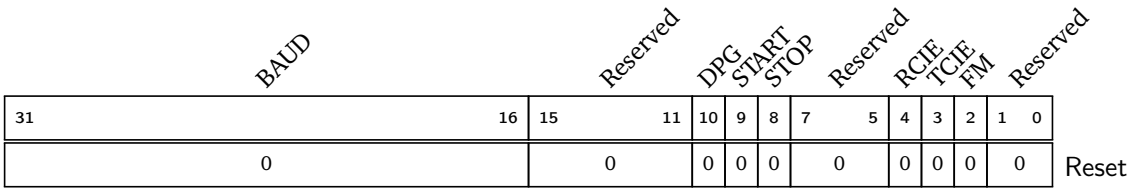


Register G.6: UART1 STATUS REGISTER UART1_STAT *(0x2c)*

TC	Transmit completed. Set directly to 1 when a character was transmitted. Automatically cleared when writing new character to the data register or when writing 0 in the TC bit in UART1_STAT.
PE	Parity error. Set to 1 if parity is enabled and there is a parity error while receiving. Automatically cleared when data register is read or when writing 0 in the PE bit in UART1_STAT.
RC	Receive completed. Set to 1 when a character was received. Automatically cleared when data register is read or when writing 0 in the RC bit in UART1_STAT.
RF	Receive failed. Set to 1 when failed receiving (invalid start bit). Automatically cleared when data register is read or when writing 0 in the RF bit in UART1_STAT.
FE	Frame error. Set to 1 when a low is detected at the position of the (first) stop bit. Automatically cleared when data register is read or writing a 0 in the FE bit in UART1_STAT.

G.3 I2C1 – Inter-Integrated Circuit master-only controller

General purpose I^2C peripheral, with programmable baud rate prescaler, start- and stop-bit generation, no clock stretching, no arbitration, Standard mode (Sm) only.



Register G.7: I2C1 CONTROL REGISTER I2C1_CTRL *(0x40)*

BAUD	Baud rate prescaler. Number of system clock pulses minus

1 for **one-half** bit time. Note: because of the 50 MHz system frequency, the lowest I^2C clock frequency is 763 Hz.

DPG Disable STOP generation after Acknowledge Fail. Can be used to send a repeated START.

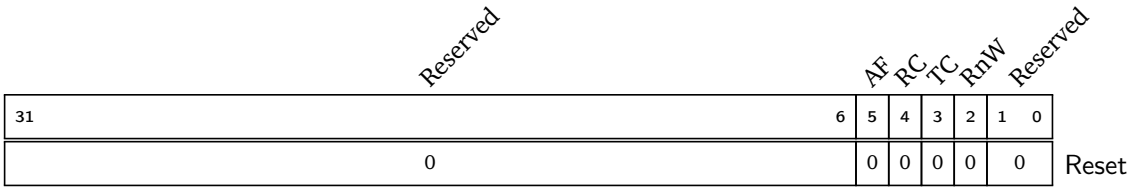
START Send a START on next byte send. Cleared by hardware when transmission ends.

STOP Send a STOP after next byte send or received. Cleared by hardware when transmission ends.

RCIE Receive Complete interrupt enable.

TCIE Transmit Complete interrupt enable.

FM Fast mode 2:1 (SCL 2/3 low, 1/3 high)



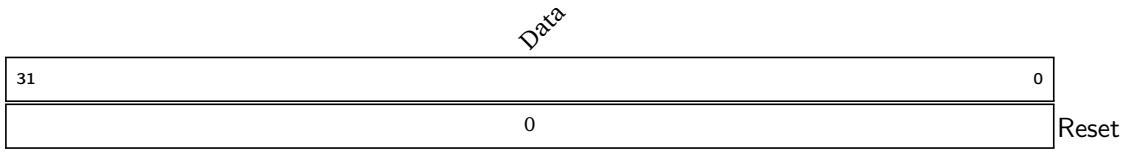
Register G.8: I2C1 STATUS REGISTER I2C1_STAT *(0x44)*

AF Acknowledge Fail, set when no target responded.

RC Receive Complete, including sending STOP. Cleared by hardware when I2C1_DATA is read.

TC Transmission Complete, including sending STOP. Cleared by hardware when I2C1_DATA is written.

RnW Indicates transmitting (0) or receiving (1)



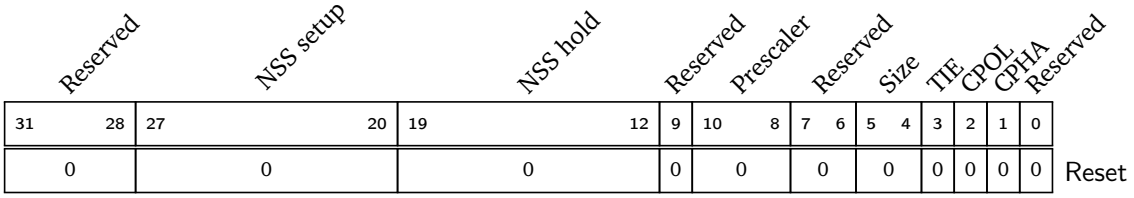
Register G.9: I2C1 DATA REGISTER I2C1_DATA *(0x48)*

Write The data is written to an internal buffer and transmitted.
Read The last received data is read.

Data size depends on the Size field in the SPI1 Control Register. Data is right aligned.

G.4 SPI1 – Serial Peripheral Interface

General purpose SPI master peripheral, with prescaler, 8/16/24/32 bits data exchange, hardware NSS and interrupt.



Register G.10: SPI1 CONTROL REGISTER SPI1_CTRL *(0x60)*

NSS setup Number of system clock pulses after NSS active before transfer starts

NSS hold Number of system clock pulses before NSS inactive after transfer ends

Prescaler
000 /2
001 /4
010 /8
011 /16
100 /32
101 /64
110 /128
111 /256

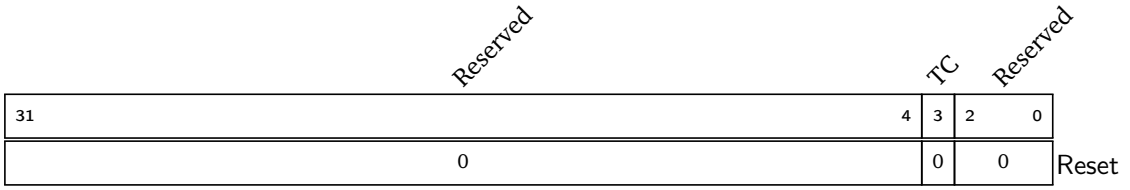
Note: because of the 50 MHz system frequency, the lowest SPI clock frequency is 195.3125 kHz.

Size
00 8 bits
01 16 bits
10 24 bits
11 32 bits

TIE Transfer complete interrupt enable

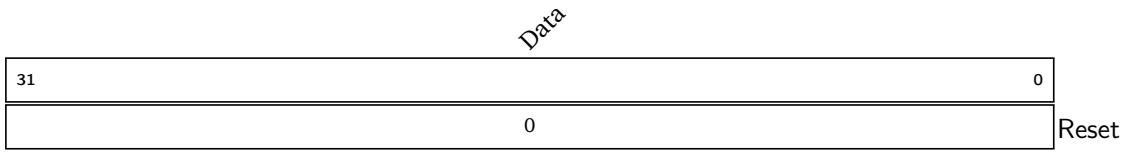
CPOL Clock polarity

CPHA Transfer phase



Register G.11: SPI1 STATUS REGISTER SPI1_STAT *(0x64)*

TC Transfer complete



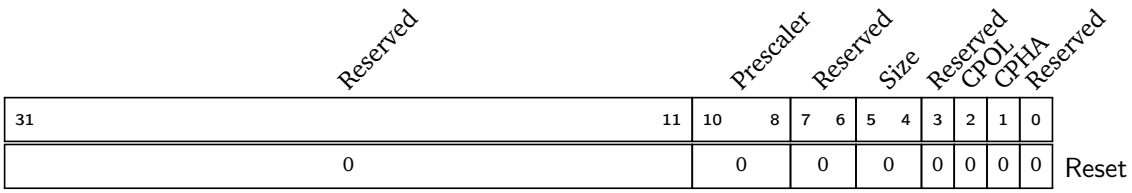
Register G.12: SPI1 DATA REGISTER SPI1_DATA *(0x68)*

Write The data is written to an internal buffer and transmitted.
Read The last received data is read.

Data size depends on the Size field in the SPI1 Control Register. Data is right aligned.

G.5 SPI2 – Serial Peripheral Interface

SPI master peripheral dedicated for SD card access, with prescaler and 8/16/24/32 bits data exchange.



Register G.13: SPI2 CONTROL REGISTER SPI2_CTRL *(0x70)*

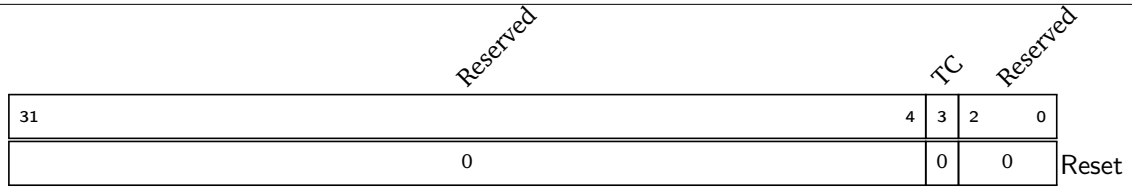
Prescaler
000 /2
001 /4
010 /8
011 /16
100 /32
101 /64
110 /128
111 /256

Note: because of the 50 MHz system frequency, the lowest SPI clock frequency is 195.3125 kHz.

Size
00 8 bits
01 16 bits
10 24 bits
11 32 bits

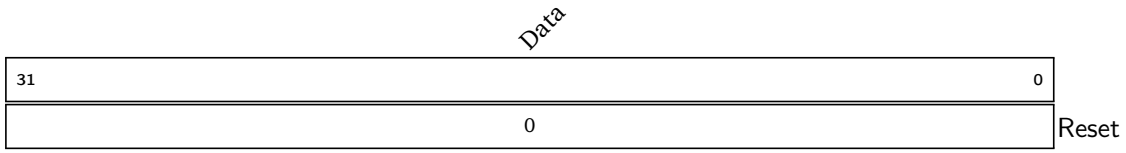
CPOL Clock polarity

CPHA Transfer phase



Register G.14: SPI2 STATUS REGISTER SPI2_STAT *(0x74)*

TC Transfer complete



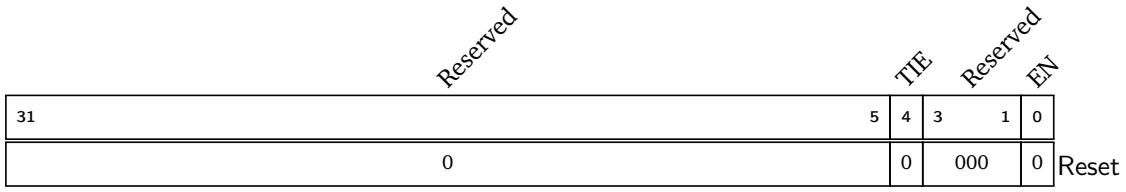
Register G.15: SPI2 DATA REGISTER SPI2_DATA *(0x78)*

Write The data is written to an internal buffer and transmitted.
Read The last received data is read.

Data size depends on the Size field in the SPI2 Control Register. Data is right aligned.

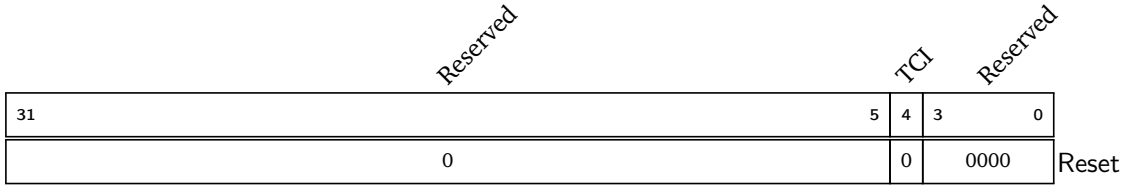
G.6 TIMER1 – a simple timer

Simple 32-bit timer peripheral for time base generation, with interrupt.



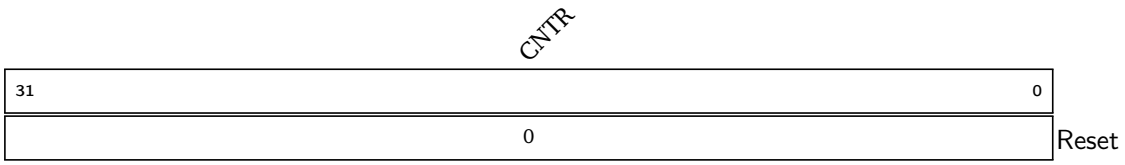
Register G.16: TIMER1 CONTROL REGISTER TIMER1_CTRL *(0x80)*

EN Enable the timer
TIE Timer compare match interrupt enable



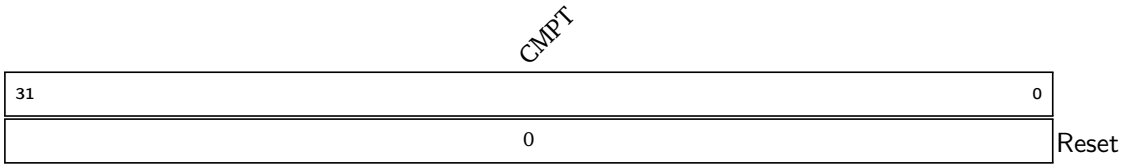
Register G.17: TIMER1 STATUS REGISTER TIMER1_STAT *(0x84)*

TCI Timer compare match interrupt. Set to 1 on compare match between the timer Count register and the Compare Match register. Must be cleared by software by writing a 0.



Register G.18: TIMER1 COUNT REGISTER TIMER1_CNTR *(0x88)*

CNTR This register holds the counted clock pulses on the timer. This register may be written by software.



Register G.19: TIMER1 COMPARE TIMER T REGISTER TIMER1_CMPT *(0x8c)*

CMPT This register holds the value at which the counter register is compared. On CNTR compares to greater than or equal to CMPT, the counter register will be cleared and the TCI flag will be set (both in the next clock cycle).

G.7 TIMER2 – a more elaborate timer

General purpose 16-bit timer with Output Compare and PWM generation capabilities, preload and interrupts.

FOCC	FOCB	FOCA	FOCT	PHAC	MODEC	PHAB	MODEB	PHAA	MODEA	PHAT	MODET	PREC	PREB	PREA	PRET	CIE	BIE	AIE	TIE	OS	Reserved	EN	
31	30	29	28	27	26 24	23	22 20	19	18 16	15	14 12	11	10	9	8	7	6	5	4	3	2 1	0	
0	0	0	0	0	000	0	000	0	000	0	000	0	0	0	0	0	0	0	0	0	00	0	Reset

Register G.20: TIMER2 CONTROL REGISTER TIMER2_CTRL *(0x90)*

FOCC Force Output Compare match C.
FOCB Force Output Compare match B.
FOCA Force Output Compare match A.
FOCT Force Output Compare match T.
PHAC Register C start phase.
MODEC Register C mode.

PHAB	Register B start phase.
MODEB	Register B mode.
PHAA	Register A start phase.
MODEA	Register A mode.
PHAT	Register T start phase.
MODET	Register T mode.
PREC	Enable compare register C preload.
PREB	Enable compare register B preload.
PREA	Enable compare register A preload.
PRET	Enable compare register T preload.
CIE	Timer compare match C interrupt enable
BIE	Timer compare match B interrupt enable
AIE	Timer compare match A interrupt enable
TIE	Timer compare match T interrupt enable
OS	One-shot mode
EN	Enable the timer

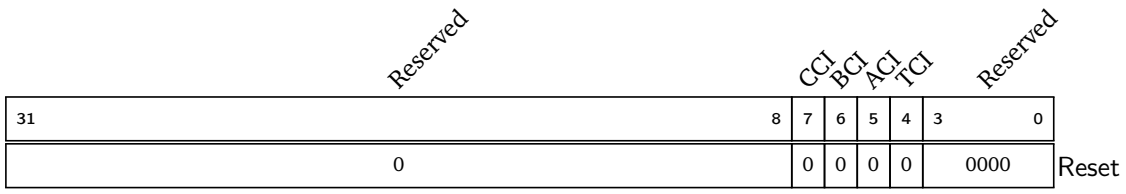
If none of the FOC*x* bits are 1, MODET and MODEA/B/C have the following meaning:

000 Output off
001 Toggle on compare match
010 Set high on compare match
011 Set low on compare match
100 Edge-aligned PWM (only A/B/C, for T not allowed)
101 not allowed
110 not allowed
111 not allowed

If at least one of the FOC*x* bits is 1, MODET and MODEA/B/C have the following meaning:

000 not allowed
001 Toggle output compare
010 Set high output compare
011 Set low output compare
100 not allowed
101 not allowed
110 not allowed
111 not allowed

In this case, the CTRL register is not written and keeps its original setting.



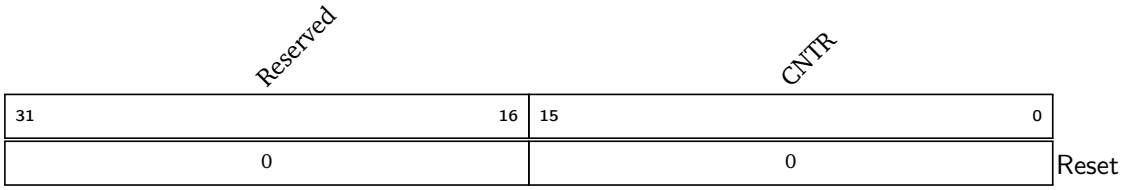
Register G.21: TIMER2 STATUS REGISTER TIMER2_STAT *(0x94)*

CCI Timer compare match A interrupt. Set to 1 on compare match between the timer Count register and the Compare Match C register. Must be cleared by software by writing a 0.

BCI Timer compare match A interrupt. Set to 1 on compare match between the timer Count register and the Compare Match B register. Must be cleared by software by writing a 0.

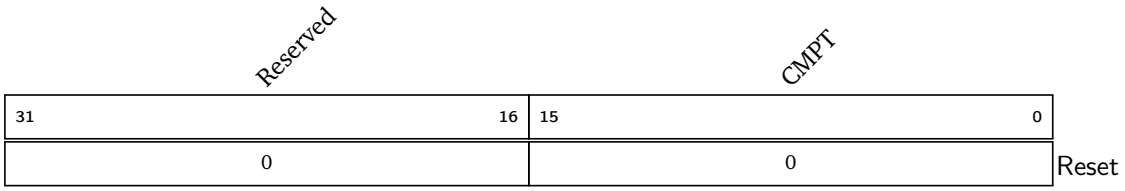
ACI Timer compare match A interrupt. Set to 1 on compare match between the timer Count register and the Compare Match A register. Must be cleared by software by writing a 0.

TCI Timer compare match T interrupt. Set to 1 on compare match between the timer Count register and the Compare Match T register. Must be cleared by software by writing a 0.



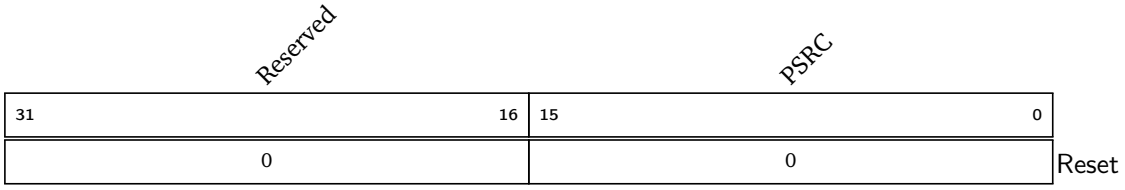
Register G.22: TIMER2 COUNT REGISTER TIMER2_CNTR *(0x98)*

CNTR This register holds the counted clock pulses on the timer. This register may be written by software. Rolls over when CNTR compare greater than or equal to CMPT on the next clock cycle.



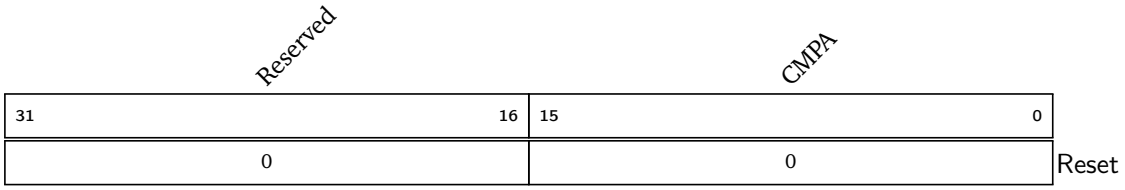
Register G.23: TIMER2 COMPARE TIMER T REGISTER TIMER2_CMPT *(0x9c)*

CMPT This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPT, the Count register will be cleared and the TCI flag will be set (both in the next clock cycle).



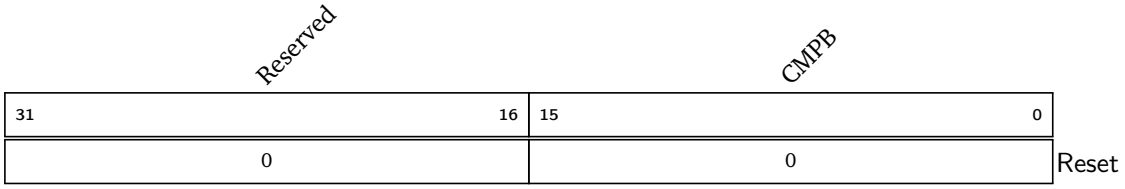
Register G.24: TIMER2 PRESCALER REGISTER TIMER2_PRSC *(0xa0)*

PRSC This register holds the prescaler of the timer. This register may be written by software. Whenever the internal prescaler is equal to or greater than this register, the internal prescaler is reset. This register should only be written when the timer is stopped. Writing this register resets the internal prescaler.



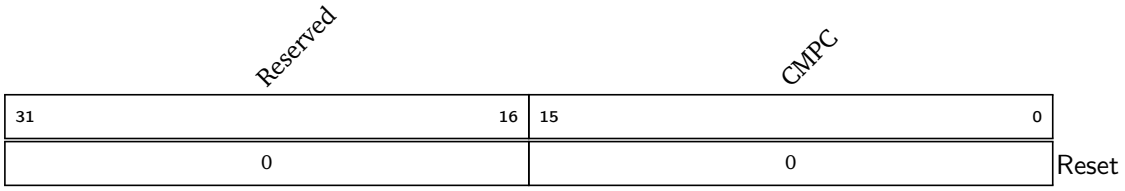
Register G.25: TIMER2 COMPARE TIMER A REGISTER TIMER2_CMPA *(0xa4)*

CMPA This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPA, the ACI flag will be set in the next clock cycle.



Register G.26: TIMER2 COMPARE TIMER B REGISTER TIMER2_CMPB *(0xa8)*

CMPB This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPB, the BCI flag will be set in the next clock cycle.

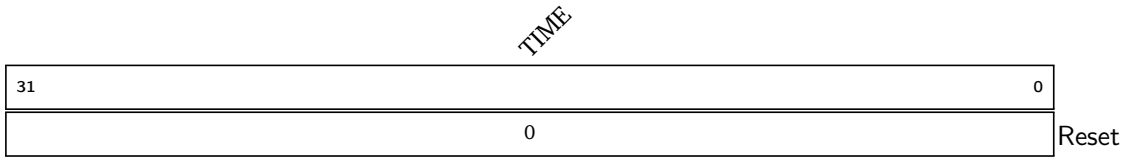


Register G.27: TIMER2 COMPARE TIMER C REGISTER TIMER2_CMPC *(0xac)*

CMPC This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPC, the CCI flag will be set in the next clock cycle.

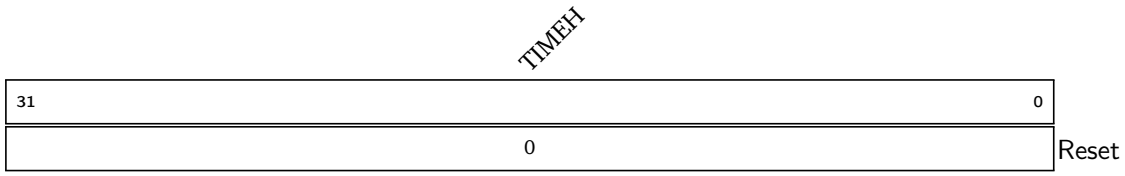
G.8 TIME – RISC-V system timer

Note: the external timer interrupt has to be enabled by writing a 1 to `mie.MTIE`.



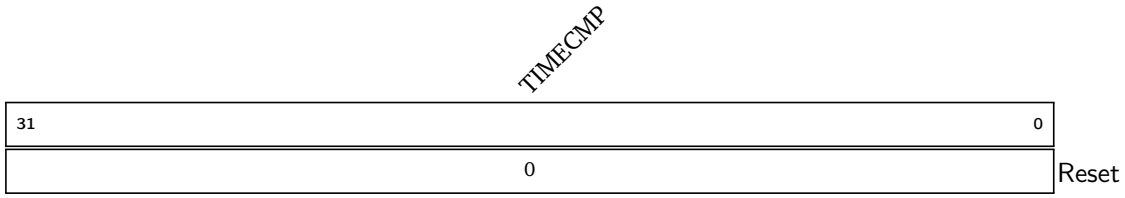
Register G.28: TIME EXTERNAL TIMER REGISTER TIME *(0xf0)*

This register holds the low 32 bits of the external timer. Currently read-only.



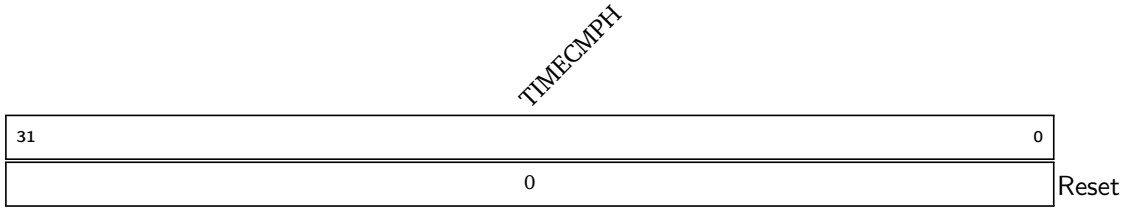
Register G.29: TIMEH EXTERNAL TIMER REGISTER TIME *(0xf4)*

This register holds the upper 32 bits of the external timer. Currently read-only.



Register G.30: TIMECMP EXTERNAL TIMER COMPARE REGISTER TIMECMP *(0xf8)*

This register holds the low 32 bits of the external timer compare register.



Register G.31: TIMECMPH EXTERNAL TIMER COMPARE REGISTER TIMECMP *(0xfc)*

	This register holds the upper 32 bits of the external timer compare register.