UCSC extension Silicon Valley

University of California Santa Cruz
Course VLSI.X400/18966
Advanced Verification with SystemVerilog OOP Testbench

Instructor:

Benjamin Ting, MSEE

Course Description:

SystemVerilog is the new IEEE-1800 standard combining the hardware description language and hardware verification language. This course focuses on the use of advanced verification features in SystemVerilog. Students will learn the step-by-step processes of creating flexible verification components, which form the basis of modern industry-standard methodologies such as UVM and OVM. They will also gain experience developing an industrial-strength object-oriented programming (OOP) testbench that is layered, configurable, constrained-random, and coverage-driven.

The course starts with a brief review of SystemVerilog language semantics and simulation fundamentals such as event ordering, delta cycles and race conditions, which will then feed into closely related entities in program block, clocking block, and interfaces. Students will learn how to develop a complete verification environment by building flexible testbench components via the use of virtual interfaces, classes, mailboxes, dynamic arrays, and queues, etc. Functional coverage in the form of covergroup, coverpoint, and SystemVerilog Assertion (SVA), will round up the development of a complete verification environment. You will become familiar with the flexibility of an OOP-centric technique, the power of constrained random verification and the use of functional coverage tools to ensure the success of a verification project.

Concepts introduced in class are reinforced in the lab. In addition to in-class hands-on labs and weekly take-home assignments, students will work on a

required project to build an advanced OOP testbench and verification environment for a selected application (such as a 10G Ethernet MAC design), with transaction-level and layered architecture. Students will form a project team, create a testplan, develop an OOP-centric verification environment, perform functional coverage, and submit a complete project report.

Topics include:

- Event scheduler, delta cycles, race conditions, and related topics in program block, clocking block and SystemVerilog interface
- Virtual interface and classes: deployment of classes in OOP Testbench
- Stimulus generation technique
- Constraint inheritance and constraint layering in OOP testbench
- Functional coverage class as a testbench component
- Simulation phases

Skills Needed:

A course in SystemVerilog and knowledge of VHDL, Verilog, C/C++, and some hardware verification experience

Prerequisite:

VLSI.X412: SystemVerilog Essentials

Performance Evaluation:

Weekly homework will be assigned. Students are expected to complete them on a timely manner. Homework submission, however, is optional. Student's grade will be based entirely on a required OOP Testbench Project

Students will be graded on a curve

Project:

A project is required as part of this course. Details will be provided in the class

Workbook & Lecture Materials:

Instructor will provide information on where to obtain class materials

UCSC Extension Policies:

Examination and Homework Return Policy

For applicable homework and examinations that you wish to receive back, please bring a self-addressed stamped envelope to the instructor on the final day of class or send one with your submitted project/exam.

Academic Integrity Policy:

UCSC Extension, as a unit of the University of California Santa Cruz, takes academic integrity very seriously. All forms of academic misconduct, including but not limited to, cheating, fabrication, plagiarism, or facilitating academic dishonesty are grounds for student discipline. Unless otherwise indicated by the course instructor, assignments must be individual efforts. It is not acceptable to copy (verbatim or even with minor changes) whole sections of a book, article or Internet resource, and submit them as one's own work. References should be listed and direct quotes indicated as such, with the author cited.

Grading Options:

When students enroll, letter grading **(A, B, C, D or F),** is the default. The Credit (CR)/Not for Credit (NC) options are available only to students in good academic standing. Students may elect to take courses for a letter grade, Credit (CR)/Not for Credit (NC). However, requests for CR/NC grades must be submitted before the last scheduled day of the course. A passing letter-grade is required in order for a course to be applicable to a certificate.

If a student does not intend to, or for any reason cannot, complete a course s/he enrolled in, it is the student's obligation to formally notify the instructor and UCSC Extension of this change in standing before the last day of class. All withdrawal requests must be submitted using the form on the Web **http://www.ucsc-extension.edu/student-services/forms/withdrawal.** Failure to follow this policy and associated guidelines will result in the entry of a default grade of "F" on the student's permanent record. Please see Student Services webpage for links to the complete description of grading options **http://www.ucsc-extension.edu/student-services/grading.**