Computer Systems Design - Lab 4

Handed Out: Thursday, 29 Jan. 2015
Due: Thursday, 5 Feb. 2015, 11:00 AM
Submit via USF Canvas
This is an team assignment. Teams can have up to 3 members
Late submissions will not be accepted

Objective:

To design and construct a Finite State Machine that can be synthesized to an FPGA device, and to test the design to ensure correct functionality.

Problem:

Design a controller FSM for a soft drink vending machine.

Description:

You are to design an FSM for use as a controller for a vending machine. The system has five (5) inputs: *quarter*, *nickel*, *dime*, *soda*, and *diet*. The *quarter* input will go high, then go low when a 25¢ coin is added to the machine. The *dime* and *nickel* inputs work in a similar manner for the 10¢ and 5¢ coins. The sodas cost 45¢each. The user presses the *soda* button to select a regular soda, and the *diet* button to select a diet soda. The *GiveSoda* output will pulse high, then low when a regular soda is released. Similarly, the *GiveDiet* output will pulse high, then low when a diet soda is released. The *Change* output will pulse high, then low once for every 5¢ returned in change. Once the user has inserted enough money to by a soda, the user cannot insert more money. You may wish to insert an additional output, *status*, to indicate whether the machine is currently accepting money. Choose a Moore or Mealy format as appropriate.

Your design must be a *pure FSM*. This means that there should be no complex operations (addition, subtraction) in your design. It must function solely on states and transitions.

The output pulses must stay **high** for a minimum of one-half of a clock cycle. The outputs will be directed to the bank of GPIO LEDs. You may select the exact mapping of outputs to LEDs. In your report, clearly list the input/button assignments.

The inputs will be taken from the Directional Buttons. These buttons will require a **debounce** circuit to operate correctly. You may select the exact mapping of inputs to buttons. In your report, clearly list the output/LED assignments.

A Xilinx training video covering Verilog FSM design has been linked on Canvas. (Under: Modules→Verilog→Web Resources) Additionally, Xilinx ISE contains code templates for Mealy and Moore finite state machines. They can be found under the [**Tools → Language Templates**] menu.

- **Part A** [*25 points*]: Design the Vending Machine FSM and verify it in simulation.
- **Part B** [*50 points*]: Synthesize the design and verify its functionality on the FPGA.

Design Constraints: The designs must properly function given the following constraints:

- The designs must both function correctly in simulation *and* on the FPGA board.
- The design must utilize a pure FSM.
- All five inputs utilize the directional buttons.
- The inputs must be properly debounced. (This will be discussed in lab)
- All three outputs utilize the GPIO LED bank.
- The 100MHz clock is used as the system clock.
- Multiple simultaneous button presses should be ignored

Lab Report: You must submit a written lab report. The lab report will consist of (at least) the following sections:

- **Cover:** Include a list of team members (with U#'s) and work distribution for each team member.
- **Introduction:** In your own words, briefly describe the lab assignment.
- **Design:** Briefly describe the structure and function of your design. Discuss your design decisions and any problems you encountered during the design process.
- **Testing:** Discuss how you verified the functionality of the design. This should include a description of your testbench and test vectors, and a brief justification of the completeness of the tests you chose. Also discuss any problems you had with the testing process.
- **Synthesis:** Discuss the synthesis process and results, including any warnings or errors encountered. Describe the function of your design on the FPGA board and discuss how you verified the functionality. Be descriptive.
- **Results:** Discuss the results of the design process, testing and the assignment overall. This should include a discussion of any simulation results and an overall analysis of your design.
- **Conclusion:** Briefly summarize your accomplishments and discuss any failures. Briefly discuss your thoughts, concerns, and feedback for this assignment. If you choose, you may rant about the software, programming language, the assignment itself, or the TAs responsible for the lab.

All reports MUST be submitted in PDF format. No exceptions.

Deliverables: Submit your report PDF and the code ZIP file separately on Canvas. The PDF should be named <netid>_lab04_report.pdf. To generate the code ZIP file:

- Select **Project** → **Cleanup Project Files...** from the menu.
- Select **OK** on the pop-up box.
- Select **Project** → **Archive...** from the menu.
- On the new window, make sure **Exclude Generated Files From Archive** is *selected*.
- Choose a location for the archive, name it <netid>_lab04_src.zip.
- Select **OK**

Insert any images and waveforms into the report PDF. Submit the report PDF and source code ZIP separately on Canvas. If you wish, you may include copies of all images in a separate ZIP file, submitted through Canvas. Name it <netid>_lab04_images.zip.

No re-grading will be done for failure to follow the guidelines. Points will be lost, never to return.