

*CDA 4203/4203L*  
*Spring 2015*  
**Computer System Design**

*Final Project Report*  
*Due by 5pm, Thursday, 30th April*

Today's Date:	4/28/15		
Team Member Names:	Sean Murphy	Austin Matthew	Jesse Walton
Team Member U #'s:	U49850246	U89904116	U89823440
Work Distribution	Briefly explain each team member's contribution.  Sean Murphy – Memory, Integration, bug fixes  Austin Matthew – LCD, menu system  Jesse Walton – Audio, Report		

**Feedback:** Your feedback is extremely important to improve the mini-project for future course offerings.

Total Number of Person Hours Spent:	<i>Estimate the number of hours spent by each team member and add the three numbers.</i>  Sean Murphy: $2 + 2 + 6 + 8 + 14 + 12 = 44$  Austin Matthew: $2 + 2 + 6 + 8 + 14 + 12 = 44$  Jesse Walton: $2 + 2 + 6 + 8 + 12 + 12 = 42$  Total: $44 + 44 + 42 = 130$ hours
Exercise Difficulty: (Easy, Average, Hard)	Hard
Issues You ran into:	<i>List all problem/issues you faced while doing this project.</i>  <i>(please use bulletized list)</i> <ul style="list-style-type: none"><li>• Audio codec – typo</li><li>• Verilog (General) – implementation and testing</li><li>• LCD – timing issues, logic</li></ul>
Any Suggestions to improve this project:	<i>Better resources and training on debugging workflow</i>  <i>Introduce components in prior labs.</i>  <i>Training on best practices of how to use new components</i>

# Overview

**Describe the overall functionality of the system. Describe any and all relevant interfaces. Maximum 1 page.**

The system uses the ram, ac97, buttons and lcd to implement an audio recorder that can record and play back 8 messages at up to 4 minutes each. This is accomplished by using a top level Verilog module to handle IO and to connect all sub-modules together.

**Powering On:** When the system is turned on, the user is greeted with a welcome message that remains on the screen until a button is pressed.

**Top Menu:** Immediately after a button is pressed, the welcome menu is removed and the top menu is shown. The menu items are: **Play, Record, Delete, Delete All** and **Volume**. The user can navigate to each item by pressing the navigation buttons.

**Play:** Selecting play brings you to a message select screen and allows you to select messages 1 through 8.

**Record:** Selecting record brings you to a message select screen and allows you to select messages 1 through 8. Upon selection of a message, the device will begin recording. While recording, the user may stop recording or return to top menu.

**Delete:** Selecting delete brings you to a message select screen and allows you to select messages 1 through 8. Selecting a message brings up a confirmation window. Confirming deletes the message from memory by resetting the timing of the recording.

**Delete All:** Selecting delete all brings you to a confirmation menu. Confirming this option will delete all messages from the system.

**Volume:** Selecting volume will bring a new window up to allow volume control using the left and right buttons.

## System Block Diagram

Show a detailed diagram of the system design. This should include all major blocks and ICs, and show all datapaths and control signals.

[see diagram 1 and diagram 2]

## System Functional Flow

Include a detailed flow diagram, FSMD, pseudo code, or whatever it takes to show precisely how the system works. This needs to be detailed out at the control line level, a sequence of specific events that accomplish that functionality. If you are using an FSM, for instance, show each state and which controls are asserted in that state, along with what causes each state transition. If you are using pseudo code, again show the case statements, loops, decisions, etc., that lead to each control line being asserted.

On system power up, the system goes through initialization. The lcd initializes to 4 bit mode using the lcd state machine which is setup to output the correct timings for the function and mode settings. After the initial settings are complete, the lcd displays a welcome message until a button is pressed. The AC97 codec is also initialized using the ac97 commands module. This module uses a state machine to iterate through setting all relevant settings like source and microphone. After both the lcd and ac97 are initialized, the system is ready for user input and will leave the welcome message machine when it is received, taking the user to the top menu.

During run time, the system latches button presses and passes them into a picoblaze implementation of a state machine to generate an encoded output that drives another picoblaze. The data is passed into the secondary picoblaze as an 8 bit value with the top 4 bits representing the lcd menu to display and the bottom 4 bits representing the positioning of the cursor. The second picoblaze uses this data to generate the appropriate LCD commands, letter by letter, and passes them into a final verilog module which takes the ascii values and converts them into the timing diagrams that run the lcd. The system remains responsive to button presses because of the high clock frequency of the system and the relatively low amount of audio cycles needed for recording and playback.

The ac97 always sends and receives data serially and interfaces with the memory directly for playback and recording. Each of those states are triggered within the first picoblaze, as it keeps track of the current position the user is in the system

## Code for Audio Codec

Include source code for the main controller. The length of this will vary widely; depending on how much of your design's functionality is in software.

```
1    `timescale 1ns / 1ps
2
3
4    module streaming_file_system(
5        command, mem_full, fnumber, ready,
6        data_in, data_out, sync,
7        ram_clock,
8        this_reset,
9        clk_out,
10
11        // RAM hardware pins
12        hw_ram_rasn, hw_ram_casn,
13        hw_ram_wen, hw_ram_ba, hw_ram_udqs_p, hw_ram_udqs_n,
14        hw_ram_ldqs_p, hw_ram_ldqs_n, hw_ram_udm, hw_ram_ldm, hw_ram_ck,
15        hw_ram_ckn, hw_ram_cke, hw_ram_odt,
16        hw_ram_ad, hw_ram_dq, hw_rzq_pin, hw_zio_pin
17    );
18
19    parameter MESSAGE_BITS = 3;
20    parameter MEM_ADDRESS_BITS = 26;
21
22    input [2:0] command;
23    output reg mem_full;
24    input [2:0] fnumber;
25    // input [MEM_ADDRESS_BITS-MESSAGE_BITS-1:0] flen;
26    input [7:0] data_in;
27    output reg [7:0] data_out;
28    input sync;
29    input ram_clock;
30    input this_reset;
31    output reg ready;
32
33    output clk_out;
34
35    reg [MESSAGE_BITS-1:0] fnumber_addr;
36    reg [MEM_ADDRESS_BITS-MESSAGE_BITS-1:0] offset;
```

```

37  wire [MEM_ADDRESS_BITS-1:0] full_ram_addr;
38  assign full_ram_addr = {fnumber_addr, offset};
39
40  reg [MEM_ADDRESS_BITS-MESSAGE_BITS-1:0] fsizes [0:7]; // 8 long array
    of 23 bit numbers
41
42  wire [MEM_ADDRESS_BITS-1:0] max_ram_address;
43  reg [7:0] ram_data_in;
44  wire [7:0] ram_data_out;
45  reg ram_read_request;
46  reg ram_read_ack;
47  wire ram_rdy;
48  wire ram_rd_data_pres;
49  reg ram_write_enable;
50
51  // RAM hardware bullshit
52  output hw_ram_rasn;
53  output hw_ram_casn;
54  output hw_ram_wen;
55  output [2:0] hw_ram_ba;
56  inout hw_ram_udqs_p;
57  inout hw_ram_udqs_n;
58  inout hw_ram_ldqs_p;
59  inout hw_ram_ldqs_n;
60  output hw_ram_udm;
61  output hw_ram_ldm;
62  output hw_ram_ck;
63  output hw_ram_ckn;
64  output hw_ram_cke;
65  output hw_ram_odt;
66  output [12:0] hw_ram_ad;
67  inout [15:0] hw_ram_dq;
68  inout hw_rzq_pin;
69  inout hw_zio_pin;
70
71  // Instantiate the RAM
72  ram_interface_wrapper myram (
73      .address(full_ram_addr),
74      .data_in(ram_data_in),
75      .write_enable(ram_write_enable),
76      .read_request(ram_read_request),
77      .read_ack(ram_read_ack),
78      .data_out(ram_data_out),
79      .reset(this_reset),
80      .clk(ram_clock),

```

```

81
82     .hw_ram_rasn(hw_ram_rasn),
83     .hw_ram_casn(hw_ram_casn),
84     .hw_ram_wen(hw_ram_wen),
85     .hw_ram_ba(hw_ram_ba),
86     .hw_ram_udqs_p(hw_ram_udqs_p),
87     .hw_ram_udqs_n(hw_ram_udqs_n),
88     .hw_ram_ldqs_p(hw_ram_ldqs_p),
89     .hw_ram_ldqs_n(hw_ram_ldqs_n),
90     .hw_ram_udm(hw_ram_udm),
91     .hw_ram_ldm(hw_ram_ldm),
92     .hw_ram_ck(hw_ram_ck),
93     .hw_ram_ckn(hw_ram_ckn),
94     .hw_ram_cke(hw_ram_cke),
95     .hw_ram_odt(hw_ram_odt),
96     .hw_ram_ad(hw_ram_ad),
97     .hw_ram_dq(hw_ram_dq),
98     .hw_rzq_pin(hw_rzq_pin),
99     .hw_zio_pin(hw_zio_pin),
100
101     .clkout(clk_out),
102     .sys_clk(clk_out),
103     .rdy(ram_rdy),
104     .rd_data_pres(ram_rd_data_pres),
105     .max_ram_address()
106 );
107
108
109     parameter c_play = 1;
110     parameter c_pause = 2;
111     parameter c_record = 3;
112     parameter c_delete = 4;
113     parameter c_delete_all = 5;
114
115
116     parameter s_wait_command = 4'b0000;
117     parameter s_finish = 4'b0001;
118     parameter s_delete = 4'b0010;
119     parameter s_delete_all = 4'b0011;
120     parameter s_play = 4'b0100;
121     parameter s_play2 = 4'b0101;
122     parameter s_play3 = 4'b0110;
123     parameter s_record = 4'b0111;
124     parameter s_record2 = 4'b1000;
125     parameter s_record3 = 4'b1001;

```



```

126
127     (* FSM_ENCODING="SEQUENTIAL", SAFE_IMPLEMENTATION="NO" *)
128     reg [3:0] state =s_finish;
129
130     always@(posedge clk_out)
131     if (this_reset) begin
132         state <= s_wait_command;
133         ram_read_request <= 0;
134         ram_read_ack <= 0;
135         ram_write_enable <= 0;
136         fsizes[0] <= 0;
137         fsizes[1] <= 0;
138         fsizes[2] <= 0;
139         fsizes[3] <= 0;
140         fsizes[4] <= 0;
141         fsizes[5] <= 0;
142         fsizes[6] <= 0;
143         fsizes[7] <= 0;
144
145     end
146     else
147         (* FULL_CASE, PARALLEL_CASE *) case (state)
148         s_wait_command : begin
149             if (command == c_play) begin
150                 state <= s_play;
151                 offset <= 0;
152                 fnumber_addr <= fnumber;
153                 ready <= 0;
154             end
155
156             else if (command == c_record) begin
157                 state <= s_record;
158                 fnumber_addr <= fnumber;
159                 offset <= 0;
160                 ready <= 0;
161             end
162
163             else if (command == c_delete) begin
164                 state <= s_delete;
165                 fnumber_addr <= fnumber;
166                 ready <= 0;
167             end
168
169             else if (command == c_delete_all) begin

```

```

170         state <= s_delete_all;
171         fnumber_addr <= fnumber;
172         ready <= 0;
173     end
174
175     else begin
176         ready <= 1;
177         ram_read_request <= 0;
178         ram_read_ack <= 0;
179     end
180
181 end
182
183 s_finish : begin
184     if (!command) begin
185         mem_full <= 0;
186         ready <= 0;
187         state <= s_wait_command;
188     end
189 end
190
191 s_delete : begin
192     fsizes[fnumber_addr] <= 0;
193     state <= s_finish;
194 end
195
196 s_delete_all : begin
197     fsizes[0] <= 0;
198     fsizes[1] <= 0;
199     fsizes[2] <= 0;
200     fsizes[3] <= 0;
201     fsizes[4] <= 0;
202     fsizes[5] <= 0;
203     fsizes[6] <= 0;
204     fsizes[7] <= 0;
205     state <= s_finish;
206 end
207
208 s_play : begin
209     ram_read_ack <= 0;
210     if (offset == fsizes[fnumber_addr])
// Are we at the end of the message?
211         state <= s_finish;
212
213     else if (!sync)

```

```

214         state <= s_play2;
215     end
216
217     s_play2 : begin
218         if (sync && (command == c_play)) begin
219             // Wait for the frame sync to get the next byte
220             state <= s_play3;
221             ram_read_request <= 1;
222         end
223         else if (command == c_pause)
224             // If pause, just stay in this block
225             state <= s_play2;
226         else if (command != c_play)
227             // Something other than play means finish up and return to function select
228             state <= s_finish;
229         else
230             state <= s_play2;
231         end
232
233     s_play3 : begin
234         if (!ram_rd_data_pres)
235             // Wait for RAM to present the data
236             state <= s_play3;
237         else begin
238             data_out <= ram_data_out;
239             offset <= offset + 1;
240             ram_read_request <= 0;
241             // Do I need to deassert this more quickly?
242             ram_read_ack <= 1;
243             state <= s_play;
244         end
245     end
246
247     s_record : begin
248         if (command != c_record) begin
249             // When we finish recording, write out our file size
250             state <= s_finish;
251             fsizes[fnumber_addr] <= offset;
252         end
253
254         else if (sync) begin
255             // wait for frame sync to grab data and write
256             ram_data_in <= data_in;

```

```

251         ram_write_enable <= 1;
252         state <= s_record2;
253     end
254 end
255
256     s_record2 : begin
257         ram_write_enable <= 0;
258         offset <= offset + 1;
259         state <= s_record3;
260     end
261
262     s_record3 : begin
263         if (offset == 0) begin
264             // praying for rollover - max message length
265             mem_full <= 1;
266             fsizes[fnumber_addr] <= -1;
267             // please please wrap around
268             state <= s_finish;
269         end
270         else if (!sync)
271             // wait for sync to drop
272             state <= s_record;
273         end
274     endcase
275 endmodule

```

## Code for LCD Display

Include source code for the main controller. The length of this will vary widely; depending on how much of your design's functionality is in software.

**// Picoblaze #1 – processes current state of system, based on button presses. Sends 8 bit encoded messages to picoblaze #2. Bits [7:4] refer to the current menu (welcome message, top, play, record, delete, delete all, message select, confirmation)**

CONSTANT CONTROL, 00

CONSTANT READY\_SIG, 07

CONSTANT MEM\_FULL, 02

CONSTANT COMMAND, 03

CONSTANT FILE, 04

CONSTANT VOLUME\_OUTPUT, 05

CONSTANT LCD\_OUTPUT, 06

NAMEREG s0, MENU\_STATE

NAMEREG s1, FILE\_STATE

NAMEREG s2, TWO\_STATE

NAMEREG s3, MASTER\_STATE

NAMEREG s4, SEANS\_CONSTANT

NAMEREG s5, VOLUME

NAMEREG s6, LCD\_BUILD

NAMEREG s7, READY\_REG

NAMEREG s8, COMMAND\_REG

NAMEREG s9, FILE\_REG

NAMEREG sA, CONTROLREG

ENABLE INTERRUPT

WELCOME: ; WELCOME MESSAGE

LOAD LCD\_BUILD, A0

OUTPUT LCD\_BUILD, LCD\_OUTPUT

CALL WAIT\_STATE

CALL INPUT\_LOADER

MAIN: ;MAIN MENU

LOAD COMMAND\_REG, FF

OUTPUT COMMAND\_REG, COMMAND

CALL PUSH

MAIN\_MENU\_RS:

LOAD MENU\_STATE, 00

MAIN\_MENU:

LOAD MASTER\_STATE, 00

CALL WAIT\_STATE

CALL INPUT\_LOADER

COMPARE CONTROLREG, 01

JUMP Z, UP\_MAIN

COMPARE CONTROLREG, 02

JUMP Z, DOWN\_MAIN

COMPARE CONTROLREG, 04

JUMP Z, BACK

COMPARE CONTROLREG, 08

JUMP Z, SELECT\_MAIN

JUMP MAIN\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;MAIN UP/DOWN;;;;;;;;;;;;;;;;

UP\_MAIN:

COMPARE MENU\_STATE, 04

JUMP NZ, UP\_GOOD

JUMP MAIN\_MENU

UP\_GOOD:

ADD MENU\_STATE, 01

CALL PUSH

JUMP MAIN\_MENU

DOWN\_MAIN:

COMPARE MENU\_STATE, 00

JUMP NZ, DOWN\_GOOD

JUMP MAIN\_MENU

DOWN\_GOOD:

SUB MENU\_STATE, 01

CALL PUSH

JUMP MAIN\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;SELECT MAIN;;;;;;;;;;;;;;;;

SELECT\_MAIN: ;ROUTES TO MASTER SWITCH

COMPARE MENU\_STATE, 00

JUMP Z, MASTER\_PLAY

COMPARE MENU\_STATE, 01

JUMP Z, MASTER\_RECORD

COMPARE MENU\_STATE, 02

JUMP Z, MASTER\_DELETE

COMPARE MENU\_STATE, 03

JUMP Z, MASTER\_DEL\_ALL

COMPARE MENU\_STATE, 04

JUMP Z, MASTER\_VOL

;////////MASTER SWITCH//////////

MASTER\_MENU:

LOAD MASTER\_STATE, 00

CALL PUSH

JUMP MAIN\_MENU\_RS

MASTER\_PLAY:

LOAD MASTER\_STATE,01

CALL PUSH

JUMP FILE\_MENU\_RS

MASTER\_RECORD:

LOAD MASTER\_STATE,02

CALL PUSH

JUMP FILE\_MENU\_RS

MASTER\_DELETE:

LOAD MASTER\_STATE,03

CALL PUSH;

JUMP FILE\_MENU\_RS

MASTER\_PLAYING:

LOAD MASTER\_STATE,04



CALL PUSH

JUMP TWO\_OPTION\_MENU\_RS

MASTER\_DELETING:

LOAD MASTER\_STATE,05

CALL PUSH

JUMP TWO\_OPTION\_MENU\_RS

MASTER\_VOL:

LOAD MASTER\_STATE,06

CALL PUSH

JUMP TWO\_OPTION\_MENU\_RS

MASTER\_DEL\_ALL:

LOAD MASTER\_STATE,07

CALL PUSH

JUMP TWO\_OPTION\_MENU\_RS

MASTER\_PAUSED:

LOAD MASTER\_STATE,08

CALL PUSH

JUMP ONE\_OPTION\_MENU

MASTER\_RECORDING:

LOAD MASTER\_STATE, 09

CALL PUSH

JUMP ONE\_OPTION\_MENU

;;;;;;;;;;FILE\_MENU CONTROL;;

FILE\_MENU\_RS:

LOAD FILE\_STATE, 00

FILE\_MENU:

CALL WAIT\_STATE

CALL INPUT\_LOADER

COMPARE CONTROLREG, 01

JUMP Z, UP\_FILE

COMPARE CONTROLREG, 02

JUMP Z, DOWN\_FILE

COMPARE CONTROLREG, 04

JUMP Z, BACK

COMPARE CONTROLREG, 08

JUMP Z, SELECT\_FILE

JUMP FILE\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;FILE UP/DOWN;;

UP\_FILE:

COMPARE FILE\_STATE, 07

JUMP NZ, UP\_FILE\_GOOD ;if file number isnt max

JUMP FILE\_MENU ;otherwise return

UP\_FILE\_GOOD:

ADD FILE\_STATE, 01

CALL PUSH

JUMP FILE\_MENU

DOWN\_FILE:

COMPARE FILE\_STATE, 00

JUMP NZ, DOWN\_FILE\_GOOD ;if file number isnt min

JUMP FILE\_MENU ;other wise return

DOWN\_FILE\_GOOD:

SUB FILE\_STATE, 01

CALL PUSH

JUMP FILE\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;;;/SELECT\_FILE;;;;;;;;;;;;;;;;;;;;;;;;;;

SELECT\_FILE:

COMPARE MASTER\_STATE, 01

JUMP Z, PLAY\_MESSAGE

COMPARE MASTER\_STATE, 02

JUMP Z, RECORD\_MESSAGE

COMPARE MASTER\_STATE, 03

JUMP Z, MASTER\_DELETING

;;;;;;;;;;;;;;;;;;;;;;;;;;/SKIP;;;;;;;;;;;;;;;;;;;;;;;;;;

SKIP:

COMPARE FILE\_STATE, 07

JUMP Z, WRAP

ADD FILE\_STATE, 01

WRAP:

LOAD FILE\_STATE, 00

JUMP PLAY\_MESSAGE

;;;;;;;;;;;;;;;;;;;;;;;;PLAY;;;;;;;;;;;;;;;;;;;;;;;;

PLAY\_MESSAGE:

LOAD COMMAND\_REG, 01

CALL SEND\_COMMAND\_PRD

JUMP MASTER\_PLAYING

;;;;;;;;;;;;;;;;;;;;;;;;RECORD;;;;;;;;;;;;;;;;;;;;;;;;

RECORD\_MESSAGE:

LOAD COMMAND\_REG, 03

CALL SEND\_COMMAND\_PRD

JUMP MASTER\_RECORDING

;;;;;;;;;;;;;;;;;;;;;;;;DELETE;;;;;;;;;;;;;;;;;;;;;;;;

DELETE\_MESSAGE:

LOAD COMMAND\_REG, 04

CALL SEND\_COMMAND\_PRD

JUMP BACK

;;;;;;;;;;;;;;;;;;;;;;;;TWO OPTION MENU///for pause/skip, yes/no ,vol up/vol down

TWO\_OPTION\_MENU\_RS:

LOAD TWO\_STATE,00

TWO\_OPTION\_MENU:

CALL WAIT\_STATE

CALL INPUT\_LOADER

COMPARE CONTROLREG, 01

JUMP Z, TWO\_OPT\_FLIP

COMPARE CONTROLREG, 02

JUMP Z, TWO\_OPT\_FLIP

COMPARE CONTROLREG, 04

JUMP Z, BACK

COMPARE CONTROLREG, 08

JUMP Z, SELECT\_TWO\_OPT

JUMP TWO\_OPTION\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;;TWO OPT UP/DOWN;;;;;;;;;;;;;;;;;;;;;;;;;

TWO\_OPT\_FLIP:

COMPARE TWO\_STATE, 00

JUMP Z, TWO\_STATE\_UP

JUMP Z, TWO\_STATE\_DOWN

TWO\_STATE\_UP:

LOAD TWO\_STATE,01

CALL PUSH

JUMP TWO\_OPTION\_MENU

TWO\_STATE\_DOWN:

LOAD TWO\_STATE,00

CALL PUSH

JUMP TWO\_OPTION\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;;TWO OPT SELECT;;;;;;;;;;;;;;;;;;;;;;;;;

SELECT\_TWO\_OPT:

COMPARE MASTER\_STATE,04 ; playing

JUMP Z, PAUSE\_SKIP

COMPARE MASTER\_STATE,05 ; deleting

JUMP Z, YES\_NO

COMPARE MASTER\_STATE,06 ; volume

JUMP Z, UP\_DOWN

COMPARE MASTER\_STATE,07 ; deleting all

JUMP Z, YES\_NO\_ALL

PAUSE\_SKIP:

COMPARE TWO\_STATE,00

JUMP Z, PAUSE

COMPARE TWO\_STATE,01

JUMP Z, SKIP

YES\_NO:

COMPARE TWO\_STATE,00

JUMP Z, BACK

COMPARE TWO\_STATE,01

JUMP Z, DELETE\_MESSAGE

YES\_NO\_ALL:

COMPARE TWO\_STATE,00

JUMP Z, BACK

COMPARE TWO\_STATE,01

JUMP Z, DELETE\_ALL

UP\_DOWN:

COMPARE TWO\_STATE,00

JUMP Z, VOL\_UP

COMPARE TWO\_STATE,01

JUMP Z, VOL\_DOWN

```

;/////////////////////////////////VOL UP/DOWN/////////////////////////////////

```

VOL\_UP:

## COMPARE VOLUME, 1F

JUMP NZ, UP\_VOL

JUMP ONE\_OPTION\_MENU

VOL\_DOWN:

COMPARE VOLUME,00

JUMP NZ, DOWN\_VOL

JUMP ONE\_OPTION\_MENU

UP\_VOL:

ADD VOLUME,01

## OUTPUT VOLUME, VOLUME\_OUTPUT

JUMP TWO\_OPTION\_MENU

DOWN\_VOL:

SUB VOLUME,01

OUTPUT VOLUME, VOLUME\_OUTPUT

JUMP TWO\_OPTION\_MENU

[illegible]

PAUSE:

LOAD COMMAND\_REG, 02

## OUTPUT COMMAND\_REG, COMMAND

JUMP MASTER\_PAUSED

```

;/////////////////////////////////RESUME_MESSAGE/////////////////////////////////

```

RESUME\_MESSAGE:

LOAD COMMAND\_REG, 01

OUTPUT COMMAND\_REG, COMMAND

JUMP MASTER\_PLAYING

;;;;;;;;;;;;;;;;;;;;;;;;;DELETE\_ALL;;;;;;;;;;;;;;;;;;;;;;;;;

DELETE\_ALL:

LOAD COMMAND\_REG, 05

CALL SEND\_COMMAND\_PRD

JUMP BACK

;;;;;;;;;;;;;;;;;;;;;;;;;ONE\_OPTION;;;;;;;;;;;;;;;;;;;;;;;;;

ONE\_OPTION\_MENU:

CALL WAIT\_STATE

CALL INPUT\_LOADER

COMPARE CONTROLREG,08

JUMP Z, ONE\_OPT\_SEL

JUMP ONE\_OPTION\_MENU

ONE\_OPT\_SEL:

COMPARE MASTER\_STATE,08

JUMP Z, RESUME\_MESSAGE ;RESUME!!!

COMPARE MASTER\_STATE,09

JUMP Z, STOP

JUMP ONE\_OPTION\_MENU

;;;;;;;;;;;;;;;;;;;;;;;;;STOP!!!!;;;;;;;;;;;;;;;;;;;;;;;;;

STOP:

LOAD SEANS\_CONSTANT,00



```

        OUTPUT SEANS_CONSTANT, COMMAND

        JUMP BACK

;/////////////////////////////////BACK!!!!/////////////////////////////////

BACK:          ;ONE BACK TO RULE THEM ALL!!!!

        JUMP MASTER_MENU

;/////////////////////////////////SEND_COMMAND P/R/D //////////////////////////////////

SEND_COMMAND_PRD:

        OUTPUT FILE_STATE, FILE

        LOAD SEANS_CONSTANT, 00

        OUTPUT SEANS_CONSTANT, COMMAND

        READY_WAIT:

        INPUT READY_REG, READY_SIG

        COMPARE READY_REG, 01

        JUMP NZ, READY_WAIT

        OUTPUT COMMAND_REG, COMMAND

;//////////WAIT STATE//////////

WAIT_STATE:

        INPUT CONTROLREG, CONTROL

        COMPARE CONTROLREG, 00      ;wait state

        JUMP NZ, WAIT_STATE

        RETURN

;//////////INPUT LOADER//////////

INPUT_LOADER:

        INPUT CONTROLREG, CONTROL ;ADD USB SHIT HERE!!!!

        COMPARE CONTROLREG, 00

```

JUMP Z, INPUT\_LOADER

RETURN

;//////////LCD\_PUSH//////////

PUSH:

LOAD LCD\_BUILD, MASTER\_STATE

SLO LCD\_BUILD

SLO LCD\_BUILD

SLO LCD\_BUILD

SLO LCD\_BUILD

COMPARE MASTER\_STATE,00

JUMP Z, MAIN\_PUSH

COMPARE MASTER\_STATE,01

JUMP Z, FILE\_PUSH

COMPARE MASTER\_STATE,02

JUMP Z, FILE\_PUSH

COMPARE MASTER\_STATE,03

JUMP Z, FILE\_PUSH

COMPARE MASTER\_STATE,04

JUMP Z, TWO\_PUSH

COMPARE MASTER\_STATE,05

JUMP Z, TWO\_PUSH

COMPARE MASTER\_STATE,06

JUMP Z, TWO\_PUSH

COMPARE MASTER\_STATE,07

JUMP Z, TWO\_PUSH

COMPARE MASTER\_STATE,08

JUMP Z, ONE\_PUSH

COMPARE MASTER\_STATE,09

JUMP Z, ONE\_PUSH

MAIN\_PUSH:

ADD LCD\_BUILD, MENU\_STATE

JUMP PUSH\_PUSH

FILE\_PUSH:

ADD LCD\_BUILD, FILE\_STATE

JUMP PUSH\_PUSH

TWO\_PUSH:

ADD LCD\_BUILD, TWO\_STATE

JUMP PUSH\_PUSH

ONE\_PUSH:

ADD LCD\_BUILD, 00

JUMP PUSH\_PUSH

PUSH\_PUSH:

OUTPUT LCD\_BUILD, LCD\_OUTPUT

RETURN

JUMP MAIN\_MENU

ISR:

LOAD LCD\_BUILD, B0

OUTPUT LCD\_BUILD, LCD\_OUTPUT

LOAD COMMAND\_REG, 00

OUTPUT COMMAND\_REG, COMMAND

CALL WAIT\_STATE

CALL INPUT\_LOADER

RETURNI ENABLE

ADDRESS 3FF

JUMP ISR

**// Picoblaze #2 – contains the characters for the various lcd messages. Receives input from picoblaze #1 and outputs data to lcd module (not lcd, yet).**

CONSTANT ENTERCODE, 01

CONSTANT COMMAND, 04

CONSTANT EXITCODE, 02

CONSTANT READY\_SIG, 03

NAMEREG s4, READY\_REG

NAMEREG s0, ENTER\_CODE

NAMEREG s1, EXIT\_CODE

NAMEREG s2, MENU

NAMEREG s3, PLACE

NAMEREG s5, COMMAND\_REG

NAMEREG s6, LAST\_CODE

LOAD LAST\_CODE, 00

BEGIN:

INPUT ENTER\_CODE, ENTERCODE

COMPARE LAST\_CODE, ENTER\_CODE

JUMP Z, BEGIN

LOAD LAST\_CODE, ENTER\_CODE

LOAD MENU, ENTER\_CODE

LOAD PLACE, ENTER\_CODE

AND PLACE, 0F

SRO MENU

SRO MENU

SRO MENU

SRO MENU

COMPARE MENU, 00

JUMP Z, MAIN\_MENU

COMPARE MENU, 01

JUMP Z, FILE\_MENU

COMPARE MENU, 02

JUMP Z, FILE\_MENU

COMPARE MENU, 03

JUMP Z, FILE\_MENU

COMPARE MENU, 04

JUMP Z, PLAY\_MENU

COMPARE MENU, 05

JUMP Z, DEL\_MENU

COMPARE MENU, 06

JUMP Z, VOL\_MENU

COMPARE MENU, 07

JUMP Z, DEL\_MENU

COMPARE MENU, 08

JUMP Z, PAUSE\_MENU

COMPARE MENU, 09

JUMP Z, RECORD\_MENU

COMPARE MENU,0A

JUMP Z, WELCOME

COMPARE MENU,0B

JUMP Z, MEM\_FULL

MAIN\_MENU:

COMPARE PLACE, 00

CALL Z, MAIN1

JUMP Z, S\_1

COMPARE PLACE, 01

CALL Z, MAIN1

JUMP Z, S\_2

COMPARE PLACE, 02

CALL Z, MAIN1

JUMP Z, S\_3

COMPARE PLACE, 03

CALL Z, MAIN2

JUMP Z, S\_1

COMPARE PLACE, 04

CALL Z, MAIN2

JUMP Z, S\_3

FILE\_MENU:

COMPARE PLACE, 00

CALL Z, FILE1\_4

JUMP Z, S\_1

COMPARE PLACE, 01

CALL Z, FILE1\_4

JUMP Z, S\_3

COMPARE PLACE, 02

CALL Z, FILE2\_4

JUMP Z,S\_1

COMPARE PLACE, 03

CALL Z, FILE2\_4

JUMP Z,S\_3

COMPARE PLACE, 04

CALL Z,FILE3\_4

JUMP Z,S\_1

COMPARE PLACE, 05

CALL Z, FILE3\_4

JUMP Z,S\_3

COMPARE PLACE, 06

CALL Z, FILE4\_4

JUMP Z,S\_1

COMPARE PLACE, 07

CALL Z, FILE4\_4

JUMP Z,S\_3

PLAY\_MENU:

CALL PAUSE\_SKIP

COMPARE PLACE, 00

JUMP Z, S\_1 ;PAUSE



JUMP NZ, S\_3 ;SKIP

DEL\_MENU:

CALL CAN\_CON

COMPARE PLACE,00

JUMP Z, S\_1 ;NO

JUMP NZ, S\_3 ;YES

VOL\_MENU:

CALL UP\_DOWN

COMPARE PLACE, 00

JUMP Z, S\_1;up

JUMP NZ, S\_3;DOWN

PAUSE\_MENU:

CALL RESUME

JUMP BEGIN

RECORD\_MENU:

CALL STOP

JUMP BEGIN

MAIN1:

CALL UPLINE

CALL PRINT\_MAIN\_LEFT

CALL DROPLINE

RETURN

MAIN2:

CALL UPLINE

CALL PRINT\_MAIN\_RIGHT

CALL DROPLINE

RETURN

FILE1\_4:

CALL UPLINE

CALL PRINTFILE1\_2

CALL DROPLINE

RETURN

FILE2\_4:

CALL UPLINE

CALL PRINTFILE3\_4

CALL DROPLINE

RETURN

FILE3\_4:

CALL UPLINE

CALL PRINTFILE5\_6

CALL DROPLINE

RETURN

FILE4\_4:

CALL UPLINE

CALL PRINTFILE7\_8

CALL DROPLINE

RETURN

PAUSE\_SKIP:

CALL UPLINE

CALL PRINT\_PAUSE\_SKIP

CALL DROPLINE

RETURN

RESUME:

CALL UPLINE

CALL PRINT\_RESUME

CALL DROPLINE

RETURN

STOP:

CALL UPLINE

CALL PRINT\_STOP

RETURN

UP\_DOWN:

CALL UPLINE

CALL PRINT\_UP\_DOWN

RETURN

CAN\_CON:

CALL UPLINE

CALL PRINT\_CAN\_CON

RETURN

WELCOME:

CALL UPLINE

CALL PRINT\_WELCOME

RETURN

MEM\_FULL:

CALL UPLINE

CALL PRINT\_MEM\_FULL

RETURN

S\_1:

LOAD EXIT\_CODE,3E

CALL PRINTFILE

LOAD EXIT\_CODE,7C

CALL PRINTFILE

LOAD EXIT\_CODE,7C

CALL PRINTFILE

LOAD EXIT\_CODE,3C

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

```
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
JUMP BEGIN
```

S\_2:

```
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE

LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,3E
CALL PRINTFILE
LOAD EXIT_CODE,7C
```

```
CALL PRINTFILE
LOAD EXIT_CODE,7C
CALL PRINTFILE
LOAD EXIT_CODE,3C
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
JUMP BEGIN
```

S\_3:

```
LOAD EXIT_CODE,20
CALL PRINTFILE
```

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,3E

CALL PRINTFILE

LOAD EXIT\_CODE,7C

CALL PRINTFILE

LOAD EXIT\_CODE,7C

CALL PRINTFILE

LOAD EXIT\_CODE,3C

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

JUMP BEGIN

DROPLINE:

INPUT READY\_REG, READY\_SIG

COMPARE READY\_REG, 01

JUMP NZ, DROPLINE

LOAD COMMAND\_REG,01

OUTPUT COMMAND\_REG, COMMAND

RETURN

UPLINE:

INPUT READY\_REG, READY\_SIG

COMPARE READY\_REG, 01

JUMP NZ, UPLINE

LOAD COMMAND\_REG,00

OUTPUT COMMAND\_REG, COMMAND

RETURN

PRINT\_MAIN\_LEFT:

LOAD EXIT\_CODE,50

CALL PRINTFILE



LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,41

CALL PRINTFILE

LOAD EXIT\_CODE,59

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,52

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,43

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,44

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,2d

CALL PRINTFILE

LOAD EXIT\_CODE,3e

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

RETURN

PRINT\_MAIN\_RIGHT:

LOAD EXIT\_CODE,3c

CALL PRINTFILE

LOAD EXIT\_CODE,2d

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,44

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,56

CALL PRINTFILE

```
LOAD EXIT_CODE,4f
CALL PRINTFILE
LOAD EXIT_CODE,4c
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,3e
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
RETURN
```

PRINTFILE1\_2:

```
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,46
CALL PRINTFILE
LOAD EXIT_CODE,49
CALL PRINTFILE
LOAD EXIT_CODE,4c
```

```
CALL PRINTFILE
LOAD EXIT_CODE,45
CALL PRINTFILE
LOAD EXIT_CODE,31
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,46
CALL PRINTFILE
LOAD EXIT_CODE,49
CALL PRINTFILE
LOAD EXIT_CODE,4c
CALL PRINTFILE
LOAD EXIT_CODE,45
CALL PRINTFILE
LOAD EXIT_CODE,32
CALL PRINTFILE
LOAD EXIT_CODE,2d
CALL PRINTFILE
LOAD EXIT_CODE,3e
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
RETURN
```

PRINTFILE3\_4:

LOAD EXIT\_CODE,3c

CALL PRINTFILE

LOAD EXIT\_CODE,2d

CALL PRINTFILE

LOAD EXIT\_CODE,46

CALL PRINTFILE

LOAD EXIT\_CODE,49

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,33

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,46

CALL PRINTFILE

LOAD EXIT\_CODE,49

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,34

```
CALL PRINTFILE
LOAD EXIT_CODE,2d
CALL PRINTFILE
LOAD EXIT_CODE,3e
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
RETURN
```

PRINTFILES5\_6:

```
LOAD EXIT_CODE,3c
CALL PRINTFILE
LOAD EXIT_CODE,2d
CALL PRINTFILE
LOAD EXIT_CODE,46
CALL PRINTFILE
LOAD EXIT_CODE,49
CALL PRINTFILE
LOAD EXIT_CODE,4c
CALL PRINTFILE
LOAD EXIT_CODE,45
CALL PRINTFILE
LOAD EXIT_CODE,35
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
```

LOAD EXIT\_CODE,46

CALL PRINTFILE

LOAD EXIT\_CODE,49

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,36

CALL PRINTFILE

LOAD EXIT\_CODE,2d

CALL PRINTFILE

LOAD EXIT\_CODE,3e

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

RETURN

PRINTFILE7\_8:

LOAD EXIT\_CODE,3c

CALL PRINTFILE

LOAD EXIT\_CODE,2d

CALL PRINTFILE

LOAD EXIT\_CODE,46

CALL PRINTFILE

LOAD EXIT\_CODE,49

CALL PRINTFILE  
LOAD EXIT\_CODE,4c  
CALL PRINTFILE  
LOAD EXIT\_CODE,45  
CALL PRINTFILE  
LOAD EXIT\_CODE,37  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,46  
CALL PRINTFILE  
LOAD EXIT\_CODE,49  
CALL PRINTFILE  
LOAD EXIT\_CODE,4c  
CALL PRINTFILE  
LOAD EXIT\_CODE,45  
CALL PRINTFILE  
LOAD EXIT\_CODE,38  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,30  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE



RETURN

PRINT\_UP\_DOWN:

LOAD EXIT\_CODE,56

CALL PRINTFILE

LOAD EXIT\_CODE,4f

CALL PRINTFILE

LOAD EXIT\_CODE,4c

CALL PRINTFILE

LOAD EXIT\_CODE,5f

CALL PRINTFILE

LOAD EXIT\_CODE,55

CALL PRINTFILE

LOAD EXIT\_CODE,50

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,56

CALL PRINTFILE

LOAD EXIT\_CODE,4c

```
CALL PRINTFILE
LOAD EXIT_CODE,5f
CALL PRINTFILE
LOAD EXIT_CODE,44
CALL PRINTFILE
LOAD EXIT_CODE,4f
CALL PRINTFILE
LOAD EXIT_CODE,57
CALL PRINTFILE
LOAD EXIT_CODE,4e
CALL PRINTFILE
RETURN
```

PRINT\_RESUME:

```
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
```

LOAD EXIT\_CODE,52

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,53

CALL PRINTFILE

LOAD EXIT\_CODE,55

CALL PRINTFILE

LOAD EXIT\_CODE,4d

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

RETURN

PRINT\_CAN\_CON:

LOAD EXIT\_CODE,43

CALL PRINTFILE

LOAD EXIT\_CODE,41

CALL PRINTFILE  
LOAD EXIT\_CODE,4e  
CALL PRINTFILE  
LOAD EXIT\_CODE,43  
CALL PRINTFILE  
LOAD EXIT\_CODE,45  
CALL PRINTFILE  
LOAD EXIT\_CODE,4c  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,43  
CALL PRINTFILE  
LOAD EXIT\_CODE,4f  
CALL PRINTFILE  
LOAD EXIT\_CODE,4e  
CALL PRINTFILE  
LOAD EXIT\_CODE,46  
CALL PRINTFILE  
LOAD EXIT\_CODE,49  
CALL PRINTFILE

LOAD EXIT\_CODE,52

CALL PRINTFILE

LOAD EXIT\_CODE,4d

CALL PRINTFILE

RETURN

PRINT\_PAUSE\_SKIP:

LOAD EXIT\_CODE,50

CALL PRINTFILE

LOAD EXIT\_CODE,41

CALL PRINTFILE

LOAD EXIT\_CODE,55

CALL PRINTFILE

LOAD EXIT\_CODE,53

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

```
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,53
CALL PRINTFILE
LOAD EXIT_CODE,4B
CALL PRINTFILE
LOAD EXIT_CODE,49
CALL PRINTFILE
LOAD EXIT_CODE,50
CALL PRINTFILE
RETURN
```

PRINT\_STOP:

```
LOAD EXIT_CODE,53
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,54
CALL PRINTFILE
```

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,4f

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,50

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

RETURN

PRINT\_WELCOME:

LOAD EXIT\_CODE,20

CALL PRINTFILE  
LOAD EXIT\_CODE,54  
CALL PRINTFILE  
LOAD EXIT\_CODE,48  
CALL PRINTFILE  
LOAD EXIT\_CODE,49  
CALL PRINTFILE  
LOAD EXIT\_CODE,53  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,57  
CALL PRINTFILE  
LOAD EXIT\_CODE,41  
CALL PRINTFILE  
LOAD EXIT\_CODE,53  
CALL PRINTFILE  
LOAD EXIT\_CODE,20  
CALL PRINTFILE  
LOAD EXIT\_CODE,45  
CALL PRINTFILE  
LOAD EXIT\_CODE,41  
CALL PRINTFILE  
LOAD EXIT\_CODE,53  
CALL PRINTFILE



LOAD EXIT\_CODE,59

CALL PRINTFILE

LOAD EXIT\_CODE,21

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

RETURN

PRINT\_MEM\_FULL:

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,20

CALL PRINTFILE

LOAD EXIT\_CODE,4d

CALL PRINTFILE

LOAD EXIT\_CODE,45

CALL PRINTFILE

LOAD EXIT\_CODE,4d

CALL PRINTFILE

LOAD EXIT\_CODE,4f

CALL PRINTFILE

LOAD EXIT\_CODE,52

CALL PRINTFILE

LOAD EXIT\_CODE,59

CALL PRINTFILE

LOAD EXIT\_CODE,20

```
CALL PRINTFILE
LOAD EXIT_CODE,46
CALL PRINTFILE
LOAD EXIT_CODE,55
CALL PRINTFILE
LOAD EXIT_CODE,4c
CALL PRINTFILE
LOAD EXIT_CODE,4c
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
LOAD EXIT_CODE,20
CALL PRINTFILE
RETURN
```

PRINTFILE:

```
INPUT READY_REG, READY_SIG
COMPARE READY_REG, 01
JUMP NZ, PRINTFILE
OUTPUT EXIT_CODE,EXITCODE
RETURN
```

## Discussion and Conclusions

In this section, discuss how you arrived at your major decisions (why you put X in hardware and Y in software, how you selected the memory chips you used, etc.). Discuss any aspects of your design that you would do differently if you had it all to do over again, and why. Include any and all thoughts you have on the project, how it could have been done differently or better, etc.

If we could start over again, we probably would have divided the workflow a little bit differently. The lcd module proved to be the most difficult thing to implement for us, and instead of trying to adapt an 8 bit example code, we should have implemented our own from the beginning. The biggest thing to take from this project is to learn the data sheet of a component thoroughly before trying to use it. Almost always, we were able to implement the components quickly, but not at 100%. Resolving issues only came after a thorough understanding of the system and what was expected. As it takes a few minutes to compile and run the Verilog on the FPGA, it is worth taking the time to understand what is happening on a very detailed level instead of just trying to change things and make it work.

The design of the project initially began with using one module for each component and a top level wrapper module. The ac97 module was the easiest to create, but typos kept us busy for quite a while. Integrating the memory and testing it was very straight forward, but difficult to understand. The LCD was the biggest issue because of how the example implemented the setup and write states. Eventually, we rewrote the entire lcd driver in Verilog, and fed it ascii values via a picoblaze, which was in turn was fed by another picoblaze which took the button inputs and ran them through a state machine to determine the output values and the lcd message to display.

Overall, this project was difficult because it was very hard to work together on many parts. A majority of our project was spent with one person coding while the other two were doing side tasks or trying to help troubleshoot stuff. In the future, I'd like to learn how to better debug signals, especially for the on board components, such as the lcd display and the ac97 IO stream.